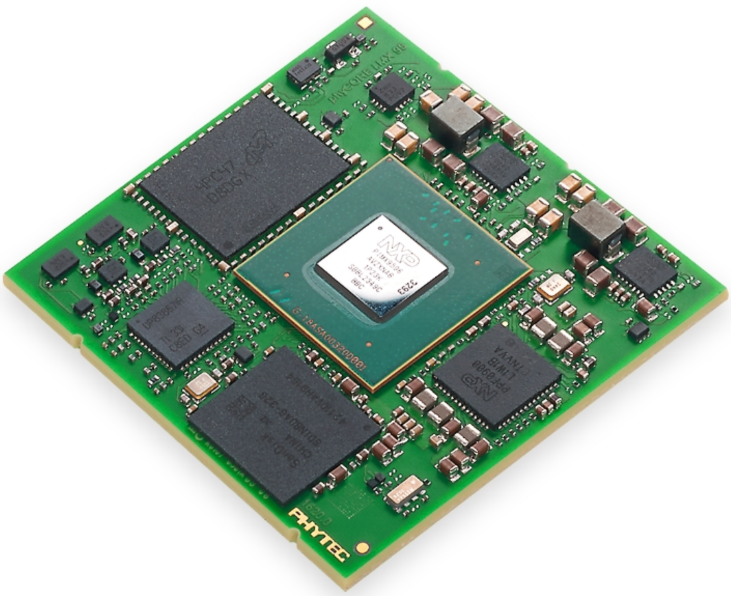
phyCORE-i.MX 95 FPSC &
Libra Development Board



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Hardware Manual - phyFLEX-i.MX 95 FPSC/Libra Development Board (1620.3/1618.2) (L-1075e.A3)	
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1 Information on this Manual

This hardware manual describes the PFL-G-02 (FPSC) System on Module, referred to as phyFLEX®-i.MX 95, and the PBA-BG-41, referred to as the Libra Development Board. This manual also specifies the phyFLEX-i.MX 95 and Libra Development Board's design and function. Precise specifications for the NXP® Semiconductor i.MX 95 microcontrollers can be found in the i.MX 95 Microcontroller Data Sheet/Reference Manual.

There will be several changes and additions to this manual. New versions will be released in the future with no notice. Please make sure that you are using the latest version of this manual when working with your product.

1.1 Future Proof Solder Core

The PFL-G-02 System on Module, referred to as phyFLEX®-i.MX 95 FPSC is designed according to FPSC Gamma Feature Set Specifications (LAN-118e.A6).

More information about PHYTEC's Future Proof Solder Core can be found on our website.

1.2 Design Considerations

The schematics shown in this hardware manual are believed to be correct. However, correctness can not be guaranteed. The schematics have been pulled from PHYTEC's designs that have been built, tested, and are known to work. The schematics have been re-formatted to fit better in this hardware manual.

Many hardware examples and suggestions are given in the following pages. Designing the phyFLEX System on Module onto a Carrier Board is generally straightforward. However, before committing to a particular active component selection when designing a carrier board, it is wise to check out the software driver support for those components. A particular device may be supported in, for example, Linux but not in Windows Embedded Compact 7. Your overall project may go smoother if you pick components that are already supported in your target OS. The premade selections for our reference designs, for example, our Single Board Computers, are typically focused on using components that are well supported under Linux.

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyFLEX-i.MX 95 on the Libra Development Board. Be aware that not all components need to be considered when designing your own carrier board.

2 Preface

As a member of PHYTEC's product family, the phyFLEX® SoM can be populated with different controllers, various types of memory (RAM, NAND flash, eMMC), and many other features. This, in turn, offers increased types of functions and configurations. PHYTEC supports a variety of 8/16/32/64-bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and evaluation platform
2. As insert-ready, fully functional phyFLEX® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "reinvent" microcontroller circuitry. Furthermore, much of the value of the phyFLEX® module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce development time and risk and allows for increased focus on product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative, full-system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/leistungen/entwicklungsunterstuetzung.html
or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Note

Assembly Options include a choice of Controller, RAM (Size/Type), Size of NAND Flash, interfaces available, vanishing, temperature range, and other features. Please contact our sales team to get more information on the ordering options available.

2.1 Declaration of Electro Magnetic Conformity of the PHYTEC phyFLEX®

CE

PHYTEC System on Modules are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Warning

PHYTEC products lacking protective enclosures are subject to damage by ESD and, therefore, must be unpacked, handled, or operated in environments in which sufficient precautionary measures have been taken with respect to ESD dangers. Only appropriately trained personnel such as qualified electricians, technicians, and engineers should handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity in accordance with the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector, and serial interface to a host-PC).

Tip

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to and certification of Electro Magnetic Directives. Users should ensure conformity following any modifications to a product as well as the implementation of a product into target systems.

2.2 Product Change Management and Information Regarding Parts Populated on the SoM

With the purchase of a PHYTEC SoM / SBC, you will, in addition to our hardware and software possibilities, receive free obsolescence maintenance service for the hardware we provide. Our Product Change Management (PCM) team of developers is continuously processing all incoming Product Change Notifications (PCNs) from vendors and distributors concerning parts that are used in our products. Possible impacts on the functionality of our products due to changes in functionality or obsolesce of certain parts are constantly being evaluated in order to take the right measures either in purchasing decisions or within our hardware/software design.

Our general philosophy here is: **We will never discontinue a product as long as there is a demand for it.**

To fulfill this, we have established a set of methods to fulfill our philosophy:

Avoidance strategies:

- Avoid changes by evaluating the longevity of parts during the design-in phase.
- Ensure the availability of equivalent second source parts.
- Stay in close contact with part vendors to keep up with roadmap strategies.

Change management in the rare event of an obsolete and non-replaceable part:

- Ensure long-term availability by stocking parts through last-time buy management according to product forecasts.
- Offer long-term frame contracts to customers.

Change management in cases of functional changes:

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating for changes through hardware redesign or backward-compatible software maintenance.
- Provide early change notifications concerning functional, relevant changes to our products.

We refrain from providing detailed part-specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.
In order to receive reliable, up-to-date, and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

2.3 PHYTEC Documentation

PHYTEC will provide a variety of hardware and software documentation for all of our products. This includes any or all of the following:

- **Quickstart Guide**: A short guide on how to set up and boot a phyFLEX board along with brief information on building a Board Support Package (BSP), the device tree, and accessing peripherals.
- **Hardware Manual**: A detailed description of the System on Module (SoM) and accompanying carrier board.

- **Yocto Guide**: A comprehensive guide for the Yocto version the phyFLEX uses. This guide contains an overview of Yocto; introducing, installing, and customizing the PHYTEC BSP; how to work with programs like Poky and Bitbake; and much more.
- **BSP Manual**: A manual specific to the BSP version of the phyFLEX. Information such as how to build the BSP, booting, updating software, device tree, and accessing peripherals can be found here.
- **Development Environment Guide**: This guide shows how to work with the Virtual Machine (VM) Host PHYTEC has developed and prepared to run various Development Environments. There are detailed step-by-step instructions for Eclipse and Qt Creator, which are included in the VM. There are instructions for running demo projects for these programs on a phyFLEX product as well. Information on how to build a Linux host PC yourself is also a part of this guide.
- **Pin Muxing Table**: phyFLEX SoMs have an accompanying pin table (in Excel format). This table will show the complete default signal path, from processor to carrier board. The default device tree muxing option will also be included. This gives a developer all the information needed in one location to make muxing changes and design options when developing a specialized carrier board or adapting a PHYTEC phyFLEX SOM to an application.

On top of these standard manuals and guides, PHYTEC will also provide Product Change Notifications, Application Notes, and Technical Notes. These will be done on a case-by-case basis. Most of the documentation can be found on the applicable download page of our products.

> **Tip**
>
> After finishing the Quickstart Guide, we recommend working through the Development Environment Guide. This will give you a comprehensive overview of the features and functions of both the SoM and carrier board.

These manuals and more can be found in the download section of phyFLEX-i.MX 95 Product page.

3 Conversions, Abbreviations, and Acronyms

Tip

Due to part maintenance for our products (which are subject to continuous changes), we refrain from providing detailed, part-specific information within this manual. Please read the section Product Change Management and Information Regarding Parts Populated on the SOM / SBC within the Preface for more information.

Tip

The BSP delivered with the phyFLEX-i.MX 95 usually includes drivers and/or software for controlling all components, such as interfaces, memory, etc. Programming close to hardware at the register level is not necessary in most cases. For this reason, this manual does not contain detailed descriptions of the controller's registers or information relevant to software development. Please refer to the i.MX 95 Reference Manual, if any information is not found in this manual, it is needed to connect customer-designed applications.

3.1 Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or “#” character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: RD), are designated as active low signals. That is, their active state is when they are driven low or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB, which depends on the desired command (read (1) or write (0)), must be added to get the complete address byte. For example, if the given address in this manual is 0x41 =>, the complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables that describe all settings show the default position in **bold, blue text**.

3.2 Types of Signals

Different types of signals are brought out at the phyFLEX-Connector. The following table lists the abbreviations used to specify the type of signal.

Signal Type	Description	Abbreviation
Power In	Supply voltage input	PWR_I
Power Out	Supply voltage output	PWR_O
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
I/O	Bidirectional input/push-pull output	I/O
Input/OD-Output	Input / open-drain output requires an external pull-up	I/OD
OC-Bidir PU	Open collector input/output with pull-up	OC-BI-PU
OC-Output	Open collector output without a pull-up requires an external pull-up	OC
OD-Bidir PU	Open-drain input/output with pull-up	OD-BI-PU
OD-Output	Open-drain output without a pull-up requires an external pull-up	OD
5 V Input PD	5 V tolerant input with pull-down	5V-PD
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 100 Ohm PCIe level input	PCIe_I
PCIe Output	Differential line pairs 100 Ohm PCIe level output	PCIe_O

Signal Type	Description	Abbreviation
PCIe IO	Differential line pairs 100 Ohm PCIe level input or output	PCIe_I/O
HDMI Input	Differential line pairs 100 Ohm HDMI level input	HDMI_I
HDMI Output	Differential line pairs 100 Ohm HDMI level output	HDMI_O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI2_I
MIPI DSI-2 Output	Differential line pairs 100 Ohm MIPI DSI-2 level output	DSI2_O
CAN FD IO	Differential line pairs 120 Ohm CAN FD level bidirectional input/output	CAN_I/O

TABLE 1: Signal Types

3.3 Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the following table to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BGA	Ball Grid Array
BSP	Board Support Package (software delivered with the Development Kit, including an operating system (Windows or Linux) preinstalled on the module and development tools)
CB	Carrier board; used in reference to the phyFLEX development kit carrier board
EMI	Electromagnetic Interference
GPI	General-purpose input
GPIO	General-purpose input and output
GPO	General-purpose output
FPSC	Future Proofed Soldering Core
IRAM	Internal RAM: the internal static RAM on the NXP® Semiconductor i.MX 95 microcontroller
J	Solder jumpers: these types of jumpers require solder equipment to remove and place
JP	Solderless jumpers: these types of jumpers can be removed and placed by hand with no special tools
OEM	Original Equipment Manufacturer
PCB	Printed circuit board
PCM	Product Change Management
PCN	Product Change Notification
PMIC	Power management IC
RTC	Real-time clock

Abbreviation	Definition
SBC	Single Board Computer
SMT	Surface mount technology
SOM	System on Module; used in reference to the PFL-G-02 /phyFLEX®-i.MX 95 module
Sx	User button Sx (e.g., S1, S2, etc.) used in reference to the available user buttons or DIP-Switches on the carrier board
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board
VM	Virtual Machine

TABLE 2: Abbreviations and Acronyms Used in this Manual

4 phyFLEX-i.MX 95 FPSC Introduction

The phyFLEX-i.MX 95 belongs to PHYTEC's phyFLEX System on Module family. The phyFLEX SOMs represent the continuous development of the PHYTEC System on Module technology. Like its mini-, micro-, and nanoMODUL predecessors, phyFLEX boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

Independent research indicates that approximately 70 % of all EMI (Electromagnetic interference) problems are caused by insufficient supply voltage grounding of electronic components in high-frequency environments. The phyFLEX board design features an increased pin package, which allows for the dedication of approximately 20 % of all connector pins on the phyFLEX boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyFLEX boards, even in high-noise environments.

phyFLEX boards achieve their small size through modern SMT and multi-layer design. Due to the complexity of our modules, 0201-packaged SMT components and laser-drilled microvias are used on the boards, providing phyFLEX users with access to this cutting-edge miniaturization technology for integration into their own design.

The phyFLEX-i.MX 95 is a subminiature (48 mm x 45 mm) insert-ready System on Module populated with the NXP® Semiconductor i.MX 95 microcontroller. Its universal design enables it to be inserted into a wide range of embedded applications. All controller signals and ports extend from the controller to surface mount technology (**FPSC FTGA 1.27 mm grid**) connectors, aligning four sides of the board, allowing it to be soldered into any target application like a "big chip".

The descriptions in this manual are based on the NXP® Semiconductor i.MX 95. Descriptions of compatible microcontroller derivative functions are not included, as such functions are not relevant for the basic functioning of the phyFLEX-i.MX 95.

4.1 phyFLEX-i.MX 95 FPSC Features

The phyFLEX-i.MX 95 FPSC offers the following features:

- Insert-ready, sub-miniature (48 mm x 45 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Mounted using FTGA Direct Solder Connector (FPSC FTGA)
- Populated with the NXP® Semiconductor i.MX 95 microcontroller (19mmx19mm BGA716 packaging)
- Up to 6 ARM-A55 cores (clock frequency up to 2.0 GHz)
- Machine Learning Neuronal Processing eIQ Neutron NPU mit 2 TOP/s
- 1x Cortex M7 core (800 MHz)
- 1x Cortex M33 core (333 MHz)
- Arm Mali-G310 Graphic Processing Unit (GPU), 3D GPU supporting 64 GFLOPs FP32, OpenGL® ES 3.2, Vulkan® 1.3, OpenCL 3.0, 4Kp60 H.265 and H.264 encode and decode
- Image Signal Processor (up to 500 MP/s)
- Boot from different memory devices (eMMC Flash standard)
- Single supply voltage of +5 V with on-board power management
- IO voltage between 1.8 V (default) and 3.3 V (factory assembly option)
- All controller-required supplies are generated on-board using sophisticated on-board Power Management
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- up to 16 GB[1] LPDDR5 RAM (MTS6400)
- up to 128 GB[1] on-board eMMC
- 4kB[1] I^2C User-EEPROM and 4kB I^2C Factory-EEPROM
- 1x USB 3.0/2.0 Type C with PHY, 1x USB 2.0 with PHY

- 2x 1Gbit Ethernet interfaces with TSN support (either one of them with Ethernet transceiver on the phyFLEX-i.MX 95 enabling a direct connection to an existing Ethernet network; the second as RGMII Signals at logic-level at the signal pins instead)
- 1x 10G Ethernet interface with TSN support (USXGMII)
- up to 8x I^2C interfaces / 2x I^3C interfaces
- up to 8x SPI interfaces
- 2x PCIe Gen 3.0 (1-lane)
- up to 8x UART interfaces
- up to 5x CAN-FD interfaces
- up to 6x Timer/PWM outputs
- 1x MIPI CSI-2/DSI-2 camera/display interface
- 1x MIPI CSI-2 camera interfaces
- 1x LVDS Tx interface 2 channels x4
- 1x 8-bit uSDHC for eMMC
- 1x 4-bit SD-Card interface
- 1x 4-bit SDIO interface
- Up to 5x SAI audio interfaces
- 1x SPDIF interface
- Extreme Low Power RTC Module
- 4x temperature sensors to monitor the board's temperature profile
- All processor interfaces available at the SOM Connector
- Available for different temperature grades (see Product Temperature Grades)

[1] The maximum memory size is listed as of the printing of this manual.
Please contact PHYTEC for more information about additional or new module configurations available.

Due to multiplexing, not all interfaces may be fully available.

4.2 phyFLEX-i.MX 95 FPSC Block Diagram

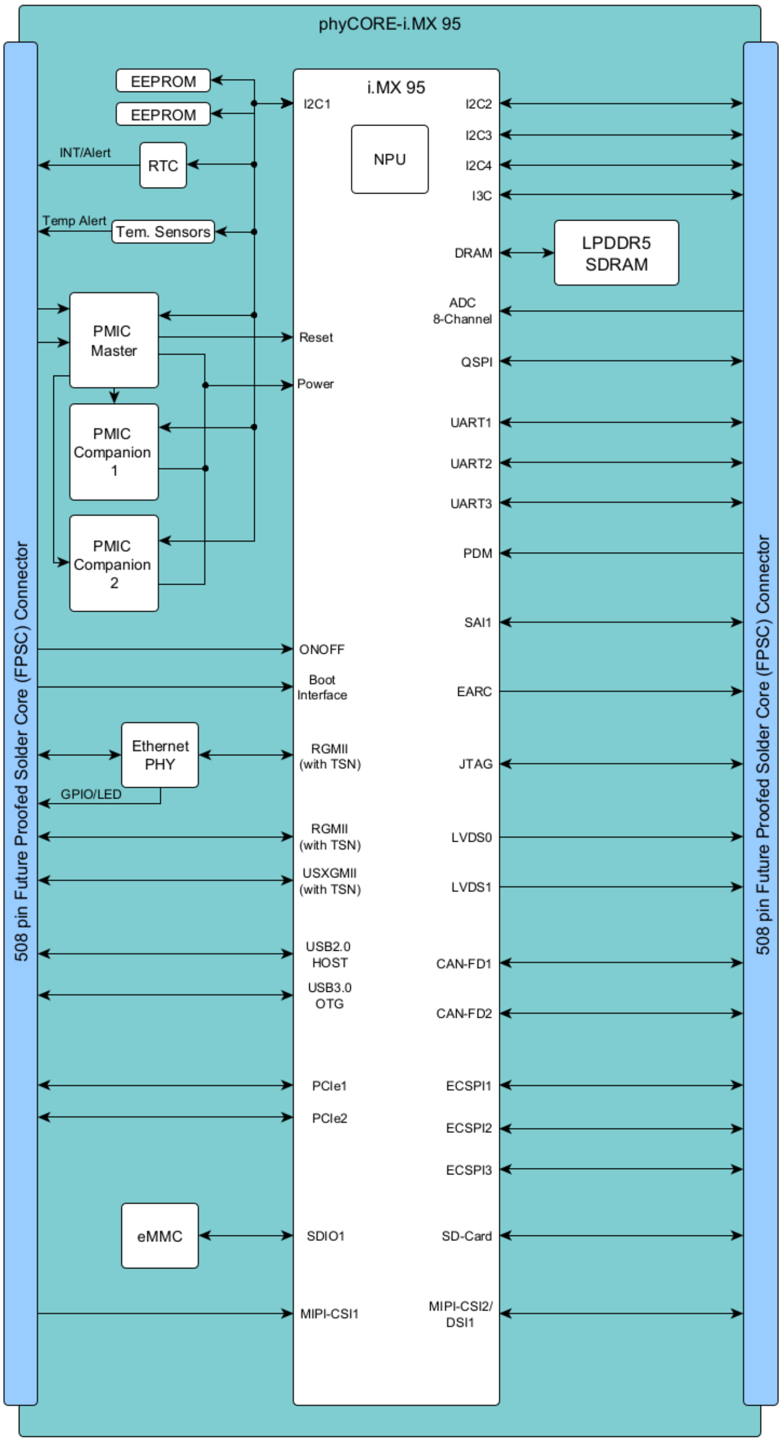


FIGURE 1: phyFLEX-i.MX 95 Block Diagram

4.3 phyFLEX-i.MX 95 FPSC Component Placement

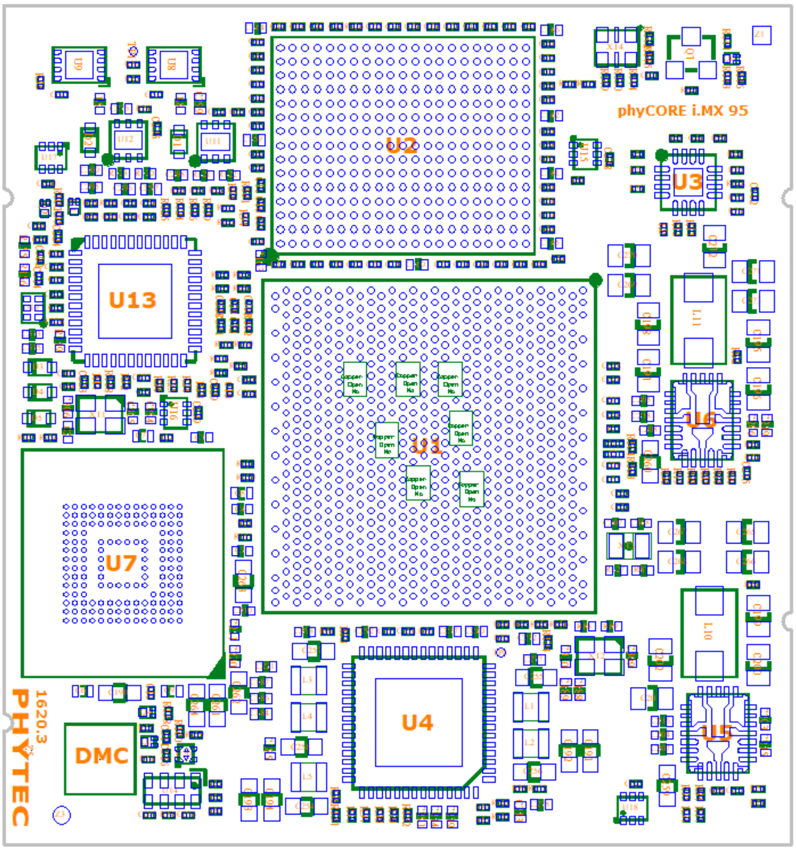


FIGURE 2: phyFLEX-i.MX 95 Component Placement (1620.3 Top View)

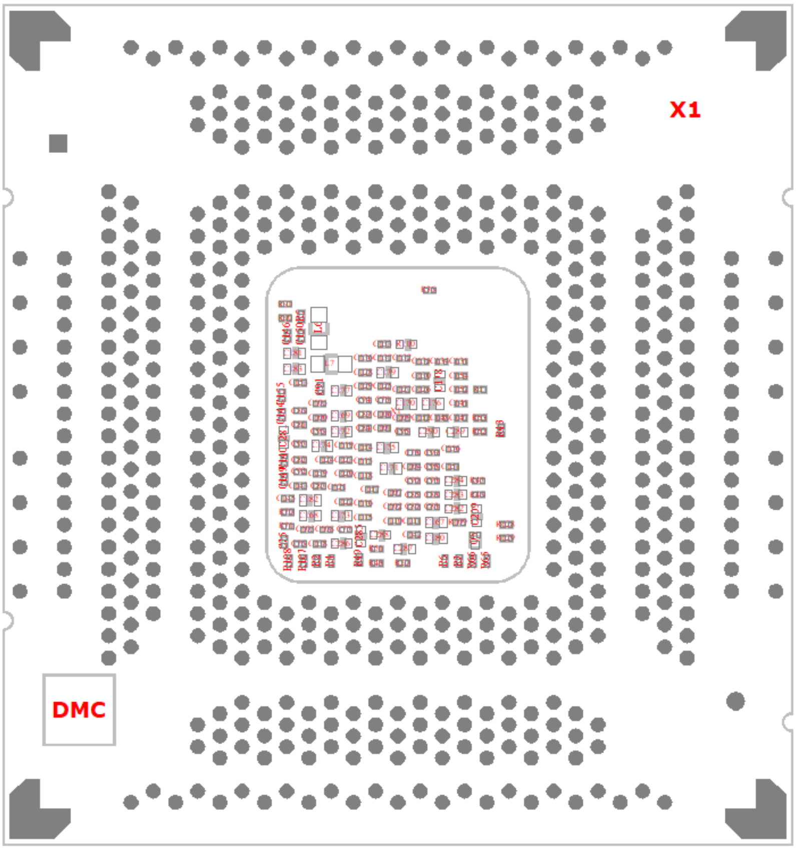


FIGURE 3: phyFLEX-i.MX 95 Component Placement (1620.3 Bottom View)

4.4 phyFLEX-i.MX 95 FPSC Minimum Operating Requirements

Warning

We recommend connecting all available VIN (+5.0 V) input contacts to the power supply system on a custom carrier board housing the phyFLEX-i.MX 95 FPSC. In addition, proper implementation of the phyFLEX-i.MX 95 FPSC module into a target application also requires connecting all GND contacts. Refer to Power for more information.

Before the phyFLEX-i.MX 95 FPSC can be used; please make sure the host system meets the minimum operating requirements. These include:

- The stable and clean input power supply of 5.0 V with low ESR bulk capacitors (e.g. 2x 47µ/16V MLCC) paired with some HF blocking capacitors (e.g. 100nF MLCC) connected to the input pins as near as possible (phyFLEX-i.MX 95 Power Consumption)
- Supply voltage for externally connected peripherals should be controlled by signal X_nPWR_READY to avoid reverse currents (External Logic IO Supply Voltage)
- If external peripherals need a longer reset delay, hold the reset signal X_POR_B as long low as needed (Reset)
- Desired boot configuration - default configuration is "Boot from on-board eMMC" (System Boot Configuration)
- To back up the on-board I^2C-RTC, connect a buffer voltage source to input pin X_RTC_VBACKUP (Backup Power (X_RTC_VBACKUP), RTC)

5 Pin Description

> **Warning**
>
> Module connections **must** not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/datasheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to the FPSC footprint. These contacts line four sides of the module (referred to as the FPSC footprint). This enables phyFLEX-i.MX 95 to be plugged into any target application like a "big chip".

PHYTEC provides a complete pinout table for the phyFLEX-i.MX 95 Connector (X1). This table contains a complete signal path for the phyFLEX-i.MX 95 and the Libra Development Board, including signal names, pin muxing paths, and descriptions specific to each pin. It also provides the appropriate voltage domain, signal type (ST), and a functional grouping of the signals. The signal type also includes information about the signal direction. A table describing the signal types can be found with the phyFLEX-i.MX 95 Pinout Table.

> **Warning**
>
> - The NXP® Semiconductor i.MX 95 is a multi-voltage-operated microcontroller, and, as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *NXP Semiconductor i.MX 95 Reference Manual* for details on the functions and features of controller signals and port pins.
> - As some of the signals that are brought out on the phyFLEX-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals that may affect the boot configuration are shown in phyFLEX-Connector Boot Configuration Pins.
> - It is necessary to avoid voltages at the IO pins of the phyFLEX-i.MX 95 FPSC, which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up or power-down. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the i.MX 95 are supposed to be powered while the phyFLEX-i.MX 95 FPSC is in suspend mode or turned off. To avoid this, bus switches are either supplied by VDD_1V8 on the phyFLEX side or have their output enabled to the SOM controlled by the X_nPWR_READY signal (see Supply Voltage for External Logic).

> **Pin Muxing Warning**
>
> If pin settings are changed from the PHYTEC standard configuration, make sure that the settings of the pull resistors are adjusted accordingly. Never rely on the SoC-internal pull resistor.

6 Jumpers

The phyFLEX-i.MX 95 FPSC (PFL-G-02) is jumperless. There are, however, a few jumpers on the Libra Development Board. Information on these jumpers can be found in Jumpers.

Warning

Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Contact our sales team if you need jumper configurations different from the default configuration.

7 Power

The phyFLEX-i.MX 95 FPSC operates off a single power supply voltage. The following section discusses the primary power pins on the phyFLEX i.MX 95 FPSC Connector X1 in detail.

7.1 Primary System Power (VIN_5V)

The phyFLEX-i.MX 95 FPSC is powered by a primary voltage supply with a nominal value of +5.0 V. On-board switching regulators generate the voltage supplies required by the i.MX 95 MCU and on-board components from the primary 5.0 V are supplied to the SOM.

For proper operation, the phyFLEX-i.MX 95 FPSC must be supplied with a voltage source of 4.75 ... 5.25 V with a maximum power consumption of a 4 A load at the VIN_5V pins on the phyFLEX.

FPSC Contact	FPSC Signal	SOM Signal Name	Signal Type	Description
L24, M25, N24, L22, N22, M21, N20, P21	VCC_IN	VIN_5V	PWR_I	5 V ± 5% Power supply input of the module.
AA74, AA8, AB13, AB23, AB59, AB69, AD13, AD23, AD59, AD69, AD7, AD75, AF13, AF23, AF59, AF69, AG74, AG8, AH13, AH23, AH27, AH31, AH35, AH39, AH43, AH47, AH51, AH55, AH59, AH69, AK7, AK75, AM23, AM27, AM31, AM35, AM39, AM43, AM47, AM51, AM55, AM59, AR30, AR36, AR46, AR52, AU26, AU30, AU34, AU38, AU44, AU48, AU52, AU56, C26, C30, C34, C38, C44, C48, C52, C56, E30, E36, E46, E52, H23, H27, H31, H35, H39, H43, H47, H51, H55, H59, K7, K75, M13, M23, M27, M31, M35, M39, M43, M47, M51, M55, M59, M69, N74, N8, P13, P23, P59, P69, T13, T23, T59, T69, T7, T75, V13, V23, V59, V69, W74, W8, Y13, Y23, Y59, Y69	0V GND	GND	GND	Power and signal ground reference.

FPSC Contact	FPSC Signal	SOM Signal Name	Signal Type	Description
1, 2, 3, 4 (Corner GND)	0V GND	GND	GND	Mechanical fixing, power, and signal ground reference.

TABLE 3: Primary System Power

Please refer to the section Pin Description for information on additional GND Pins located at the phyFLEX i.MX 95 Connector X1.

For information on various power consumption scenarios that PHYTEC has run, go to phyFLEX-i.MX 95 FPSC Power Consumption.

Warning

As a general design rule, PHYTEC recommends connecting all GND pins to neighboring signals that are being used in the application circuitry. For maximum EMI performance, all GND pins should be connected to a solid ground plane. Additionally, take care of a solid, low impedance connection of the power supply line to avoid voltage drop. It is recommended to place a couple of bulk capacitors as near as possible to the phyFLEX's system power input (VIN_5V) to compensate for the trace inductance.

7.2 Power Management IC (PMIC) (U4/U5/U6)

The phyFLEX-i.MX 95 FPSC provides an on-board Power Management IC (PMIC) at position U4 and two slave regulators U5/U6 (VDD_ARM/VDD_SOC) to generate different voltages required by the microcontroller and the on-board components. The PMIC supports many functions, different power management functionalities like dynamic voltage control, different low-power modes, and regulator supervision. It is connected to the i.MX 95 via the on-board I^2C bus (I^2C2). The I^2C address of the PMIC U4 is 0x08. The slave regulator U5 has an I^2C bus address of 0x2A, and U6 has 0x29.

7.3 Power Domains

External voltages to supply the board:

- VIN_5V 5.0 V main supply voltage (4.75 .. 5.25 V / max. 4A)
- X_RTC_VBACKUP backup supply voltage for the on-board I^2C-Bus RTC U14 (RV-3028-C7)

7.4 External Logic IO Supply Voltage

The voltage level of the phyFLEX's logic interface circuitry is VDD_1V8 (1.8 V).

The power-up and power-down sequencing is mandatory for the i.MX 95. External devices connected to the phyFLEX interface circuitry have to be supplied by an external power supply, which is controlled by the output signal X_nPWR_READY (OD driver), which is brought out at pin X1-U22. X_nPWR_READY should control the external supply voltage, which is used to supply the external interface circuitry connected to the phyFLEX's interfaces. X_nPWR_READY switches to GND to start the external voltage supply or to switch over a power switch. If the on-board interface voltage switches off, X_nPWR_READY is released to high impedance. To raise the signal, an external pull-up resistor (eg, 4k7) is needed. It can be connected to voltage levels up to 10V (the Transistor DMN1260UFA has an absolute max. of 12V), depending on the external power supply control signal requirement. Use of X_nPWR_READY ensures that external components are only supplied when the supply voltages of the i.MX 95 is stable and avoids undefined return currents while the system is powered down.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
Y25	Specialized	-	-	-	-	-
U22	nPWRREADY_OUT	X_nPWR_READY	-	abs. max 12 V	OD	Needs an external PU-Resistor (abs. max. 12 V). Use it to control the power sequencing of your baseboard.

TABLE 4: X_nPWR_READY (OD driver)

> **Warning**
>
> PHYTEC recommends monitoring the externally generated power supply voltages using a voltage supervisor.

7.5 Backup Power (X_RTC_VBACKUP)

To back up the on-board I^2C-Bus RTC U14 (RV-3028-C7), an external voltage source must be added at Pin X1-AC7 (X_RTC_VBACKUP). The RTC has an extremely low backup current consumption of only 40nA (@3 V).

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AA22	VCC_RTC	X_RTC_VBACKUP	-	nom. 3.3 V (max. range 1.1 V to 5.5 V)	PWR_I	Connect a gold cap or a battery here. If a battery is used, make sure that the RTC trickle charger is deactivated!

TABLE 5: X_RTC_VBACKUP

7.6 Manual Power Switch (X_OnOff)

The signal X_OnOff (Pin X1-R20) is used to manually switch the power of the SOM. X_OnOff signal can be left unconnected if not used. It has a weak on-board pull-up resistor against 1.8 V (VDD_VAON) and is held high as long as VIN_5V is present. To drive the signal to GND, use an open collector driver or push button. For more information about ON/OFF, refer to the *NXP Semiconductor i.MX 95 Reference Manual*.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
R20	ON/OFF	X_OnOff (F40)	VDD_VAON	1.8 V	I	Wake up and power off the Processor. Intended to connect a push-button or an open-collector driver.

TABLE 6: X_OnOff

8 Reset

The X_nRESET_IN signal (Pin X1-Y21) on the phyFLEX-Connector is designated as a "cold reset" input. Driving X_nRESET_IN to low (has 10k pull-up to VIN_5V) will restart the system, performing a complete power recycle. Holding X_nRESET_IN low will force the system reset and hold it in the reset state. This input can be used for a mechanical reset switch button.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P15	Specialized	X_WDOG_ANY (J45)	NVCC_AON	1.8 V	OD	X_WDOG_ANY is connected to X_FCCU1 via R132 and is used to trigger a cold reset.
Y21	nRESET_IN	X_nRESET_IN	VIN_5V	5.0 V (module input supply voltage)	OD_IN	X_nRESET_IN acts as a cold reset input. Driving X_nRESET_IN to low (has 10k pull-up to VIN_5V) will restart the system, performing a complete power recycle triggert from the falling edge of the signal. Holding X_nRESET_IN low will force the system reset and hold it in the reset state. This input can be used for a mechanical reset switch button.
R22	nRESET_OUT	X_POR_B	VDD_VAON	1.8 V	OD	This pin is internally connected to the processor and the PMIC. Connect it to the reset input of your baseboard peripherals. X_POR_B has a 10k pull-up resistor to 1.8 V.

TABLE 7: X_FCCU1

9 System Boot Configuration

Most features of the i.MX 95 microcontrollers are configured and/or programmed during the initialization routine. Other features that impact program execution must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Boot mode selection
- Boot device selection
- Boot device configuration

The internal ROM code is the first code executed during the initialization process of the i.MX 95 after POR. The ROM code detects the boot mode by using the boot mode pins (BOOT_MODE[3:0]), while the boot device is selected and configured by determining the state of the eFUSEs and/or the corresponding GPIO input pins (X_BOOT_MODE[3:0]).

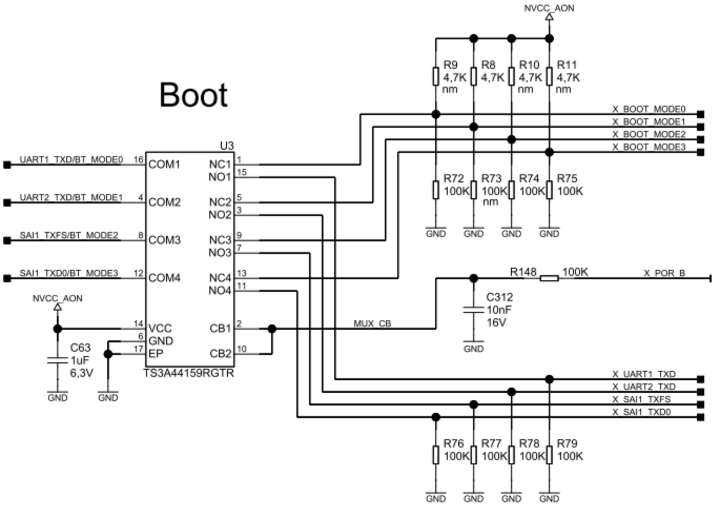
9.1 Boot Mode Selection

The boot mode of the i.MX 95 microcontroller is determined by the configuration of four boot mode inputs BOOT_MODE[3:0], during the reset cycle of the operational system. These inputs are brought out at the phyFLEX processor pins X_BOOT_MODE[3:0] ((X1-AA7, X1-AA6, X1-AA5, X1-AA4). phyFLEX-i.MX 95 Boot Modes show the possible settings of pins X_BOOT_MODE[3:0] and the resulting boot configuration of the i.MX 95.

Boot Mode	X_BOOT_MODE3	X_BOOT_MODE2	X_BOOT_MODE1	X_BOOT_MODE0	Boot Source
	0/**1**				0: A55 core **1: M33 core (default)**
1	0/1	0	0	1	USB1 serial download
2	**0/1**	**0**	**1**	**0**	**Boot from onboard eMMC (default)**
3	0/1	0	1	1	Boot from the external SD card on SD2
4	0/1	1	0	0	Boot FlexSPI serial NOR

TABLE 8: phyFLEX-i.MX 95 FPSC Boot Modes

The X_BOOT_MODE[3,2,0] lines have 100 kΩ pull-down resistors populated (and unpopulated pull-up resistors) while X_BOOT_MODE[1] has a 4,7 kΩ pull-up resistor on the module in parallel to the internal pull-down resistors of the i.MX 95. Leaving the four pins unconnected sets the controller to boot mode 2, boot from the on-board eMMC U7 memory device. The boot configuration settings can be changed by changing the populated resistors configuration on the module or by connecting configuration resistors (e.g., 4,7 kΩ pull-up) to the X_BOOT_MODE configuration signals. The pull-up resistors must be supplied by the right voltage level (default NVCC_AON=1.8 V, see section External Logic IO Supply Voltage).



No.	X_BOOT_MODE[3..0]	Boot Modes
	(0XXX)	(Cortex-A55 boot)
	1XXX	Cortex-M33 boot (rev A1 A55)
1	X001	USB1 serial download
2	X010	Boot from onboard eMMC (default)
3	X011	Boot from ext. SD-Card on SD2
4	X100	Boot from onboard SPI Flash

FIGURE 4: phyFLEX-i.MX 95 FPSC Onboard Boot Configuration Schematic

The BOOT_MODE is initialized by sampling the BOOT_MODE inputs on the rising edge of the POR_B. After these inputs are sampled, their subsequent state does not affect the contents of the BOOT_MODE internal register. X_BOOT_MODE module input signals are connected only during the reset phase to the processor inputs. For runtime, the X_UART and X_SAI1 signals are routed through the MUX U3.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P25	BOOT_MODE1	X_BOOT_MODE0 (MUX->F52)	NVCC_AON	1.8 V	I	Boot configuration pin 0 during reset has on-board 100k pull-down resistor (SMD 0201)
R24	BOOT_MODE2	X_BOOT_MODE1 (MUX->F48)	NVCC_AON	1.8 V	I	Boot configuration pin 1 during reset has on-board 4,7 k pull-down resistor (SMD 0201)
T25	BOOT_MODE3	X_BOOT_MODE2 (MUX->G49)	NVCC_AON	1.8 V	I	Boot configuration pin 2 during reset has an on-board 100k pull-down resistor (SMD 0201)
U24	BOOT_MODE4	X_BOOT_MODE3 (MUX->H48)	NVCC_AON	1.8 V	I	Boot configuration pin 3 during reset has on-board 100k pull-down resistor (SMD 0201)

TABLE 9: phyFLEX-i.MX 95 FPSC Boot Configuration Pins

10 System Memory

The phyFLEX-i.MX 95 FPSC provides four types of on-board memory:

	Basic-Version	Kit-Version	Exclusive-Version	Maximum Available
LPDDR5 RAM	4 GByte	8 GByte	16 GByte	16 GByte
eMMC	8 GByte	32 GByte	128 GByte	256 GByte
I^2C User EEPROM	4 kB	4 kB	4 kB	32 kB
I^2C Factory EEPROM [2]	4 kB	4 kB	4 kB	32 kB

TABLE 10: phyFLEX-i.MX 95 FPSC Onboard Memory Types

2. Factory EEPROM should not be used by the application. It contains module-specific information to identify the module during factory handling and testing.

10.1 LPDDR5-RAM (U2)

The RAM interface of the phyFLEX-i.MX 95 FPSC supports one 32-bit LPDDR5-RAM chip (U2). The memory interface supports MTS6400 transfer speed.

Typically, the LPDDR5-RAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, the RAM must be initialized by accessing the appropriate RAM configuration registers on the i.MX 95 controller. Refer to the *NXP Semiconductor i.MX 95 Reference Manual* to access and configure these registers.

10.2 eMMC Flash Memory (U7)

The main flash memory of the i.MX 95 is eMMC and is populated at U7. The eMMC Flash memory is connected to the SD1 interface of the i.MX 95.

For more information about the eMMC Flash interface, please refer to the *NXP Semiconductor i.MX 95 Reference Manual*.

10.3 I^{2}C Factory EEPROM (U8)

The phyFLEX-i.MX 95 FPSC is populated with a non-volatile 4 kB I^{2}C EEPROM at U8. This memory can be used to store configuration data or other general-purpose data. This device is accessed through I^{2}C port 1 on the i.MX 95. Please see the *NXP Semiconductor i.MX 95 Reference Manual* for detailed information on the I^{2}C port 1.

The three lower address bits are fixed to 0x1, which means that the EEPROM can be accessed at I^{2}C address 0x51. The EEPROM has a second address on 0x59, which is called the Identification Page and is reserved for internal PHYTEC use only.

The device is write-protected by default. Write protection can be deactivated by driving the signal X_EEPROM1_WC (X1-DE21) to GND. The signal has a 10k pull-up resistor to VDD_IO (default 1.8 V).

10.4 I^{2}C User EEPROM (U9)

The phyFLEX-i.MX 95 FPSC is populated with a non-volatile 4 kB I^{2}C EEPROM at U9. This memory is free for use. This device is accessed through I^{2}C port 1 on the i.MX 95. Please see the *NXP Semiconductor i.MX 95 Reference Manual* for detailed information on the I^{2}C port 1.

The three lower address bits are fixed to 0x,0, which means that the EEPROM can be accessed at I^{2}C address 0x50. The EEPROM has a second address on 0x58, which is called the Identification Page.

The device is not write-protected by default. Write protection can be established by driving the signal X_EEPROM2_WC (X1-DF20) to VDD_IO (default 1.8 V). The signal has a 10k pull-down resistor.

11 Serial Interfaces

The phyFLEX-i.MX 95 FPSC provides numerous dedicated serial interfaces, some of which are equipped with a transceiver to enable direct connection to external devices:

1. 1x 4-bit SDIO interface (SD2) with controlled IO voltage for µSD card.
2. 1x 4-bit SDIO interface (SD3)
3. 3x high-speed UARTs
4. 2x CAN-FD interfaces
5. 1x USB 3.0/2.0 Dual-Role interfaces with PHY
6. 1x USB 2.0 Dual-Role interfaces with PHY
7. 2x 1Gbit Ethernet interfaces with TSN support (ENET2 with Ethernet transceiver on the phyFLEX-i.MX 95 FPSC enabling a direct connection to an existing Ethernet network; ENET1 as RGMII Signals at logic-level at the signal pins instead)
8. 5x I^2C interfaces
9. 2x Serial Peripheral Interfaces (SPI)
10. 1x SAI audio interface
11. 2x PCI Express with x1 interface
12. 1x MIPI CSI-2 camera interfaces
13. 1x MIPI CSI-2/DSI-2 display interface

Details for each of these serial interfaces and any applicable jumper configurations are below.

11.1 SDIO Interface

The SDIO interface can be used to connect external SD cards, eMMC, or any other device requiring an SDIO interface (i.e, WiFI, I/O expansion, etc.) The phyFLEX bus features one SDIO interface. On the phyFLEX-i.MX 95 FPSC, the interface signals extend from the second and third Ultra Secured Digital (SD2 and SD3) Host controller to the phyFLEX-Connector.

The tables below show the location of the different interface signals on the phyFLEX-Connector. The MMC/SD/SDIO Host Controller is fully compatible with the SD Memory Card Specification 3.0. The interface SD2 supports SD cards with 3.3 V and 1.8 V I/O signals.

11.2 SDIO SD2 (4-bit)

SDIO SD2 is a 4-bit wide interface with controlled I/O voltage to support high-speed modes that require 1.8 V I/O voltage. During runtime, the I/O voltage can be switched from 3.3 V (default) to 1.8 V by the processor, which controls the PMIC integrated voltage regulator. X_VDDSW_SD2 will be used exclusively to supply an external SD or MicroSD memory card. X_VDDSW_SD2 is monitored by the PMIC for overcurrent and short circuits. For more details, please refer to the PMIC data sheet provided by NXP.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
Y57	SDCARD_VCC_OUT	X_VDDSW_SD2	X_VDDSW_SD2	3.3 V	PWR_O	Controlled SD Card Supply Voltage
V57	SDCARD_CD	X_SD2_CD_B (AD48)	NVCC_SD2	1.8 V / 3.3 V	I	SD2 Card Detect
V67	SDCARD_WP	-	-	-	-	-
W58	SDCARD_CMD	X_SD2_CMD (AB52)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Command
W60	SDCARD_CLK	X_SD2_CLK (AB48)	NVCC_SD2	1.8 V / 3.3 V	O	SD2 Clock
W62	SDCARD_DATA0	X_SD2_DATA0 (AC51)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 0
Y61	SDCARD_DATA1	X_SD2_DATA1 (AC49)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 1
U60	SDCARD_DATA2	X_SD2_DATA2 (AA51)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 2
V61	SDCARD_DATA3	X_SD2_DATA3 (AA49)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 3

TABLE 11: SDIO Interface Pinout of SD2

11.3 SDIO SD3 (4-bit)

SDIO SD3 is a 4-bit wide interface. The default I/O voltage is 1.8 V (refer to External Logic IO Supply Voltage).

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
G56	SDIO_CMD	X_SD3_CMD (AF48)	NVCC_WAKEUP	1.8 V	I/O	SD3 Command
H57	SDIO_CLK	X_SD3_CLK (AG51)	NVCC_WAKEUP	1.8 V	O	SD3 Clock
G62	SDIO_DATA0	X_SD3_DATA0 (AG49)	NVCC_WAKEUP	1.8 V	I/O	SD3 Data 0
H61	SDIO_DATA1	X_SD3_DATA1 (AH52)	NVCC_WAKEUP	1.8 V	I/O	SD3 Data 1
G60	SDIO_DATA2	X_SD3_DATA2 (AE49)	NVCC_WAKEUP	1.8 V	I/O	SD3 Data 2
G58	SDIO_DATA3	X_SD3_DATA3 (AE51)	NVCC_WAKEUP	1.8 V	I/O	SD3 Data 3
G54	SDIO_WP	-	-	-	-	-
J58	SDIO_CD	-	-	-	-	-
J56	SDIO_VIO_OUT	NVCC_WAKEUP	NVCC_WAKEUP	1.8 V	PWR_O	Voltage output (max. 20mA) to supply VDD_IO of the connected device

TABLE 12: SDIO Interface Pinout of SD3

11.4 Universal Asynchronous Interfaces (UARTs)

The phyFLEX-i.MX 95 FPSC provides four high-speed universal asynchronous interfaces. The following table shows the location of the signals on the phyFLEX-Connector.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L44	UART1_RXD	X_GPIO_IO13 (N49)	VDD_1V8	1.8 V	I	LPUART8_RX
L42	UART1_TXD	X_GPIO_IO12 (N45)	VDD_1V8	1.8 V	O	LPUART8_TX
N42	UART1_RTS	X_GPIO_IO15 (P44)	VDD_1V8	1.8 V	O	LPUART8_RTS
M41	UART1_CTS	X_GPIO_IO14 (N51)	VDD_1V8	1.8 V	I	LPUART8_CTS
N46	UART2_RXD	X_GPIO_IO01 (J51)	VDD_1V8	1.8 V	I	LPUART5_RX (Usually used as M7 Debug)
N44	UART2_TXD	X_GPIO_IO00 (J49)	VDD_1V8	1.8 V	O	LPUART5_TX (Usually used as M7 Debug)
M45	UART2_RTS	X_GPIO_IO03 (K52)	VDD_1V8	1.8 V	O	LPUART5_RTS
L46	UART2_CTS	X_GPIO_IO02 (K48)	VDD_1V8	1.8 V	I	LPUART5_CTS

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AE22	UART3_RXD	X_GPIO_IO37 (Y52)	VDD_1V8	1.8 V	I	LPUART7_RX (Usually used as A55 Debug)
AE20	UART3_TXD	X_GPIO_IO36 (Y48)	VDD_1V8	1.8 V	O	LPUART7_TX (Usually used as A55 Debug)

TABLE 13: UART Signal Locations

11.5 CAN Interfaces

The CAN-FD interfaces of the phyFLEX-i.MX 95 FPSC is connected to the FLEXCAN modules (FLEXCAN1/FLEXCAN2) of the i.MX 95, which is a full implementation of the CAN FD protocol specification version 2.0B. It supports a flexible message payload, ranging from 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes. It also supports standard and extended message frames and programmable bit rates of 2, 5, and 8 Mb/s.

The following table shows the position of the signals on the phyFLEX-Connector.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
N38	CAN1_RX	X_PDM_BIT_STREAM0 (G45)	VDD_1V8	1.8 V	I	FLEXCAN1 RX
N36	CAN1_TX	X_PDM_CLK (F46)	VDD_1V8	1.8 V	O	FLEXCAN1 TX
L38	CAN2_RX	X_GPIO_IO27 (U49)	VDD_1V8	1.8 V	I	FLEXCAN2 RX
M37	CAN2_TX	X_GPIO_IO25 (T52)	VDD_1V8	1.8 V	O	FLEXCAN2 TX

TABLE 14: CAN Interface Signal Location

11.6 USB Interfaces

The phyFLEX-i.MX 95 provides one USB 3.0/2.0 and one USB 2.0 dual-role interface. The USB 3.0 supports super-speed (5Bbit/s) with two sets of SuperSpeed SerDes lanes with automatic identification by the Type-C assist system. USB 2.0 supports high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operation. The applicable interface signals can be found on the phyFLEX-Connector X1. If overcurrent and power enable signals are needed for the USB host interface, the functionality can be easily implemented with GPIOs.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AC60	USB1_VBUS	X_USB1_VBUS (via 30k resistor to E23)	VDD_3V3	3.3 V / 5 V	I	USB 1 bus voltage detection (5 V compliant)
AE60	USB1_ID	X_USB1_ID (C23)	VDD_1V8	1.8 V	I	Currently has no function due to being a dedicated CPU pin. Use GPIO to implement OTG if needed.
AD61	USB1_D_N	X_USB1_D_N (B18)	VDD_3V3	-	USB_I/O	USB 1 Data-
AD62	USB1_D_P	X_USB1_D_P (C19)	VDD_3V3	-	USB_I/O	USB 1 Data+
AF71	USB1_TX0_N	X_USB1_TX0_N (via 100nF capacitor to E25)	VDD_3V3	-	USB_I/O	USB 1 Lane 1 Transmit Data- (AC coupling capacitor is located on the module)
AE70	USB1_TX0_P	X_USB1_TX0_P (via 100nF capacitor to D26)	VDD_3V3	-	USB_I/O	USB 1 Lane 1 Transmit Data+ (AC coupling capacitor is located on the module)
AF67	USB1_RX0_N	X_USB1_RX0_N (B20)	VDD_3V3	-	USB_I/O	USB 1 Lane 1 Receive Data-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AE66	USB1_RX0_P	X_USB1_RX0_P (A21)	VDD_3V3	-	USB_I/O	USB 1 Lane 1 Receive Data+
AH71	Specialized	X_USB1_TX1_N (via 100nF capacitor to D22)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Transmit Data- (AC coupling capacitor is located on the module)
AG70	Specialized	X_USB1_TX1_P (via 100nF capacitor to E21)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Transmit Data+ (AC coupling capacitor is located on the module)
AH67	Specialized	X_USB1_RX1_N (A17)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Receive Data-
AG66	Specialized	X_USB1_RX1_P (B16)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Receive Data+
AE58	USB1_OC	GPIO_IO33 (W45)	VDD_1V8	1.8 V	I	USB 1 over current status input
AD57	USB1_PWR_EN	SAI1_TXFS (via boot mux to G49)	VDD_1V8	1.8 V	O	USB 1 power enable output

TABLE 15: USB 1 Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AA58	USB2_VBUS	X_USB2_VBUS (via 30k resistor to E27)	VDD_3V3	3.3 V / 5 V	I	USB 2 bus voltage detection (5 V compliant)
AA60	USB2_ID	X_USB2_ID (F24)	VDD_1V8	1.8 V	I	Currently has no function due to being a dedicated CPU pin. X_GPIO1_IO11 (DD5) is pre-connected to this contact via 0R resistor R143
AB61	USB2_D_N	X_USB2_D_N (A25)	VDD_3V3	-	USB_I/O	USB 2 Data-
AA62	USB2_D_P	X_USB2_D_P (B24)	VDD_3V3	-	USB_I/O	USB 2 Data+
AC58	USB2_OC	X_GPIO_IO34 (W49)	VDD_1V8	1.8 V	I	USB 2 over current status input
AB57	USB2_PWR_EN	X_SAI1_TXD0 (via boot mux to H48)	VDD_1V8	1.8 V	O	USB 2 power enable output

TABLE 16: USB 2 Signal Locations

11.7 Ethernet Interfaces ENET1 and ENET2

The phyFLEX-i.MX 95 FPSC provides two Ethernet Interfaces, ENET1 and ENET2, with TSN support. Connection of the phyFLEX-i.MX 95 FPSC to the World Wide Web or a local area network (LAN) is possible using the on-board GbE PHY at U13. It is connected to the RGMII interface of ENET2. The PHY operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s. Additionally, the RGMII interface of ENET1, which is available on the phyFLEX-Connector, can be used to connect an external PHY. (ENET1 RGMII Interface).

Note

PHYTEC has chosen to make the ENET1 available as RGMII for customers to accommodate their individual needs when it comes to choosing the right PHY or switching components applicable to their network topology.
As an example, we have connected a TSN-capable Ethernet PHY to ENET1 on the carrier board, which may be used for reference in your own design. See Ethernet (X8/X9) for details.

11.7.1 ENET2 Ethernet PHY (U13)

With an Ethernet PHY mounted at U13, the phyFLEX-i.MX 95 FPSC has been designed for use in 10Base-T, 100Base-T, and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyFLEX-Connector X1. **In a Linux environment, ENET2 interface is called eth0 as it is the port with on-board PHY.**

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AH57	GB_ETH1_A_N	X_ETH2_A_N	-	-	ETH_I/O	Gb Ethernet1 A N
AJ58	GB_ETH1_A_P	X_ETH2_A_P	-	-	ETH_I/O	Gb Ethernet1 A P
AF57	GB_ETH1_B_N	X_ETH2_B_N	-	-	ETH_I/O	Gb Ethernet1 B N
AG58	GB_ETH1_B_P	X_ETH2_B_P	-	-	ETH_I/O	Gb Ethernet1 B P
AG62	GB_ETH1_C_N	X_ETH2_C_N	-	-	ETH_I/O	Gb Ethernet1 C N
AH61	GB_ETH1_C_P	X_ETH2_C_P	-	-	ETH_I/O	Gb Ethernet1 C P
AE62	GB_ETH1_D_N	X_ETH2_D_N	-	-	ETH_I/O	Gb Ethernet1 D N
AF61	GB_ETH1_D_P	X_ETH2_D_P	-	-	ETH_I/O	Gb Ethernet1 D P
AJ68	Specialized	X_ETH2_GPIO0	VDD_1V8	1.8 V	I/O	1588 RX/TX SFD
AJ70	Specialized	X_ETH2_GPIO1	VDD_1V8	1.8 V	I/O	1588 RX/TX SFD
AJ60	GB_ETH1_LED_LINK	X_ETH2_LED0_LINK	-	-	OD	Gb Ethernet1 LED Link

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AG60	GB_ETH1_LED_ACT	X_ETH2_LED2_ACT	-	-	OD	Gb Ethernet1 LED Activity

TABLE 17: Ethernet PHY Signal Locations

11.7.1.1 Ethernet Signal Locations of ENET2

The on-board GbE PHY supports HP Auto-MDIX technology, eliminating the need for a direct-connect LAN or cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet PHY is connected to the RGMII interface ENET1 of the i.MX 95. Please refer to the *NXP Semiconductor i.MX 95 Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network, some external circuitry is required. The required termination resistors on the analog signals (ETH_A±, ETH_B±, ETH_C±, ETH_D±) are integrated into the chip, so there is no need to connect external termination resistors to these signals. Connection to external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+/C-, and D+/D- signals should be routed as 100-Ohm differential pairs. The same applies to the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

> **Warning**
>
> Please refer to the Ethernet PHY datasheet when designing the Ethernet transformer circuitry or request the schematic of the applicable carrier board (Libra Development Board i.MX 95).

11.7.2 Reset of the Ethernet Controller

The reset input of the Ethernet PHY at U13 is connected to the system reset POR_B.

11.7.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the internet, a table is used to convert the assigned IP address to the hardware's MAC address. In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyFLEX-i.MX 95 FPSC is located on the barcode sticker attached to the module. This number is a 12-digit HEX value.

11.7.4 ENET1 RGMII Interface

In order to use an external Ethernet PHY, the RGMII interface (ENET1) of the i.MX 95 is brought out at phyFLEX-Connector X1. ENET1 supports TSN network operation. For that use case, an external TSN-ready Ethernet switch device is used. **In a Linux environment, ENET1 interface is called eth1 as it is the port with external PHY.**

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AG44	RGMII2_MDIO	X_ENET1_MDIO (via 0R R131 to ENET2_MDIO AJ31)	VDD_1V8	1.8 V	I/O	Management Data
AJ50	RGMII2_TX_D0	X_ENET1_TD0 (AG33)	VDD_1V8	1.8 V	O	Transmit Data 0
AJ48	RGMII2_TX_D1	X_ENET1_TD1 (AG35)	VDD_1V8	1.8 V	O	Transmit Data 1
AH49	RGMII2_TX_D2	X_ENET1_TD2 (AF36)	VDD_1V8	1.8 V	O	Transmit Data 2
AJ46	RGMII2_TX_D3	X_ENET1_TD3 (AG37)	VDD_1V8	1.8 V	O	Transmit Data 3
AG50	RGMII2_TX_CTL	X_ENET1_TX_CTL (AF32)	VDD_1V8	1.8 V	O	Transmit Control
AG52	RGMII2_TXC	X_ENET1_TXC (AG31)	VDD_1V8	1.8 V	O	Transmit Clock
AG54	RGMII2_RX_CTL	X_ENET1_RX_CTL (AH34)	VDD_1V8	1.8 V	I	Receive Control
AG56	RGMII2_RXC	X_ENET1_RXC (AJ33)	VDD_1V8	1.8 V	I	Receive Clock

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ56	RGMII2_RX_D0	X_ENET1_RXD0 (AJ35)	VDD_1V8	1.8 V	I	Receive Data 0
AJ54	RGMII2_RX_D1	X_ENET1_RXD1 (AK36)	VDD_1V8	1.8 V	I	Receive Data 1
AJ52	RGMII2_RX_D2	X_ENET1_RXD2 (AJ37)	VDD_1V8	1.8 V	I	Receive Data 2
AH53	RGMII2_RX_D3	X_ENET1_RXD3 (AH38)	VDD_1V8	1.8 V	I	Receive Data 3
AG46	RGMII2_MDC	X_ENET1_MDC (via 0R R130 to ENET2_MDC AK32)	VDD_1V8	1.8 V	O	Management Clock
AH45	RGMII2_EVENT_IN	X_CCM_CLKO3 (AK20)	VDD_1V8	1.8 V	I	TSN Event In
AJ44	RGMII2_EVENT_OUT	X_CCM_CLKO4 (AJ21)	VDD_1V8	1.8 V	O	TSN Event Out
AG48	RGMII_nINT	X_GPIO_IO16 (P46)	VDD_1V8	1.8 V	I	PHY IRQ Input

TABLE 18: ENET0 RGMII Interface Signal Locations

11.8 10G Ethernet

The phyFLEX i.MX 95 provides 10G Ethernet MAC (TSN) with a USXGMII Interface to connect an external PHY. With an externally connected PHY like AQR113, the interface supports 10/100M and 1G/2G5/5G and 10G Ethernet.

Care must be taken with signal routing to connect the USXGMII SerDes lanes to an external PHY. PCB traces must be routed accurately with a differential impedance of 85 ohms (±10%). For AC coupling capacitors, connect high-quality X7R 100nF capacitors to the RX signals on the baseboard side to connect the TX outputs of the PHY device. It is recommended to strictly limit the number of vias and to use a maximum of two vias for each trace without stubs.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
U70	Specialized	X_ETH_TX0_N (via 100nF to AK16)	VDD_0V8	0.8 V	HCSL	10G Transmit -
T71	Specialized	X_ETH_TX0_P (via 00nF to AJ17)	VDD_0V8	0.8 V	HCSL	10G Transmit +
W70	Specialized	X_ETH_RX0_N (AK12)	VDD_0V8	0.8 V	HCSL	10G Receive -
V71	Specialized	X_ETH_RX0_P (AJ13)	VDD_0V8	0.8 V	HCSL	10G Receive +

TABLE 19: 10G Interface Signal Locations

11.9 SPI Interface

The Serial Peripheral Interface (SPI) is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyFLEX provides four SPI on the phyFLEX-Connector X1. The SPI provides one chip select signal for each interface. The Low Power SPI (LPSPI) of the i.MX 95 has eight separate modules (LPSPI1 to LPSPI8), which support clock rates of up to 60 MHz. The interface signals of three modules (LPSPI3, LPSPI4, LPSPI7) are made available on the phyFLEX-Connector. These modules are master/slave configurable. The following table lists the SPI signals on the phyFLEX-Connector.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L34	SPI1_CS	X_GPIO_IO04 (K46)	VDD_1V8	1.8 V	O	LPSPI7 Chip Select
N32	SPI1_MOSI	X_GPIO_IO06 (L49)	VDD_1V8	1.8 V	O	LPSPI7 Master Out
N34	SPI1_MISO	X_GPIO_IO05 (L45)	VDD_1V8	1.8 V	I	LPSPI7 Master In
M33	SPI1_SCLK	X_GPIO_IO07 (L51)	VDD_1V8	1.8 V	O	LPSPI7 Clock
N30	SPI2_CS	X_GPIO_IO08 (M44)	VDD_1V8	1.8 V	O	LPSPI3 Chip Select
L30	SPI2_MOSI	X_GPIO_IO10 (M48)	VDD_1V8	1.8 V	O	LPSPI3 Master Out
L32	SPI2_MISO	X_GPIO_IO09 (M46)	VDD_1V8	1.8 V	I	LPSPI3 Master In
M29	SPI2_SCLK	X_GPIO_IO11 (M52)	VDD_1V8	1.8 V	O	LPSPI3 Clock
AM41	SPI3_CS	X_GPIO_IO18 (P52)	VDD_1V8	1.8 V	O	LPSPI4 Chip Select

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AL38	SPI3_MOSI	X_GPIO_IO20 (R49)	VDD_1V8	1.8 V	O	LPSPI4 Master Out
AL36	SPI3_MISO	X_GPIO_IO19 (R45)	VDD_1V8	1.8 V	I	LPSPI4 Master In
AL40	SPI3_SCLK	X_GPIO_IO21 (R51)	VDD_1V8	1.8 V	O	LPSPI4 Clock

TABLE 20: SPI Interface Signal Locations

11.10 QSPI Interface

The Quad Serial Peripheral Interface (QSPI) is a bidirectional serial bus with up to 4 data lanes that provides a simple and efficient method for data exchange among devices. The phyFLEX provides QSPI on the phyFLEX-Connector X1. The QSPI provides one chip select signal for the interface. The FLexSPI of the i.MX 95 supports single, dual, and quad modes in single data rate (SDR) and double data rate (DDR) transfer mode. The interface signals of FlexSPI mode are made available on the phyFLEX-Connector. The following table lists the QSPI signals on the phyFLEX-Connector.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ24	Mandatory	X_XSPI1_SS0_B (AJ41)	VDD_1V8	1.8 V	O	FlexSPI chip select
AG24	Mandatory	X_XSPI1_SCLK (AJ43)	VDD_1V8	1.8 V	O	FlexSPI clock
AF21	Mandatory	X_XSPI1_DATA0 (AJ45)	VDD_1V8	1.8 V	I/O	FlexSPI data lane 0
AG20	Mandatory	X_XSPI1_DATA1 (AH46)	VDD_1V8	1.8 V	I/O	FlexSPI data lane 1
AG22	Mandatory	X_XSPI1_DATA2 (AJ47)	VDD_1V8	1.8 V	I/O	FlexSPI data lane 2
AH21	Mandatory	X_XSPI1_DATA3 (AK48)	VDD_1V8	1.8 V	I/O	FlexSPI data lane 3
AJ22	Optional	-	-	-	-	-

TABLE 21: QSPI Interface Signal Locations

11.11 I^2C / I^3C Interface

The (Improved) Inter-Integrated Circuit (I^2C / I^3C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 95 contains eight identical and independent Multimaster fast-mode I^2C modules and two I^3C modules. The interface of 5 modules is available on the phyFLEX-Connector X1. I^2C2 is reserved for controlling the SOM, and I^2C1 supports the I^3C protocol.

Tip

To ensure the proper functioning of the I^2C interface, external pull resistors matching the load at the interface must be connected. There are no pull-up resistors mounted on the module. For detailed information on the voltage levels for the pull-up resistors, please refer to the *i.MX 95 Datasheet.*

The following table lists the I^2C / I^3C ports on the phyFLEX-Connector:

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L60	I2C2_SCL	X_GPIO_IO23 (T46)	VDD_1V8	1.8 V	I/OD	LPI^{2}C5 Clock
L58	I2C2_SDA	X_GPIO_IO22 (T44)	VDD_1V8	1.8 V	I/OD	LPI^{2}C5 Data
M61	I2C3_SCL	X_GPIO_IO29 (V44)	VDD_1V8	1.8 V	I/OD	LPI^{2}C3 Clock
N60	I2C3_SDA	X_GPIO_IO28 (U51)	VDD_1V8	1.8 V	I/OD	LPI^{2}C3 Data
AN36	I2C4_SCL	X_GPIO_IO31 (V48)	VDD_1V8	1.8 V	I/OD	LPI^{2}C4 Clock
AN38	I2C4_SDA	X_GPIO_IO30 (V46)	VDD_1V8	1.8 V	I/OD	LPI^{2}C4 Data
AN40	I2C5_SCL/I3C_SCL	X_I2C1_SCL (D48)	VDD_1V8	1.8 V	I/OD	LPI^{2}C1/I^{3}C1 Clock

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AN42	I2C5_SDA/I3C_SDA	X_I2C1_SDA (D52)	VDD_1V8	1.8 V	I/OD	LPI^2C1/I^3C1 Data
L26	I2C1_SCL_DNU	I2C2_SDA (E45)	VDD_1V8	1.8 V	I/OD	LPI^2C2 Clock used for on-board communication to PMIC
L28	I2C1_SDA_DNU	I2C2_SCL (E43)	VDD_1V8	1.8 V	I/OD	LPI^2C2 Data used for on-board communication to PMIC

TABLE 22: I2C / I3C Interface Signal Locations

11.12 Audio Interface

The i.MX 95 supports multiple audio interfaces. One of them is available by default as listed below:

Interface	RX Data Line	TX Data Line
SAI-5	4	0

TABLE 23: phyFLEX-i.MX 95 FPSC Audio Interfaces

11.12.1 I^2S Audio Interface (SAI)

The phyFLEX-i.MX 95 FPSC features a Synchronous Audio Interface that supports full-duplex serial interfaces with frame synchronization, such as I2S, AC97, and TDM. The interface is divided into four sub-interfaces: SAI1, SAI2, SAI3, and SAI5. SAI5 is routed directly to the phyFLEX-Connector X1 by default.

The tables below show the signal locations of the SAI5 interface.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level**	Signal Type	Muxing / Description
AJ32	SAI1_MCLK	na	-	-	-	Add an external clock generator
AH29	SAI1_TX_BCLK	X_XSPI1_DATA6 (AJ51)	VDD_1V8	1.8V	O	SAI5 TX BCLK
AJ30	SAI1_TX_SYNC	X_XSPI1_DATA5 (AK50)	VDD_1V8	1.8V	O	SAI5 TX SYNC
AJ28	SAI1_TX_DATA	X_XSPI1_DATA4 (AJ49)	VDD_1V8	1.8V	O	SAI5 TXD0
AG28	SAI1_RX_BCLK	XSPI1_SS1_B (AH42)	VDD_1V8	1.8V	I	SAI5 RXC
AG32	SAI1_RX_SYNC	XSPI1_DQS (AK44)	VDD_1V8	1.8V	I	SAI5 RXFS
AG30	SAI1_RX_DATA	XSPI1_DATA7 (AH50)	VDD_1V8	1.8V	I	SAI5 RXD0

TABLE 24: SAI1 Interface Signal Locations

11.13 PCI Express Interfaces

The phyFLEX-i.MX 95 FPSC supports two one-lane PCI Express interfaces with PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. Additional control signals that might be required (e.g., “present” and “wake”) can be implemented with GPIOs. Please refer to the schematic of a suitable PHYTEC carrier board (e.g., Libra Development Board) for a circuit example.

The position of the PCIe signals on the phyFLEX-Connector X1 is shown below:

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
Y11	PCIE1_TXN_N	X_PCIE1_TX0_N (via 100nF to D30)	VDDA_1V8	LVDS	PCIe_O	PCIe1 TXN- (The AC coupling capacitor is located on the module)
AA12	PCIE1_TXN_P	X_PCIE1_TX0_P (via 100nF to E29)	VDDA_1V8	LVDS	PCIe_O	PCIe1 TXN+ (The AC coupling capacitor is located on the module)
AB11	PCIE1_RXN_N	X_PCIE1_RX0_N (A29)	VDDA_1V8	LVDS	PCIe_I	PCIe1 RXN-
AC12	PCIE1_RXN_P	X_PCIE1_RX0_P (B28)	VDDA_1V8	LVDS	PCIe_I	PCIe1 RXN+
AA14	PCIE1_CLK_N	X_PCIE1_CLK_P (B26 or B30)	VDDA_1V8	LVDS	PCIe_I/O	PCIe1 Ref CLK+ Output/Input J1=2+3 CPU Output from B26 (default) J1=1+2 CPU Input to B30 ** Diff-Pair polarity is inverse. Does not affect functionality.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	**FPSC Signal** **Mandatory** **Optional** **Specialized**	**SOM Signal Name (CPU Ball)**	**SOM Voltage Domain**	**Signal Level**	**Signal Type**	**Muxing / Description**
AB15	PCIE1_CLK_P	X_PCIE1_CLK_N (C27 or C31)	VDDA_1V8	LVDS	PCIe_I/O	PCIe1 Ref CLK- Output/Input J2=2+3 CPU Output from C27 (default) J2=1+2 CPU Input to C31 ** Diff-Pair polarity is inverse. Does not affect functionality.
AC16	PCIE1_nCLKREQ	X_GPIO_IO32 (V52)	VDD_1V8	1.8 V	I	PCIe1 Clk request Input
AC14	PCIE1_nPERST	X_PDM_BIT_STREAM1 (H46)	VDD_1V8	1.8 V	O	PCIe1 reset Output
AN22	PCIE2_TXN_N	X_PCIE2_TX0_N (via 100nF to F32)	VDDA_1V8	LVDS	PCIe_O	PCIe1 TXN- (The AC coupling capacitor is located on the module)
AN24	PCIE2_TXN_P	X_PCIE2_TX0_P (via 100nF to E31)	VDDA_1V8	LVDS	PCIe_O	PCIe1 TXN+ (The AC coupling capacitor is located on the module)

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AN26	PCIE2_RXN_N	X_PCIE2_RX0_N (C35)	VDDA_1V8	LVDS	PCIe_I	PCIe1 RXN-
AN28	PCIE2_RXN_P	X_PCIE2_RX0_P (B34)	VDDA_1V8	LVDS	PCIe_I	PCIe1 RXN+
AL24	PCIE2_CLK_N	X_PCIE2_REF_PAD_CLK_N (A33)	VDDA_1V8	LVDS	PCIe_I/O	PCIe1 Ref CLK- Input
AL26	PCIE2_CLK_P	X_PCIE2_REF_PAD_CLK_P (B32)	VDDA_1V8	LVDS	PCIe_I/O	PCIe1 Ref CLK+ Input
AM21	PCIE2_nCLKREQ	X_GPIO_IO35 (W51)	VDD_1V8	1.8 V	I	PCIe1 Clk request Input
AM25	PCIE2_nPERST	X_SAI1_RXD0 (H52)	VDD_1V8	1.8 V	O	PCIe1 reset Output

TABLE 25: PCIe Interface Signal Locations

12 General Purpose I/Os

All pins that are not used by any of the other interfaces specifically described in this manual can be used as GPIO without affecting other features of the phyFLEX-i.MX 95 FPSC. These pins are listed below:

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AL32	GPIO1	X_UART1_TXD (F52)	VDD_1V8	1.8 V	I/O	GPIO1_IO05
AN30	GPIO2	X_UART1_RXD (E49)	VDD_1V8	1.8 V	I/O	GPIO1_IO04
AN32	GPIO3	X_SAI1_TXC (G51)	VDD_1V8	1.8 V	I/O	GPIO1_IO12
L40	GPIO4	X_GPIO_IO17 (P48)	VDD_1V8	1.8 V	I/O	GPIO2_IO17
N40	GPIO5	-	-	-	-	-
AL34	GPIO6	-	-	-	-	-
AN34	GPIO7	-	-	-	-	-
CA18	PWM1	GPIO_IO24 (T48)	VDD_1V8	1.8 V	O	TPM3_3
CB19	PWM2	GPIO_IO26 (U45)	VDD_1V8	1.8 V	O	TPM5_3
BD11	PWM3	-	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
BE17	PWM4	-	-	-	-	-

TABLE 26: GPIO Pin Locations

Besides these pins, most of the i.MX 95 signals, which are connected directly to the module connector, can be configured to act as GPIOs due to the multiplexing functionality of most controller pins. Normally, pins with signal type I/O are able to work as a GPIO.

13 Debug Interface

The phyFLEX-i.MX 95 FPSC is equipped with a JTAG interface to download program code into the external flash, internal controller RAM, or any debugging programs being executed. The location of the JTAG pins on the phyFLEX-Connector X1 are below:

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AC20	JTAG_TCK	X_JTAG_TCK (AG21)	VDD_1V8	1.8 V	I	JTAG clock signal.
AC22	JTAG_TDI	X_JTAG_TDI (AK24)	VDD_1V8	1.8 V	I	JTAG data in the signal
AD25	JTAG_TDO	X_JTAG_TDO (via 0R to AJ23)	VDD_1V8	1.8 V	O	JTAG data out signal
AC24	JTAG_TMS	X_JTAG_TMS (AH22)	VDD_1V8	1.8 V	I	JTAG test mode select signal
AD21	JTAG_Reserved	-	-	-	-	-

TABLE 27: Debug Interface Signal Locations

13.1 UART Debug

The default debug UART Interfaces is FPSC UART3 (i.MX 95 LPUART7) for Cortex-A55 Cores and FPSC UART2 (i.MX 95 LPUART5) for Cortex-M7 Core. FPSC UART3 is accessible on connector X1 pins AE22 (RXD) and AE20 (TXD), and FPSC UART2 on pins N46 (RXD) and N44 (TXD).

For more information, also refer to Universal Asynchronous Interfaces (UARTs).

14 Display Interfaces

14.1 Low Voltage Differential Signal Display Interface (LVDS)

The phyFLEX-i.MX 95 FPSC offers one LVDS display interface, which supports two output channels.

The locations of the LVDS signals are shown below:

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
LVDS channel 0						
L52	LVDS1_DATA0_N	X_LVDS0_D0_N (G9)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA0-
L50	LVDS1_DATA0_P	X_LVDS0_D0_P (G7)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA0+
L54	LVDS1_DATA1_N	X_LVDS0_D1_N (F8)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA1-
M53	LVDS1_DATA1_P	X_LVDS0_D1_P (F6)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA1+
N52	LVDS1_CLK_N	X_LVDS0_CLK_N (A5)	VDDA_1V8	LVDS	LVDS_O	LVDS0 Clock-
N50	LVDS1_CLK_P	X_LVDS0_CLK_P (B4)	VDDA_1V8	LVDS	LVDS_O	LVDS0 Clock+
N56	LVDS1_DATA2_N	X_LVDS0_D2_N (E7)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA2-
N54	LVDS1_DATA2_P	X_LVDS0_D2_P (D6)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA2+
M57	LVDS1_DATA3_N	X_LVDS0_D3_N (E9)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA3-
L56	LVDS1_DATA3_P	X_LVDS0_D3_P (D8)	VDDA_1V8	LVDS	LVDS_O	LVDS0 DATA3+

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
LVDS channel 1						
AN60	LVDS2_DATA0_N	X_LVDS1_D0_N (A3)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA0-
AM61	LVDS2_DATA0_P	X_LVDS1_D0_P (B2)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA0+
AL56	LVDS2_DATA1_N	X_LVDS1_D1_N (C3)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA1-
AL58	LVDS2_DATA1_P	X_LVDS1_D1_P (C1)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA1+
AN54	LVDS2_CLK_N	X_LVDS1_CLK_N (D4)	VDDA_1V8	LVDS	LVDS_O	LVDS1 Clock-
AN56	LVDS2_CLK_P	X_LVDS1_CLK_P (D2)	VDDA_1V8	LVDS	LVDS_O	LVDS1 Clock+
AM57	LVDS2_DATA2_N	X_LVDS1_D2_N (E3)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA2-
AN58	LVDS2_DATA2_P	X_LVDS1_D2_P (E1)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA2+
AL52	LVDS2_DATA3_N	X_LVDS1_D3_N (F4)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA3-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AL54	LVDS2_DATA3_N	X_LVDS1_D3_P (F2)	VDDA_1V8	LVDS	LVDS_O	LVDS1 DATA3+

TABLE 28: Display Interface LVDS Signal Locations

15 Camera Connections

The phyFLEX-i.MX 95 FPSC offers 2 MIPI-CSI interfaces to connect digital cameras. The two MIPI/CSI-2 camera interfaces of the i.MX 95 extends to the phyFLEX-Connector X1 with 4 data lanes and one clock lane.

The locations of the MIPI-CSI signals are shown below:

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
T57	CSI1_D0_N	MIPI_CSI1_D0_N (F20)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA0-
U58	CSI1_D0_P	MIPI_CSI1_D0_P (E19)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA0+
T61	CSI1_D1_N	MIPI_CSI1_D1_N (D18)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA1-
U62	CSI1_D1_P	MIPI_CSI1_D1_P (E17)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA1+
R62	CSI1_CLK_N	MIPI_CSI1_CLK_N (F16)	VDD_1V8	LVDS	CSI2_I	CSI1 Clock-
R60	CSI1_CLK_P	MIPI_CSI1_CLK_P (E15)	VDD_1V8	LVDS	CSI2_I	CSI1 Clock+
P57	CSI1_D2_N	MIPI_CSI1_D2_N (D14)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA2-
R58	CSI1_D2_P	MIPI_CSI1_D2_P (E13)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA2+
N62	CSI1_D3_N	MIPI_CSI1_D3_N (F12)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA3-
P61	CSI1_D3_P	MIPI_CSI1_D3_P (E11)	VDD_1V8	LVDS	CSI2_I	CSI1 DATA3+

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
G42	CSI2_D0_N	MIPI_DSICSI1_D0_N (C15)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA0-
G44	CSI2_D0_P	MIPI_DSICSI1_D0_P (B14)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA0+
J44	CSI2_D1_N	MIPI_DSICSI1_D1_N (D18)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA1-
H45	CSI2_D1_P	MIPI_DSICSI1_D1_P (E17)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA1+
H41	CSI2_CLK_N	MIPI_DSICSI1_CLK_N (C11)	VDD_1V8	LVDS	CSI2_I	CSI2 Clock-
J42	CSI2_CLK_P	MIPI_DSICSI1_CLK_P (B10)	VDD_1V8	LVDS	CSI2_I	CSI2 Clock+
J38	CSI2_D2_N	MIPI_DSICSI1_D2_N (D14)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA2-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J40	CSI2_D2_P	MIPI_DSICSI1_D2_P (E13)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA2+
G38	CSI2_D3_N	MIPI_DSICSI1_D3_N (B6)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA3-
G40	CSI2_D3_P	MIPI_DSICSI1_D3_P (C7)	VDD_1V8	LVDS	CSI2_I	CSI2 DATA3+

TABLE 29: Camera Interface MIPI / CSI-2 Signal Locations

16 ADC Inputs

The phyFLEX i.MX 95 FPSC provides a 16-channel, 12-bit SAR ADC with 8 single-ended inputs. The second 8 channels are muxed internally in the CPU.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
R16	ADC0	ADC_IN0 (A37)	VDD_1V8	1.8 V	I	ADC Analog Inut 0
T15	ADC1	ADC_IN1 (B38)	VDD_1V8	1.8 V	I	ADC Analog Inut 1
U16	ADC2	ADC_IN2 (C39)	VDD_1V8	1.8 V	I	ADC Analog Inut 2
U14	ADC3	ADC_IN3 (B40)	VDD_1V8	1.8 V	I	ADC Analog Inut 3
V15	ADC4	ADC_IN4 (A41)	VDD_1V8	1.8 V	I	ADC Analog Inut 4
W16	ADC5	ADC_IN5 (B42)	VDD_1V8	1.8 V	I	ADC Analog Inut 5
W14	ADC6	ADC_IN6 (B44)	VDD_1V8	1.8 V	I	ADC Analog Inut 6
Y15	ADC7	ADC_IN7 (A45)	VDD_1V8	1.8 V	I	ADC Analog Inut 7

TABLE 30: ADC Inputs Signal Locations

17 FPSC Reserved Target-Specific Proprietary Signals

The following signals are not defined according to FPSC Gamma Feature Set Specifications (LAN-118e.A6). These signals are processor-specific and should only be used in an application if no direct compatibility between different SOMs is required.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
V25	Specialized	nc	-	-	-	-
W22	Specialized	nc	-	-	-	-
W24	Specialized	nc	-	-	-	-
N28	Specialized	nc	-	-	-	-
P15	Specialized	X_WDOG_ANY (J45)	NVCC_AON	1.8 V	OD	X_WDOG_ANY is connected to X_FCCU1 via R132 and is used to drive a cold reset.
Y25	Specialized	nc	-	-	-	-
AH67	Specialized	X_USB1_RX1_N (A17)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Receive Data-
AG66	Specialized	X_USB1_RX1_P (B16)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Receive Data+
AH71	Specialized	X_USB1_TX1_N (via 100nF capacitor to D22)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Transmit Data- (AC coupling capacitor is located on the module)

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AG70	Specialized	X_USB1_TX1_P (via 100nF capacitor to E21)	VDD_3V3	-	USB_I/O	USB 1 Lane 2 Transmit Data+ (The AC coupling capacitor is located on the module.)
AA66	Specialized	nc	-	-	-	-
Y67	Specialized	nc	-	-	-	-
AA70	Specialized	nc	-	-	-	-
Y71	Specialized	nc	-	-	-	-
E26	Specialized	nc	-	-	-	-
E28	Specialized	nc	-	-	-	-
E32	Specialized	nc	-	-	-	-
E34	Specialized	nc	-	-	-	-
E38	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
E40	Specialized	nc	-	-	-	-
E42	Specialized	nc	-	-	-	-
E44	Specialized	nc	-	-	-	-
E48	Specialized	nc	-	-	-	-
E50	Specialized	nc	-	-	-	-
E54	Specialized	nc	-	-	-	-
E56	Specialized	nc	-	-	-	-
H75	Specialized	nc	-	-	-	-
J74	Specialized	nc	-	-	-	-
L74	Specialized	nc	-	-	-	-
M75	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P75	Specialized	nc	-	-	-	-
R74	Specialized	nc	-	-	-	-
U74	Specialized	nc	-	-	-	-
V75	Specialized	nc	-	-	-	-
Y75	Specialized	nc	-	-	-	-
AB75	Specialized	nc	-	-	-	-
AC74	Specialized	nc	-	-	-	-
AE74	Specialized	nc	-	-	-	-
AF75	Specialized	nc	-	-	-	-
AH75	Specialized	nc	-	-	-	-
AJ74	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AL74	Specialized	X_CCM_CLKO2	VDD_1V8	1.8 V	I/O	GPIO3_IO27
H7	Specialized	nc	-	-	-	-
G20	Specialized	nc	-	-	-	-
G22	Specialized	nc	-	-	-	-
G24	Specialized	X_UART2_TXD	VDD_1V8	1.8 V	O	UART2_TXD (imx95 M33 System-Manger Debug)
G26	Specialized	X_UART2_RXD	VDD_1V8	1.8 V	I	UART2_RXD
G28	Specialized	nc	-	-	-	-
G30	Specialized	nc	-	-	-	-
G32	Specialized	nc	-	-	-	-
G34	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
G36	Specialized	nc	-	-	-	-
G46	Specialized	X_TAMPER1	VDD_1V8	1.8 V	I	TAMPER1 Input. Has a 100k pull-down.
G48	Specialized	nc	-	-	-	-
G50	Specialized	nc	-	-	-	-
G52	Specialized	X_CLKIN1	VDD_1V8	1.8 V	I	Clock Input. Has a 100k pull-down.
L70	Specialized	nc	-	-	-	-
M71	Specialized	nc	-	-	-	-
H25	Specialized	nc	-	-	-	-
H29	Specialized	nc	-	-	-	-
H33	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
H37	Specialized	nc	-	-	-	-
H49	Specialized	X_EEPROM2_WC	VDD_1V8	1.8 V	I	Write Control Input of the User EEPROM. EEPROM is write-unprotected by default. Has a 10k pull-down.
H53	Specialized	X_CLKIN2	VDD_1V8	1.8 V	I	Clock Input. Has a 100k pull-down.
L68	Specialized	nc	-	-	-	-
N68	Specialized	nc	-	-	-	-
R68	Specialized	nc	-	-	-	-
U68	Specialized	X_ETH_CLK_EN	VDD_1V8	1.8 V	I	Clock Enable Input for 10G ETH clock generator. Pre-connected via R146 (0R) to X_CCM_CLKO1. Has a 10k pull-down.
W68	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	**FPSC Signal** **Mandatory** **Optional** **Specialized**	**SOM Signal Name (CPU Ball]**	**SOM Voltage Domain**	**Signal Level**	**Signal Type**	**Muxing / Description**
AA68	Specialized	nc	-	-	-	-
AC68	Specialized	nc	-	-	-	-
J28	Specialized	nc	-	-	-	-
J30	Specialized	nc	-	-	-	-
J32	Specialized	nc	-	-	-	-
J34	Specialized	nc	-	-	-	-
J36	Specialized	nc	-	-	-	-
J46	Specialized	X_TAMPER0	VDD_1V8	1.8 V	I	TAMPER0 Input. Has a 100k pull-down.
J48	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J50	Specialized	X_EEPROM1_WC	VDD_1V8	1.8 V	I	Write Control Input of the Factory EEPROM. EEPROM is write-protected by default. Has a 10k pull-up.
J52	Specialized	X_nTEMP_ALERT	VDD_1V8	1.8 V	OD	ALERT wired-or outputs of the Temperature Sensors U15-U18. X_nTEMP_ALERT has a 10k pull-up to VDD_1V8.
J54	Specialized	X_RTC_EVI	VDD_3V3 or X_RTC_VBACKUP	3.3 V or X_RTC_VBACKUP voltage level	I	Event Input of the RTC RV-3028-C7 U14. X_RTC_EVI has a 100k pull-down and can be left unconnected. Input high level is 0.8xVDD, determined by VDD_3V3 or the voltage level at X_RTC_VBACKUP in backup mode. For more information, refer to the Micro Crystal RV-3028-C7 App-Manual
M67	Specialized	nc	-	-	-	-
N66	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P67	Specialized	nc	-	-	-	-
AJ42	Specialized	nc	-	-	-	-
AJ40	Specialized	nc	-	-	-	-
AJ38	Specialized	nc	-	-	-	-
AJ36	Specialized	nc	-	-	-	-
AJ34	Specialized	nc	-	-	-	-
AJ26	Specialized	nc	-	-	-	-
M49	Specialized	nc	-	-	-	-
AH41	Specialized	nc	-	-	-	-
AH37	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AM75	Specialized	X_CCM_CLKO1	VDD_1V8	1.8 V	O	X_CCM_CLKO1 is connected via R146 (0R) to X_ETH_CLK_EN.
AR56	Specialized	nc	-	-	-	-
AR54	Specialized	nc	-	-	-	-
AR50	Specialized	nc	-	-	-	-
AR48	Specialized	nc	-	-	-	-
AR44	Specialized	nc	-	-	-	-
AR42	Specialized	nc	-	-	-	-
AR40	Specialized	nc	-	-	-	-
AR38	Specialized	nc	-	-	-	-
AR34	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AR32	Specialized	nc	-	-	-	-
AR28	Specialized	nc	-	-	-	-
AR26	Specialized	nc	-	-	-	-
AM7	Specialized	nc	-	-	-	-
AL8	Specialized	nc	-	-	-	-
AJ8	Specialized	nc	-	-	-	-
AH7	Specialized	nc	-	-	-	-
AF7	Specialized	nc	-	-	-	-
AE8	Specialized	nc	-	-	-	-
AC8	Specialized	nc	-	-	-	-
AB7	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
Y7	Specialized	nc	-	-	-	-
V7	Specialized	nc	-	-	-	-
U8	Specialized	nc	-	-	-	-
R8	Specialized	nc	-	-	-	-
P7	Specialized	nc	-	-	-	-
M7	Specialized	nc	-	-	-	-
L8	Specialized	nc	-	-	-	-
J8	Specialized	nc	-	-	-	-
N70	Specialized	nc	-	-	-	-
P71	Specialized	nc	-	-	-	-
R70	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	**FPSC Signal** **Mandatory** **Optional** **Specialized**	**SOM Signal Name (CPU Ball]**	**SOM Voltage Domain**	**Signal Level**	**Signal Type**	**Muxing / Description**
AD71	Specialized	nc	-	-	-	-
AJ70	Specialized	X_ETH2_GPIO1	VDD_1V8	1.8 V	I/O	GPIO_1 (Pin 40) from the Ethernet PHY DP83867IRRGZ.
AN62	Specialized	nc	-	-	-	-
AN20	Specialized	X_EARC_AUX	#NV	#NV	#NV	#NV
W12	Specialized	nc	-	-	-	-
V11	Specialized	nc	-	-	-	-
U12	Specialized	nc	-	-	-	-
T11	Specialized	nc	-	-	-	-
R12	Specialized	nc	-	-	-	-
P11	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
N12	Specialized	X_PGOOD	VDD_1V8	1.8 V	OD	PMIC Power Good status output. Has a 100k pull-up.
M11	Specialized	X_FS0B	VDD_1V8	1.8 V	OD	PMIC status output. Has a 100k pull-up.
L12	Specialized	nc	-	-	-	-
H21	Specialized	nc	-	-	-	-
AE68	Specialized	nc	-	-	-	-
AG68	Specialized	nc	-	-	-	-
AJ68	Specialized	X_ETH2_GPIO0	VDD_1V8	1.8 V	I/O	GPIO_0 (Pin 39) from the Ethernet PHY DP83867IRRGZ. It is used for the 4-Strap config. Do not drive this signal during reset.
AM53	Specialized	nc	-	-	-	-
AM37	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AM33	Specialized	VDD_ARM	VDD_ARM	0.9 V	-	Do not connect. For factory use only.
AM29	Specialized	VDD_SOC	VDD_SOC	0.9 V	-	Do not connect. For factory use only.
R14	Specialized	nc	-	-	-	-
N14	Specialized	nc	-	-	-	-
L14	Specialized	X_ENET1_MDC/ GPIO4_IO00	VDD_1V8	1.8 V	O	X_ENET1_MDC is connected via R45 (0R) to X_ETH2_nINT_nPWDN.
J24	Specialized	VDD2_DDR	VDD2_DDR	1.05 V	-	Do not connect. For factory use only.
J26	Specialized	nc	-	-	-	-
R66	Specialized	nc	-	-	-	-
T67	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
U66	Specialized	nc	-	-	-	-
W66	Specialized	nc	-	-	-	-
AD67	Specialized	nc	-	-	-	-
AL30	Specialized	nc	-	-	-	-
AL28	Specialized	nc	-	-	-	-
AA16	Specialized	nc	-	-	-	-
N16	Specialized	nc	-	-	-	-
M15	Specialized	nc	-	-	-	-
L36	Specialized	nc	-	-	-	-
L48	Specialized	nc	-	-	-	-
AH33	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AH25	Specialized	nc	-	-	-	-
AG42	Specialized	nc	-	-	-	-
AG40	Specialized	nc	-	-	-	-
AG38	Specialized	nc	-	-	-	-
AG36	Specialized	nc	-	-	-	-
AG34	Specialized	nc	-	-	-	-
AG26	Specialized	X_PMIC_INT_B	VDD_1V8	1.8 V	OD	X_PMIC_IRQ_B is connected via R58 (0R) to X_ENET1_MDIO/ GPIO4_IO01 (AJ39) to support PMIC IRQ. X_PMIC_IRQ_B has a 10k pull-up.
AF25	Specialized	nc	-	-	-	-
W70	Specialized	X_ETH_RX0_N (AK12)	VDD_0V8	0.8 V	HCSL	10G Receive -

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
V71	Specialized	X_ETH_RX0_P (AJ13)	VDD_0V8	0.8 V	HCSL	10G Receive +
U70	Specialized	X_ETH_TX0_N (via 100nF to AK16)	VDD_0V8	0.8 V	HCSL	10G Transmit -
T71	Specialized	X_ETH_TX0_P (via 00nF to AJ17)	VDD_0V8	0.8 V	HCSL	10G Transmit +

TABLE 31: PSC Reserved Target-Specific Proprietary Signals

18 RTC

The phyFLEX i.MX 95 has an on-board, externally mounted RTC. The RV-3028-C7 is the newest generation of RTC from Micro Crystal with an extremely low backup current, typically 40nA at 25 degrees. PHYTEC uses the most optimal implementation in each phyFLEX design to give the most optimal usage for all customers.

The RTC is accessible over I^2C1 on Address 0x52. In a normal operation state, the RTC power is supplied from the SOM voltage VDD_3V3. If the SOM is not powered and RTC backup is needed, the VBACKUP Pin of the RTC can be supplied over the X_RTC_VBACKUP pin X1-AA22. The RTC provides an interrupt output signal (X_RTC_INT), which is fed to the module connector X1-T21. This signal is an open drain (OD). The on-board pull-up resistor is, by default, not mounted. To use the X_RTC_INT signal, add an external pull-up resistor (e.g., 10k) to an appropriate I/O voltage level (e.g., X_RTC_VBACKUP).

Furthermore, the RTC is able to supply a programmable clock output signal (push-pull) RTC_CLKOUT. Frequencies of 1/32/64/1024/8192 Hz and 32.768 Hz (default) are programmable. The RTC_CLKOUT signal is fed to the module connector at X1-U20 (1.8V level shifted). For a detailed description of the programming capabilities of the RTC, refer to the *Micro Crystal RV-3028-C7 App-Manua*l. The RTC supports an external event input signal (X_RTC_EVI at X1-J54), which can be used, e.g., for interrupt generation or timestamp functions. A 100k pull-down resistor is connected to this signal. For a detailed description of the programming capabilities of the RTC, refer to the *Micro Crystal RV-3028-C7 App-Manua*l.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
U20	RTC_CLKOUT	X_RTC_CLKOUT	VDD_1V8	1.8 V	O	
T21	RTC_nINT	X_RTC_INT	-	-	OD	RTC IRQ output. Needs an external Pull-Up resistor.
AA22	VCC_RTC	X_RTC_VBACKUP	-	3.3 V (1.1 V to 5.5V)	PWR_I	3.3 V backup voltage input. If not needed, pull with 10k to GND
J54	Specialized	X_RTC_EVI	VDD_3V3 or X_RTC_VBACKUP	3.3 V or X_RTC_VBACKUP voltage level	I	Event Input of the RTC RV-3028-C7 U14. X_RTC_EVI has a 100k pull-down and can be left unconnected. Input high level is 0.8xVDD, determined by VDD_3V3 or the voltage level at X_RTC_VBACKUP in backup mode. For more information, refer to the Micro Crystal RV-3028-C7 App-Manual

TABLE 32: RTC Signal Locations

19 Temperature Sensors

The phyFLEX-i.MX 95 FPSC supports two internally sensored thermal zones in the i.MX 95 CPU as well as 4 externally sensored thermal zones for monitoring board-level temperatures. The presence of the sensors depends on the delivery variant of the module.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J52	Specialized	X_nTEMP_ALERT	VDD_1V8	1.8 V	OD	ALERT wired-or outputs of the Temperature Sensors U15-U18. X_nTEMP_ALERT has a 10k pull-up to VDD_1V8.

TABLE 33: Temperature Sensors Signal Locations

The external temperature sensors are located at the following positions.

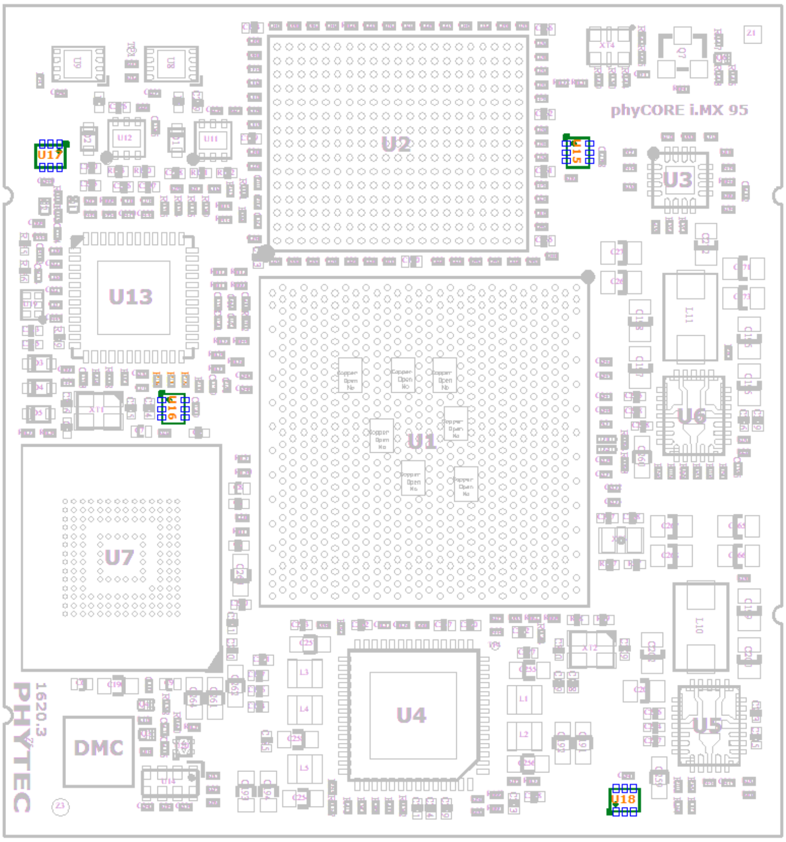


FIGURE 5: Temperature Sensor Locations

The TMP102 temperature sensor devices used are connected to the I^2C1 bus. TMP102 measures temperatures from -40 °C to +125 °C. For a more detailed description of TMP102, refer to the Texas Instruments *TMP102 Datasheet*.

Sensor	I^2C Slave Address
U15	0x48
U16	0x49
U17	0x4A
U18	0x4B

TABLE 34: I2C1 Temperature Sensor Slave Addresses

20 CPU Core Frequency Scaling

The phyFLEX-i.MX 95 FPSC is able to scale the clock frequency and voltage. This is used to save power and reduce heat dissipation when the full performance of the CPU is not needed. Scaling the frequency and voltage is referred to as 'Dynamic Voltage and Frequency Scaling' (DVFS). The phyFLEX-i.MX 95 FPSC BSP supports the DVFS feature. The *Linux* kernel provides a DVFS framework that allows each CPU core to have a min/max frequency as well as the applicable voltage and a governor that governs these values depending on the system load. Depending on the i.MX 95 variant used; several different frequencies are supported. Further details on how to configure this governor can be found in the phyFLEX-i.MX 95 BSP Manual.

21 Technical Specifications

> **Warning**
>
> Due to changes in functionality and design that are currently being developed, there are several values that cannot be determined in time for the release of this manual. All values with "TBD (To Be Determined)" are currently being evaluated. These values will be added to future manual editions.

The module's profile is max. 6 mm thick, with a maximum component height of 1 mm on the bottom side of the PCB and approximately 3 mm on the top side. The board itself is approximately 2 mm thick. The phyFLEX-i.MX 95 Footprint can be seen below.

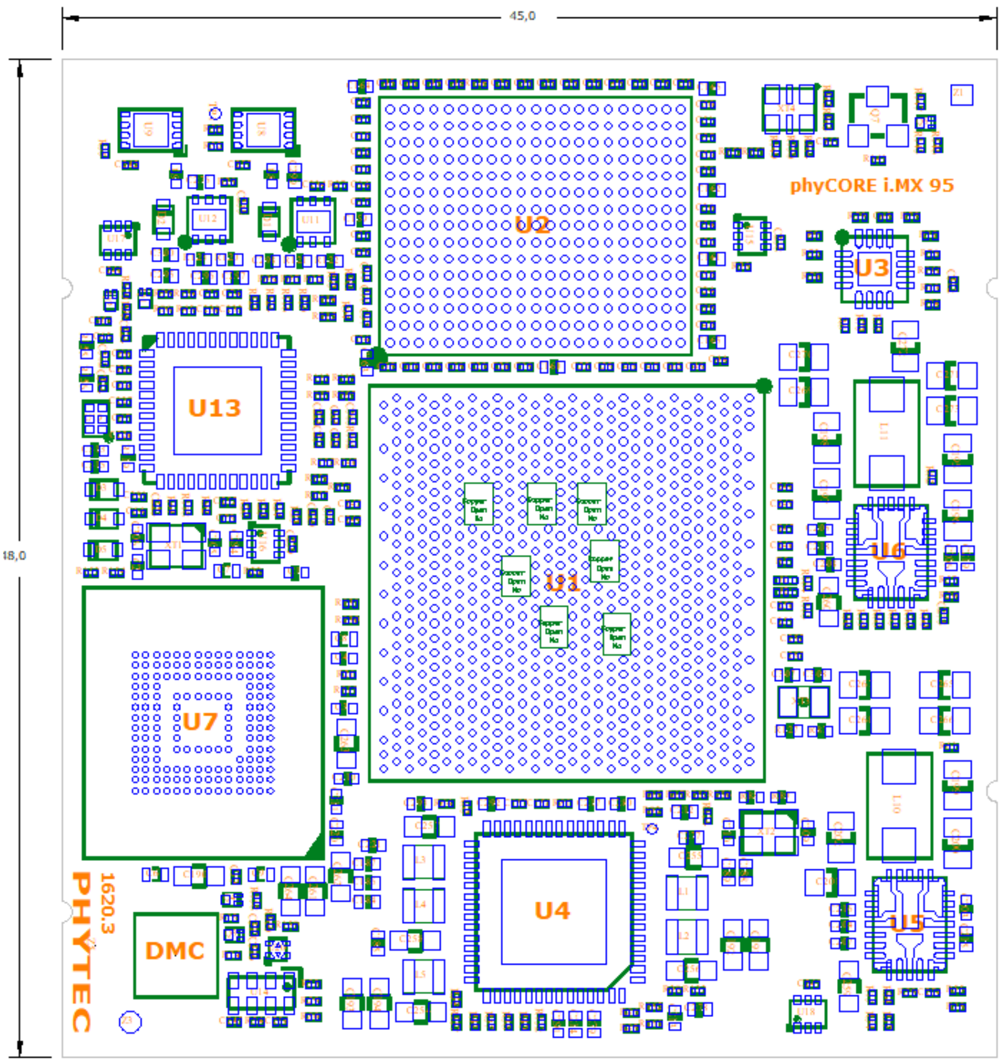


FIGURE 6: phyFLEX-i.MX 95 FPSC Footprint (top to bottom view; unit in mm)

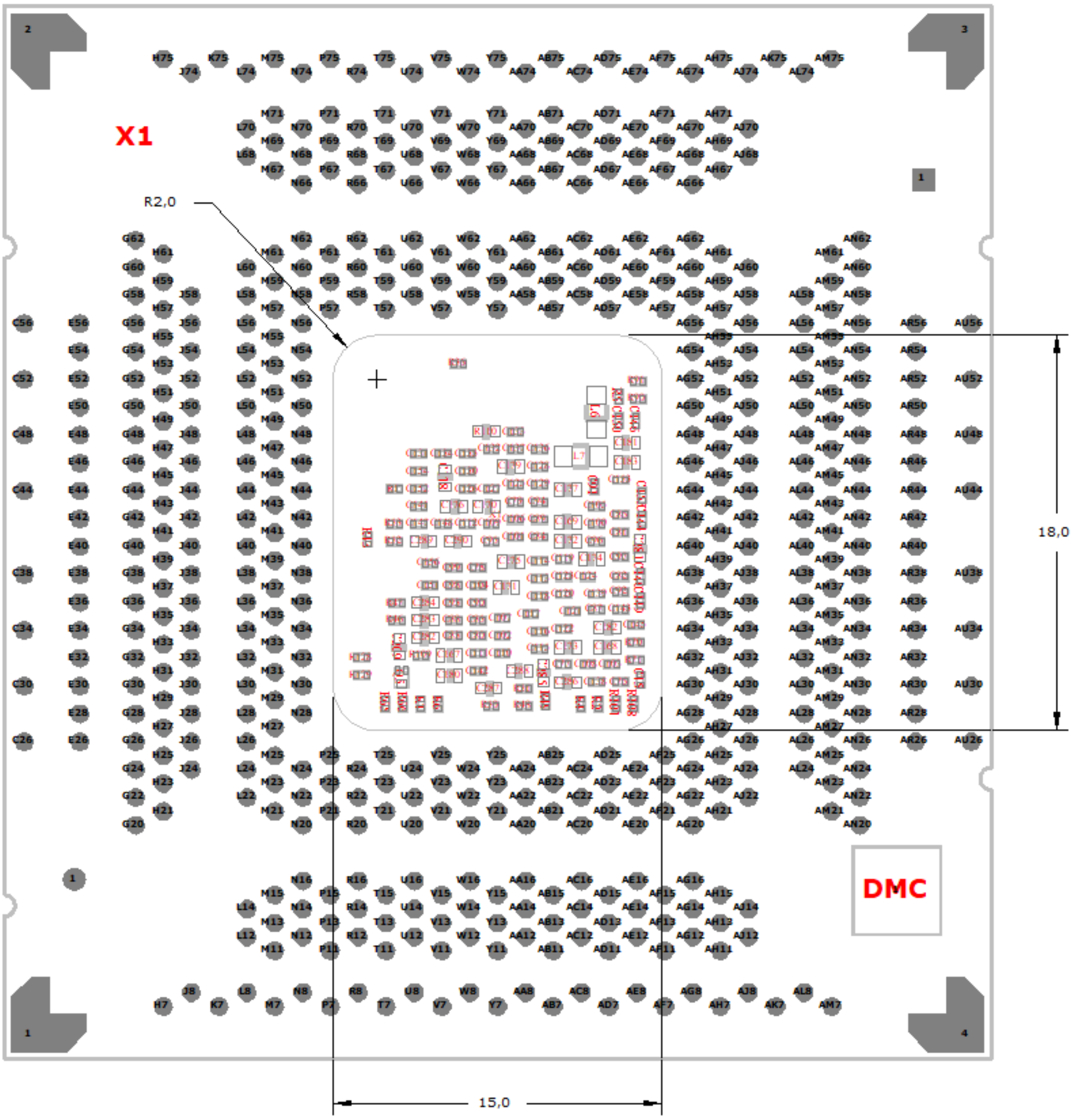


FIGURE 7: phyFLEX-i.MX 95 FPSC Footprint (bottom view top down; unit is mm)

> **Tip**
>
> For a downloadable version of the phyFLEX-i.MX 95 FPSC footprint, go to the download section of our product website: phyFLEX-i.MX 95 FPSC Download Page

Additional specifications:

Dimensions:	(48 x 45) mm
Weight:	ca. 17 g
Storage Temperature:	-40 to +85 °C
Operating Temperature:	i.MX 95 Product Temperature Grades

Humidity:	10 % - 90 % (non-condensing)
Operating Voltage:	4.75 V .. 5.25 V
Power Consumption:	phyFLEX-i.MX 95 FPSC Power Consumption

TABLE 35: Technical Specifications

These specifications describe the standard configuration of the phyFLEX-i.MX 95 FPSC as of the printing of this manual.

21.1 phyFLEX-i.MX 95 FPSC Power Consumption

The values listed in the table below are guidelines to determine the required dimensions of the power supply circuitry on a carrier board. They do not take application-specific load situations into account. These values have been generated by looking at the maximum power consumption measured using different load scenarios and adding a voltage source of 5.0 V. These values are based on internal PHYTEC testing. Customers need to consider their application power requirements to ensure they do not generate a load greater than the values listed here.

Required Supply Voltage	5.0 V
Ramp-Up Time (10 %-90 %)	100 µs to 10 ms
Allowed Tolerance of Supply Voltage	4.75 V .. 5.25 V (Abs. max 5.5 V)
Max. current consumption	4 A

TABLE 36: phyFLEX-i.MX 95 FPSC Power Consumption

For power measurement, a SOM (PCL-078) with 8 GB RAM, 32GB eMMC, ETH0, and a PIMX9596AVZXNAB was used together with PDx.x.x.

Warning

These tests are currently ongoing. Due to this, the table below has been intentionally left blank. These values will be available in future versions of this manual.

	Case 1	**Case 2**	**Case 3**	**Case 4**	**Case 5**	**Case 6**
eMMC-Boot system idle DVFS ondemand	TBD	TBD	TBD	TBD	TBD	TBD
iperf3 client eth0 (~900MBit/s)	TBD	TBD	TBD	TBD	TBD	TBD
CPU-Load (4x dd from /dev/urandom to /dev/null)	TBD	TBD	TBD	TBD	TBD	TBD
RAM-Load (memtester)	TBD	TBD	TBD	TBD	TBD	TBD
GPU-Load (qt5-opengles2-test)	TBD	TBD	TBD	TBD	TBD	TBD
VPU-Load (video 1080p)	TBD	TBD	TBD	TBD	TBD	TBD
Power Consumption [Watt]	TBD	TBD	TBD	TBD	TBD	TBD
CPU Thermal Zone 0 [°C]	TBD	TBD	TBD	TBD	TBD	TBD
CPU Thermal Zone 1 [°C]	TBD	TBD	TBD	TBD	TBD	TBD
CPU Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
RAM Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD

	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
Eth-PHY Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
PMIC Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
Ambient [°C]	TBD	TBD	TBD	TBD	TBD	TBD

TABLE 37: phyFLEX-i.MX 95 FPSC Power Consumption Test Scenarios

Additionally, there are some values that cannot be tested. Situations such as suspending to RAM, suspend freeze, and standby mode must be tested on a case-by-case basis to ensure the application's power consumption stays within the guidelines stated above.

> **Tip**
>
> For further information and assistance regarding your application's power consumption, please contact PHYTEC sales.

21.2 Product Temperature Grades

> **Warning**
>
> The right temperature grade for the module greatly depends on the use case. It is necessary to determine if the use case suits the temperature range of the chosen module (see below). A heat spreader can be used if temperature compensation is required.

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high-performance microcontrollers and other active parts, such as the ones described within this manual, are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about minimum or maximum ambient temperature ratings for the described SOM is not possible. However, the above-mentioned parts are available at different temperature qualification levels by the producers. We offer our SOMs in different configurations, making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration, we have categorized our SOMs into three temperature grades.

The table below describes these grades in detail. This table describes a set of components that, in combination, add up to a useful set of product options with different temperature grades. This enables us to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the minimum or maximum qualification levels are met within an application, the following conditions must be defined by considering the use case:

- Determined the processing load for the given software use case
- Maximum temperature ranges of components (table below)
- Power consumption resulting from a baseload and the calculating power required (in consideration of peak loads as well as time periods for system cooldown)
- Surrounding temperatures and existing airflow in case the system is mounted in a housing
- Heat resistance of the heat dissipation paths within the system, along with the considered usage of a heat spreader or a heat sink to optimize heat dissipation

Product Temperature Grade	Controller Range (Junction Temperature)	RAM (Case Temperature)	Other (Ambient)
I	Industrial: -40 °C to +105 °C	Industrial: -40 °C to +95 °C	Industrial: -40 °C to +85 °C
C	Commercial: 0 °C to +95 °C	Consumer: 0 °C to +95 °C	Consumer: 0 °C to +70 °C

TABLE 38: Product Temperature Grades

22 FPSC Footprint on the phyFLEX-i.MX 95 FPSC

For information on the footprint, mating baseboard footprint, numbering schema, etc., please refer to the corresponding FPSC Gamma Feature Set Specifications (LAN-118e.A6).

Pin numbering schema:

FPSC Gamma Feature Set Specifications (LAN118e.A6) - Pin Numbering

Mating FPSC Baseboard Footprint;

FPSC Gamma Feature Set Specifications (LAN118e.A6) - Baseboard

23 Interface Signal Trace Length

PHYTEC recommends a control delay and trace length of the high-speed interface signals. Signal delay and trace length of the high-speed interface signals routed on the front of the phyFLEX-i.MX 95 FPSC are listed in the following table. Take these values into consideration for the calculation of the overall delay and trace length budgets.

Signal	Delay [ps]	Length [mm]	Signal	Delay [ps]	Length [mm]
X_ENET1_RD0	393	56,53	X_MIPI_CSI1_CLK_N	207	29,86
X_ENET1_RD1	384	55,17	X_MIPI_CSI1_CLK_P	207	29,75
X_ENET1_RD2	381	54,91	X_MIPI_CSI1_D0_N	208	29,72
X_ENET1_RD3	393	56,45	X_MIPI_CSI1_D0_P	208	29,71
X_ENET1_RX_CTL	396	57,33	X_MIPI_CSI1_D1_N	208	29,72
X_ENET1_RXC	389	56,14	X_MIPI_CSI1_D1_P	208	29,70
X_ENET1_TD0	396	56,90	X_MIPI_CSI1_D2_N	208	29,78
X_ENET1_TD1	410	58,71	X_MIPI_CSI1_D2_P	208	29,68
X_ENET1_TD2	391	56,34	X_MIPI_CSI1_D3_N	208	29,74
X_ENET1_TD3	406	58,11	X_MIPI_CSI1_D3_P	208	29,72
X_ENET1_TX_CTL	402	57,57	X_MIPI_DSICSI1_CLK_N	267	38,22
X_ENET1_TXC	393	57,10	X_MIPI_DSICSI1_CLK_P	267	38,14

X_ETH_RX0_N	164	23,49	X_MIPI_DSICSI1_D0_N	267	38,19
X_ETH_RX0_P	164	23,50	X_MIPI_DSICSI1_D0_P	267	38,16
X_ETH_TX0_N	165	23,67	X_MIPI_DSICSI1_D1_N	266	38,13
X_ETH_TX0_P	165	23,70	X_MIPI_DSICSI1_D1_P	266	38,11
X_ETH2_A_N	283	40,64	X_MIPI_DSICSI1_D2_N	267	38,32
X_ETH2_A_P	284	40,68	X_MIPI_DSICSI1_D2_P	266	38,31
X_ETH2_B_N	283	40,68	X_MIPI_DSICSI1_D3_N	266	38,14
X_ETH2_B_P	284	40,64	X_MIPI_DSICSI1_D3_P	266	38,12
X_ETH2_C_N	285	40,77	X_PCIE1_CLK_N	248	35,65
X_ETH2_C_P	285	40,78	X_PCIE1_CLK_P	249	35,61
X_ETH2_D_N	284	40,64	X_PCIE1_RX0_N	223	31,84
X_ETH2_D_P	283	40,68	X_PCIE1_RX0_P	223	31,92
X_LVDS0_CLK_N	197	28,45	X_PCIE1_TX0_N	222	31,77

X_LVDS0_CLK_P	197	28,51	X_PCIE1_TX0_P	223	31,90
X_LVDS0_D0_N	197	28,12	X_PCIE2_REF_PAD_CLK_N	143	20,76
X_LVDS0_D0_P	196	28,18	X_PCIE2_REF_PAD_CLK_P	143	20,82
X_LVDS0_D1_N	197	28,29	X_PCIE2_RX0_N	142	20,43
X_LVDS0_D1_P	198	28,32	X_PCIE2_RX0_P	141	20,42
X_LVDS0_D2_N	196	28,02	X_PCIE2_TX0_N	142	20,74
X_LVDS0_D2_P	196	27,96	X_PCIE2_TX0_P	142	20,85
X_LVDS0_D3_N	197	28,61	X_SD3_CLK	304	43,76
X_LVDS0_D3_P	197	28,65	X_SD3_CMD	306	43,84
X_LVDS1_CLK_N	104	14,97	X_SD3_DATA0	306	43,83
X_LVDS1_CLK_P	104	14,98	X_SD3_DATA1	306	43,74
X_LVDS1_D0_N	105	15,18	X_SD3_DATA2	312	44,64
X_LVDS1_D0_P	106	15,19	X_SD3_DATA3	308	44,07

X_LVDS1_D1_N	105	15,27	X_USB1_D_N	223	33,20
X_LVDS1_D1_P	105	15,26	X_USB1_D_P	223	33,23
X_LVDS1_D2_N	105	15,08	X_USB1_RX0_N	311	44,60
X_LVDS1_D2_P	105	15,11	X_USB1_RX0_P	310	44,53
X_LVDS1_D3_N	104	15,32	X_USB1_RX1_N	311	44,92
X_LVDS1_D3_P	104	15,31	X_USB1_RX1_P	310	44,92
X_SD2_CLK	205	31,10	X_USB1_TX0_N	336	48,19
X_SD2_CMD	207	31,19	X_USB1_TX0_P	336	48,24
X_SD2_DATA0	205	31,59	X_USB1_TX1_N	336	48,14
X_SD2_DATA1	203	31,14	X_USB1_TX1_P	336	48,20
X_SD2_DATA2	212	32,02	X_USB2_D_N	260	38,74
X_SD2_DATA3	212	32,10	X_USB2_D_P	261	38,94

TABLE 39: Interface Signal Trace Length

24 Hints for Integrating and Handling the phyFLEX-i.MX 95 FPSC

24.1 Integrating the phyFLEX-i.MX 95 FPSC

Besides this hardware manual, more information is available to facilitate the integration of the phyFLEX-i.MX 95 FPSC into customer applications.

1. The design of the Libra Development Board can be used as a reference for any customer application.
2. Many answers to common questions can be found at: https://www.phytec.de/produkte/system-on-modules/phyflex-imx-95-fpsc/#downloads/
3. The link “Carrier Board” within the category Dimensional Drawing leads to the layout data phyFLEX-i.MX 95 FPSC Footprint. It is available in different file formats. The use of this data allows the user to integrate the phyFLEX-i.MX 95 FPSC SOM as a single component in their design.
4. Different support packages are available for support in all stages of embedded development. Please visit https://www.phytec.de/support/support-pakete/ or https://www.phytec.eu/support/support-packages/ or contact our sales team for more details.

24.2 Handling the phyFLEX-i.MX 95 FPSC

24.2.1 phyFLEX Module Modifications

The removal of various components, such as the microcontroller or the standard quartz, is not advisable, given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered components need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, a hot air rework station, or other desoldering method is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

Warning

If any modifications to the module are performed, regardless of their nature, the manufacturer's guarantee may be null and void.

24.2.2 Integrating the phyFLEX into a Target Application

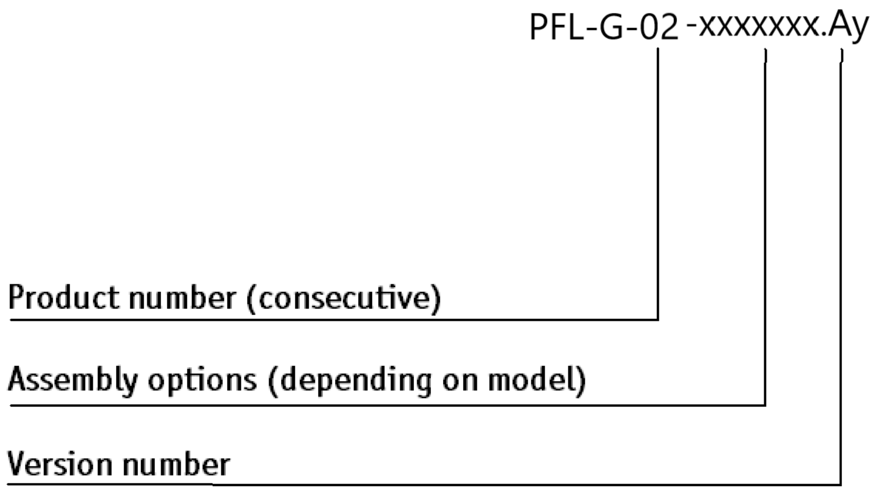
Successful integration in the user target circuitry greatly depends on adherence to the layout design rules for the GND connections of the phyFLEX module. For maximum EMI performance, PHYTEC recommends, as a general design rule, connecting all GND pins to a solid ground plane. At a minimum, all GND pin neighboring signals that are being used in the application circuitry should be connected to GND.

Tip

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyFLEX-i.MX 95 FPSC on the Libra Development Board. Be aware that not all components need to be considered when designing your own carrier board.

24.2.3 Ordering Information

The part numbering of the phyFLEX PFL-G-02 has the following structure:



24.2.4 Product-Specific Information and Technical Support

In order to receive product-specific information on all future changes and updates, we recommend registering at:
http://www.phytec.de/support/registrierung.html or http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our website, which provides product-specific information, such as errata sheets, application notes, FAQs, etc.
https://www.phytec.de/produkte/system-on-modules/phyflex-imx-95-fpsc/
or
https://www.phytec.eu/en/produkte/system-on-modules/phyflex-imx-95-fpsc/

25 phyFLEX-i.MX 95 FPSC on the Libra Development Board

25.1 Hardware Overview

The Libra Development Board for phyFLEX-i.MX 95 FPSC is a low-cost, feature-rich software development platform supporting the NXP Semiconductors i.MX 95 microcontroller. Due to numerous standard interfaces, the Libra Development Board i.MX 95 can serve as the bedrock for any application. At the core of the Libra Development Board is the PFL-G-02/phyFLEX-i.MX 95 FPSC System On Module (SOM) containing the processor, LPDDR5 RAM, eMMC Flash, power regulation, supervision, transceivers, and other core functions required to support the i.MX 95 processor. Surrounding the SOM is the PBA-BG-41/Libra Development Board carrier board, adding power input, buttons, connectors, signal breakout, and Ethernet connectivity, along with other peripherals.

25.2 Libra Development Board Concept

PHYTEC phyFLEX carrier boards are fully equipped with all the mechanical and electrical components necessary for a fast, secure start-up. Subsequent communication to and programming of the applicable PHYTEC System on Modules (SOM) is made easy. phyFLEX carrier boards are designed for evaluation, testing, and prototyping of PHYTEC System on Modules in laboratory environments prior to their use in customer-designed applications.

This modular development platform concept includes the following components:

- The **phyFLEX-i.MX 95 FPSC Module** populated with the i.MX 95 microcontroller and all applicable SOM circuitry such as LPDDR5 SDRAM, eMMC-Flash, Ethernet-PHY, PMIC, etc.
- The **Libra Development Board Carrier Board** offers all essential components and connectors for a start-up, including a power supply for 24 V input voltage and interface connectors such as **HDMI**, **USB**, and **Ethernet**, which enable the use of the SOM's interfaces with a standard cable.

The carrier board can also serve as a reference design for developing custom target hardware in which the phyFLEX SOM can be deployed. Carrier board schematics are available under a Non-Disclosure Agreement (NDA). The reuse of carrier board circuitry enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

SBCplus Concept

The SBCplus concept was developed to meet the many small differences in customer requirements with little development effort. This greatly reduces the time-to-market. The core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a large number of function blocks (so-called "building blocks") that are continuously being refined and updated.

Recombining these function blocks allows PHYTEC to develop a customer-specific SBC within a short time. We are able to deliver production-ready custom single-board computers within a few weeks at very low costs. The already developed SBCs, such as the Libra Development Board, each represent a combination of different customer wishes. This means all necessary interfaces are already available on the standard versions, allowing PHYTEC SBCs to be integrated into a large number of applications without modification.

For any necessary detail adjustment, extension connectors are available, which enable a wide variety of functions to be added.

> **Tip**
>
> For further information, please contact PHYTEC sales.

25.3 Libra Development Board Features

supports the following features:
[1]

- Developed under PHYTEC's FPSC concept
- Implements FPSC Featureset Gamma Rev. 1
- Populated with PHYTEC's phyFLEX FPSC SoM (see phyFLEX SoM Feature List)
- Dimensions of 200 mm × 130 mm
- Boot from eMMC, SD Card, or over USB with the Serial Downloader
- 24 V input voltage
- USB-C input power
- 64 MByte QSPI-NOR
- 2 kBit EEPROM
- 2x RJ45 jack for 10/100/1000 Mbps Ethernet
- 1x SFP+ receptacle for 10/100/1000/2500/5000/10000 Mbps Ethernet
- 1x Dual USB 3.0 Type-A connector (Actual USB speed depends on mounted SoM)
- 1x USB-C 3.2 interface connected to phyFLEX FPSC SoM (Actual USB speed depends on mounted SoM)
- 1x Secure Digital / MultiMedia Memory Card interface brought out to a Micro SD-Card receptacle
- 1x HDMI interface brought out to a standard Type-A connector (HDMI availability depends on mounted SoM)
- 1x MIPI-DSI brought out to be used with PEB-AV-12 (MIPI-DSI availability depends on the mounted SoM)
- 2x MIPI-CSI-2 camera interfaces brought out as a phyCAM-M interface (MIPI-DSI availability depends on mounted SoM)
- 1x M.2 Key-E connector with (Key-E interface availability depends on the mounted SoM):
  - 1x PCIe
  - 1x SDIO
  - 1x UART with flow-control
  - 1x I2C
  - 1x USB 2.0 (no protective circuitry on carrier board)
- 1x M.2 Key-M connector with (Key-M interface availability depends on the mounted SoM):
  - 1x PCIe
  - 1x I2C
- RS-232 or RS-485 available at 2x5 pin header 2.54 mm RS-232 (up to Mbps) including a handshake and RS-485 Half-Duplex (up to Mbps)
- Up to 8 ADC input pins (Number of useable ADC input signals depends on the mounted SoM)
- 8-Bit SPI-ADC
- Reset button
- ON/OFF button
- 1x multicolor LED
- 1x PHYTEC Audio/Video connector for PEB-AV-10/13 with:
  - 1x LVDS (LVDS interface availability depends on the mounted SoM)
  - 1x Synchronous Audio Interface
  - 1x USB 2.0 (no protective circuitry on carrier board)
- SAI Audio brought out via an A/V connector
- 1x JTAG at 2x10 pin socket 2.54 mm
- Goldcap backup supply for SoM RTC
- On-board measurement of SoM Power Consumption
- I2C/I3C Temperature Sensor (Temperature Sensor availability depends on I2C capabilities of mounted SoM)
- Trusted Platform Module (TPM)

1. PCM-937-L

25.4 Block Diagram

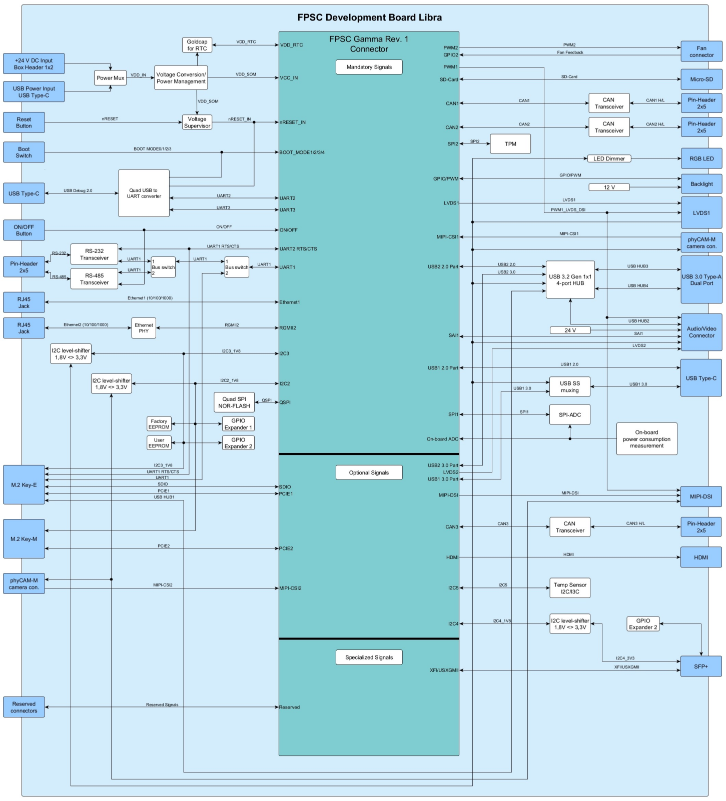


FIGURE 8: Libra Development Board Block Diagram

25.5 SoM Feature List on the Libra Development Board

There are several SoMs that can be used with the Libra Development Board. Below is a comprehensive list of features that each SoM contains and can be used with the Libra Development Board. For more information, please contact your PHYTEC representative (Contact Information).

		phyFLEX-i.MX 95	**phyFLEX-i.MX 8M Plus**	**phyFLEX-STM32MP 2**	**phyFLEX-AM62Lx**	**phyFLEX-i.MX 93**	**phyFLEX-i.MX 91**	**phyFLEXi.MX952**	**phyFLEXSL2610**
	Featureset	**Gamma**	**Gamma**	**Gamma**	**Gamma**	**Gamma**	**Gamma**	**Gamma**	**GammaLite**
	Subclass	**1 / 2 / 3**	**1 / 2 / 3**	**1 / 2 / 3**	**2 / 3**	**1 / 2 / 3**	**3**	**1 / 2 / 3**	
Mandatory Signals	RGMII	x	x	x	x	x	x	x	x
	Ethernet	x	x	x	x	x	x	x	x
	USB 2.x	x	x	x	x	x	x	x	x
	USB 2.x	x	x	x	x	x	x	x	NA
	LVDS	x	x	x	x	x	NA	x	NA

	MIPI-CSI-2 (2 or 4 lanes)	x	x	x	NA	x	NA	x	x (2 Lanes)
	SD Card	x	x	x	x	x	x	x	x
	QSPI	x	x	x	x	x	x	x	x
	CAN(-FD) (2)	x	x	x	x	x	x	x	x
	UART+Flow (2)	x	x	x	x	x	x	x	x
	UART	x	x	x	x	x	x	x	x
	SPI+CS (2)	x	x	x	x	x	x	x	x
	I2C (2)	x	x	x	x	x	x	x	x
	PWM (2)	x	x	x	x	x	x	x	x
	SAI 2-Lane	x	x	x	x	x	x	x	x (w/o TDM)
	JTAG	x	x	x	x	x	x	x	x
	PWR_IN	x	x	x	x	x	x	x	x
	Control/ Misc	x	x	x	x	x	x	x	x
	GPIO (4)	x	x	x	x	x	x	x	x

Optional Signals	USB 3.x (1-2)	1	2	1	0	0	0	0	0
	LVDS	1	1	1	0	0	0	1	0
	MIPI-DSI	1	1	1	1	1	0	1	1
	MIPI-CSI (2 or 4 lanes)	1	1	0	0	0	0	1 (2 Lanes)	0
	HDMI/ eARC	0	1	0	0	0	0	0	0
	PCIe 2-Lane (1-2)	2	1	1	0	0	0	1	0
	CAN(-FD)	0	0	0	1	0	0	0	0
	SDIO4	1	1	1	1	0	0	1	1
	SPI+CS	1	1	1	1	0	0	1	0
	I2C (1-2)	1	1	2	1	0	0	2	1
	PWM (1-2)	2	2	2	2	0	0	2	2
	ADC (1-8)	8	0	4 (5)	4	4	4	8	8
	GPIO (1-3)	3	3	3	3	0	0	3	3
Specialized Signals	10G Ethernet	1	0	0	0	0	0	0	0
	USB 3 SS Signals	1	0	1 (or PCIe)	0	0	0	0	0
	GPIO	1	4	4	4	0	0	7	5

TABLE 40: FPSC Gamma Feature Set Signals

25.6 **Temperature Range**

Most components on the Libra Development Board have an operating temperature range of -40 °C to 85 °C. The following components are the exception:

BOM No.	**Component Description**	**Temperature Range**	**Advice**
C111	Double-layer capacitor for RTC Backup	-25 °C to 70 °C	
X37	HDMI Connector	-25 °C to 85 °C	There is no replacement available
X43	LVDS1 Data Connector	-35 °C to 85 °C	There is no replacement available
X44	LVDS1 Backlight Connector	-25 °C to 85 °C	There is no replacement available
X68	Fan Connector	-35 °C to 85 °C	
X60	Micro SD-Card Slot	-25 °C to 85 °C	The SD-Card slot can be used in the range of -40 °C to 85 °C without mechanical changes

TABLE 41: Libra Development Board Component Temperature Range

For this reason, the operation temperature range for the kit variant is: -25 °C to 70 °C. The storage temperature range is -40 °C to 85 °C.

25.7 Mechanical Dimensions

For detailed dimensions, refer to the provided CAD data (e.g., DXF file) in the download section of our specific FPSC SoMs:

- phyFLEX-i.MX 95 FPSC
- phyFLEX-i.MX 8M Plus FPSC
- phyFLEX-STM32MP2x FPSC
- phyFLEX-AM62Lx FPSC
- phyFLEX-AM62P FPSC (COMING SOON)

26 Libra Development Board Components

Tip

For high-resolution pictures of the Libra Development Board, please go to the download section of our specific FPSC SoMs.

Note

For easy reference, Pin 1 for each component has been highlighted.

26.1 Libra Development Board Component Placement Diagram

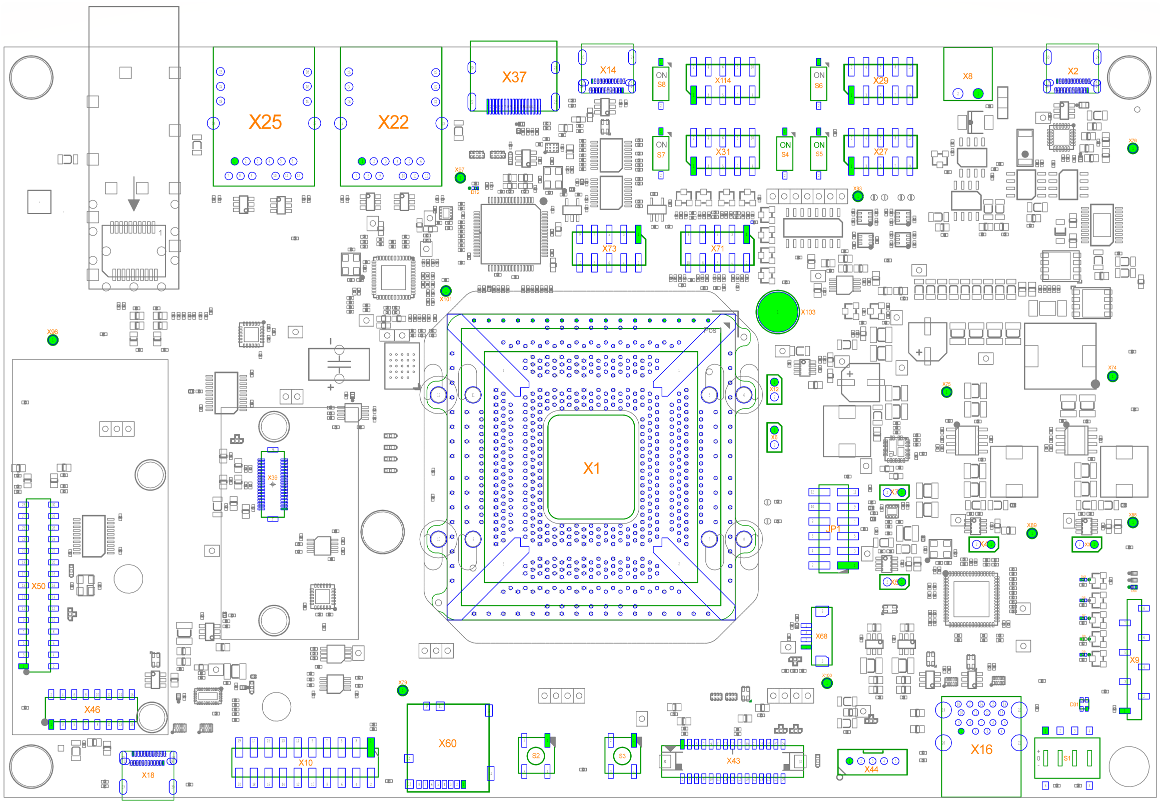


FIGURE 9: Libra Development Board Components (Top)

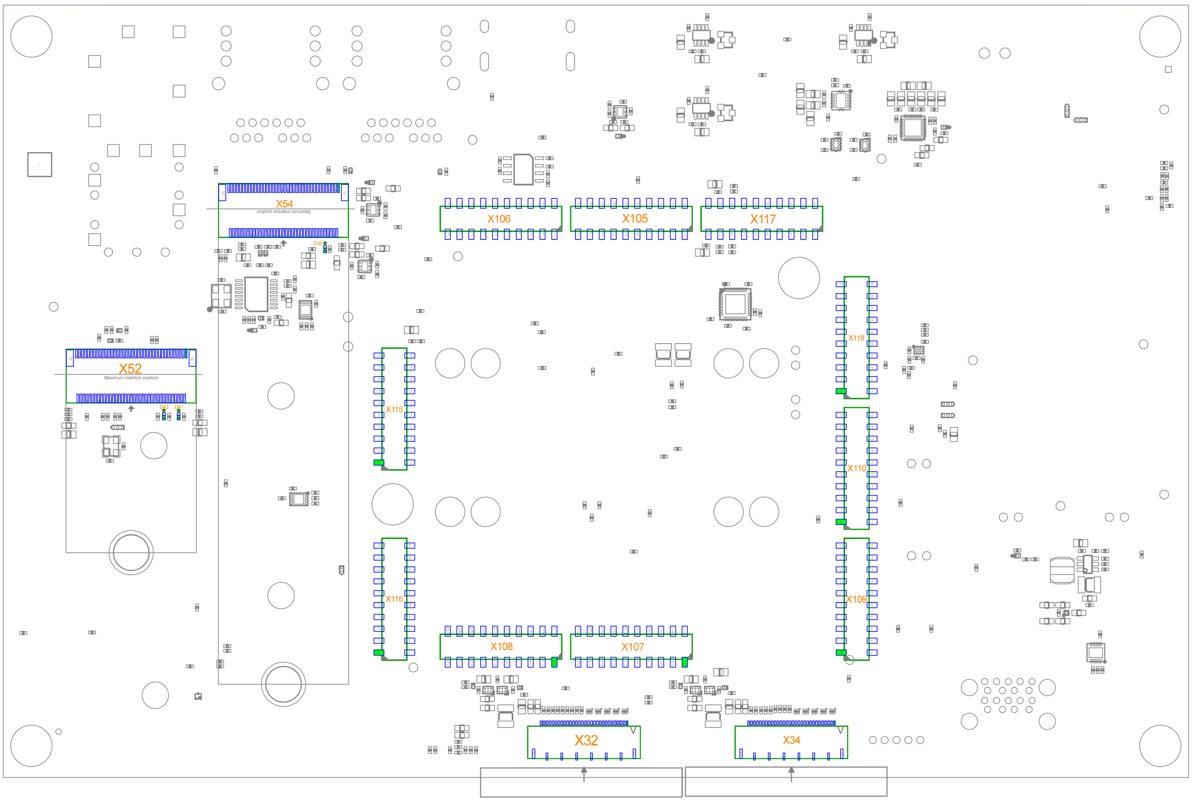


FIGURE 10: Libra Development Board Components (Bottom)

26.2 Libra Development Board Component Overview

The Libra Development Board features many interfaces and is equipped with the components listed in the table Connectors and Pin Header. For a more detailed description of each component, refer to the appropriate section listed in the table below. Libra Development Board Components (Top) and Libra Development Board Components (Bottom) highlight the location of each component for easy identification.

26.2.1 Connectors and Pin Header

The table below lists all available connectors on the Libra Development Board.

Reference Designator	Description	Section
X1	SoM FPSC solder connection	phyFLEX Connector (X1)
X2	Carrier board power in USB-C	Power Supply (X2/X8)
X3	VDD_5V0 current amp header 2,54 mm (not mounted)	
X4	VDD_3V3 current amp header 2,54 mm(not mounted)	

Reference Designator	Description	Section
X5	VDD_1V8 current amp header 2,54 mm(not mounted)	
X6	SoM 3,3 V output header 2,54 mm(not mounted)	
X7	SoM 1,8 V output header 2,54 mm (not mounted)	
X8	Carrier board power in a 2-pin connector	Power Supply (X2/X8)
X9	Boot Mode manipulation header	Boot Header (X9)
X10	JTAG header 2,54 mm voltage level 1,8 V	JTAG (X10)
X12	SoM input current amp header 2,54 mm(not mounted)	SoM Input Current Amp Header (X12)
X14	USB-C-Debug	USB Debug (X14)
X16	Dual USB-A 3.0	USB Type-A 3.0 Interface (X16)
X18	Dual-role USB-C 3.2	USB-C 3.2 GEN 1 Interface (X18)
X22	Ethernet Gigabit RJ-45	Ethernet (X22/X25)
X25	Ethernet Gigabit RJ-45	
X27	RS232/RS485 10-pin header 2,54 mm	RS-232/RS-485 (X27)
X29	CAN-FD1 10-pin header 2,54 mm	CAN FD (X29/X31/X114)
X31	CAN-FD2 10-pin header 2,54 mm	
X114	CAN-FD3 10-pin header 2,54 mm	

Reference Designator	Description	Section
X32	phyCAM-M CSI1	phyCAM-M MIPI CSI Camera Connectors (X32/34)
X34	phyCAM-M CSI2	
X37	HDMI	HDMI (X37)
X39	MIPI-DSI 36-pin board-to-board	MIPI-DSI (X39)
X43	LVDS1 data connector	LVDS1 (X43/X44)
X44	LVDS1 backlight connector	
X46	LVDS2 AV-Connector display data 16-pin header 2 mm	Audio/Video (LVDS2/SAI1)
X50	AV-Connector audio + control 30-pin header 2 mm	
X52	M.2 Key-E	M.2 Key-E (X52)
X54	M.2 Key-M	M.2 Key-M (X54)
X60	Micro SD-Card receptacle	Secure Digital Memory Card / MultiMedia Card (X60)
X68	Fan Connector 4-pin	Fan (X68)
X71	SPI-ADC input 10-pin header 2,54 mm	SPI-ADC (X71)
X73	ADC input 10-pin header 2,54 mm	ADC (X73)
X74, X75, X76, X79, X88, X89, X92, X93, X96, X97, X100, X101	GND Stud	
X105-X110, X115-X118	FPSC reserved a 20-pin socket 2 mm	

TABLE 42: Libra Development Board Connectors and Pin Headers

> **Warning**
>
> Ensure that all module connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

26.2.2 LEDs

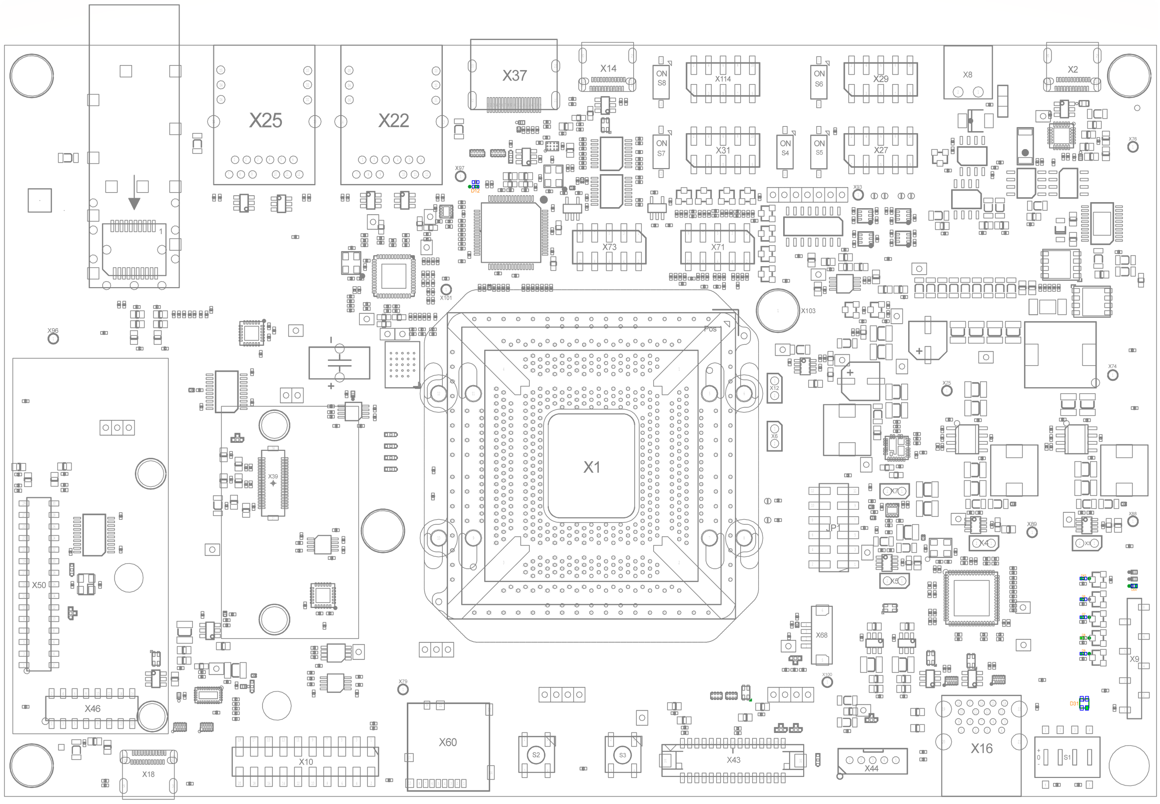


FIGURE 11: Libra Development Board LEDs (Top)

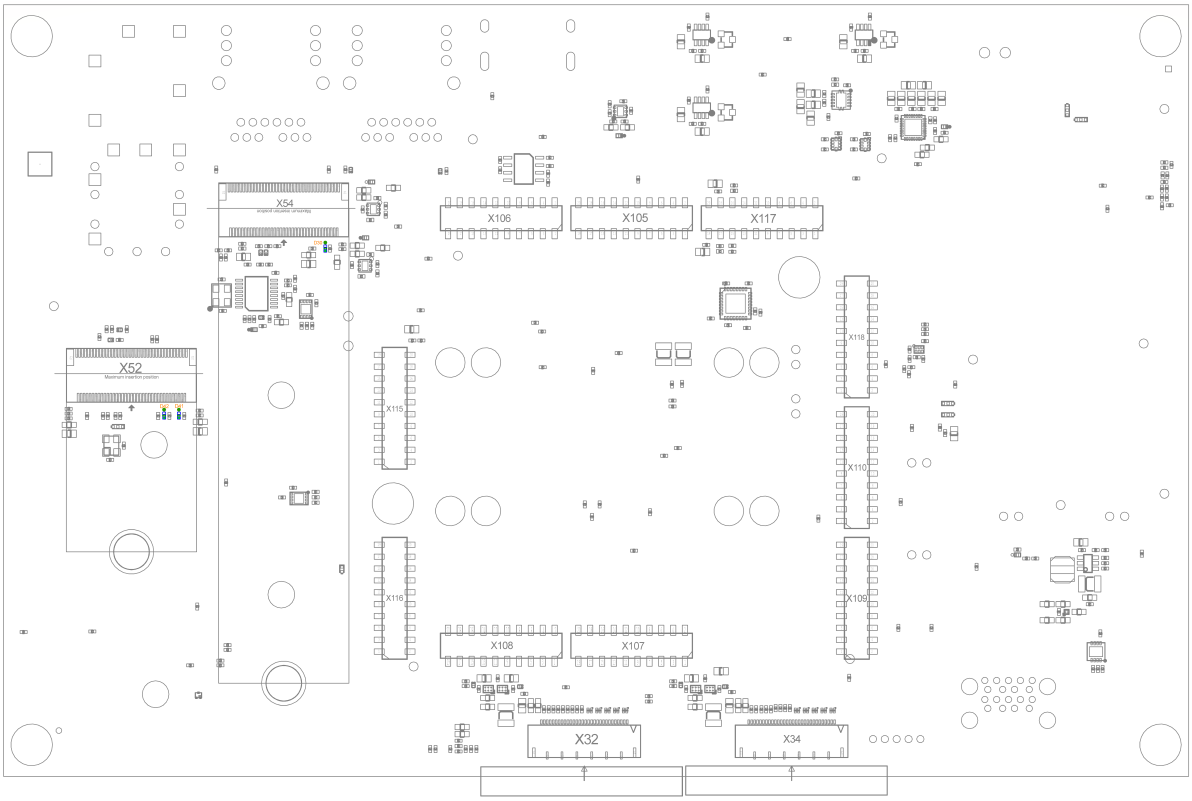


FIGURE 12: Libra Development Board LEDs (Bottom)

The Libra Development Board is populated with 7 LEDs. Libra Development Board Components (Top) and Libra Development Board Components (Bottom) show the location of the LEDs. Their functions are listed in the table below:

LED	Color	Description	Section
D6	Blue	VDD_5V0 good indicator	
D7	Blue	VDD_3V3 good indicator	
D8	Blue	VDD_1V8 good indicator	
D9	Blue	VDD_SOM good indicator	
D12	Red	Debug USB-C VBUS good indicator	
D30	Yellow	M.2 SSD activity indicator	
D31	RGB	Multi-color LED user-controllable	Multicolor (RGB) LED (D31)
D41	Yellow	M.2 status LED 1#	

LED	Color	Description	Section
D42	Yellow	M.2 status LED 2#	
D43	Blue	VDD_12V0 good indicator	

TABLE 43: Libra Development Board LED Descriptions

26.2.3 Switches and Buttons

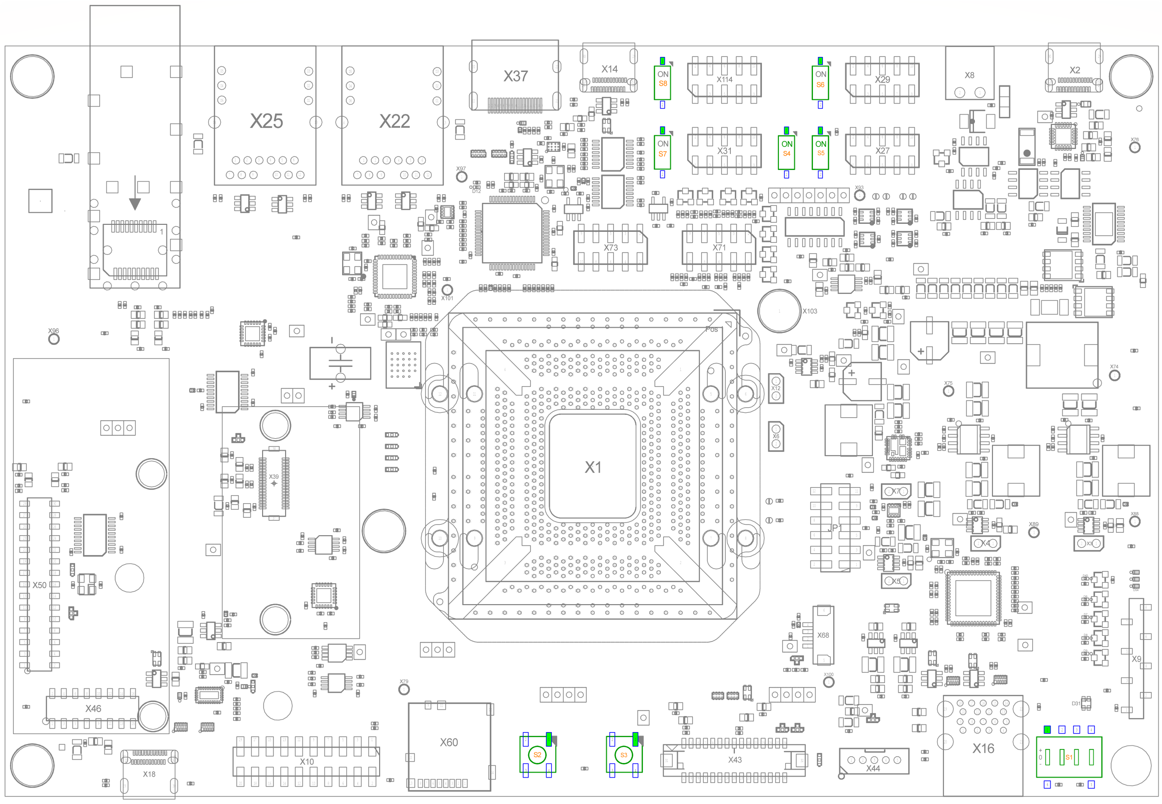


FIGURE 13: Libra Development Board Switch Locations

The Libra Development Board is populated with multiple switches and buttons. The table below shows their functions:

Switch	Description	Section
S1	4-port tri-state Boot Mode switch	Boot Switch (S1)
S2	Reset push button	System Reset Button (S2)
S3	ON/OFF push button	System ON/OFF Button (S3)
S4	RS485 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	
S5	UART1 target switch ON: UART1 is converted to RS232 OFF: UART1 is converted to RS485	

Switch	Description	Section
S6	CAN FD1 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	
S7	CAN FD2 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	
S8	CAN FD3 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	

TABLE 44: Libra Development Board Switches

26.2.4 Jumpers

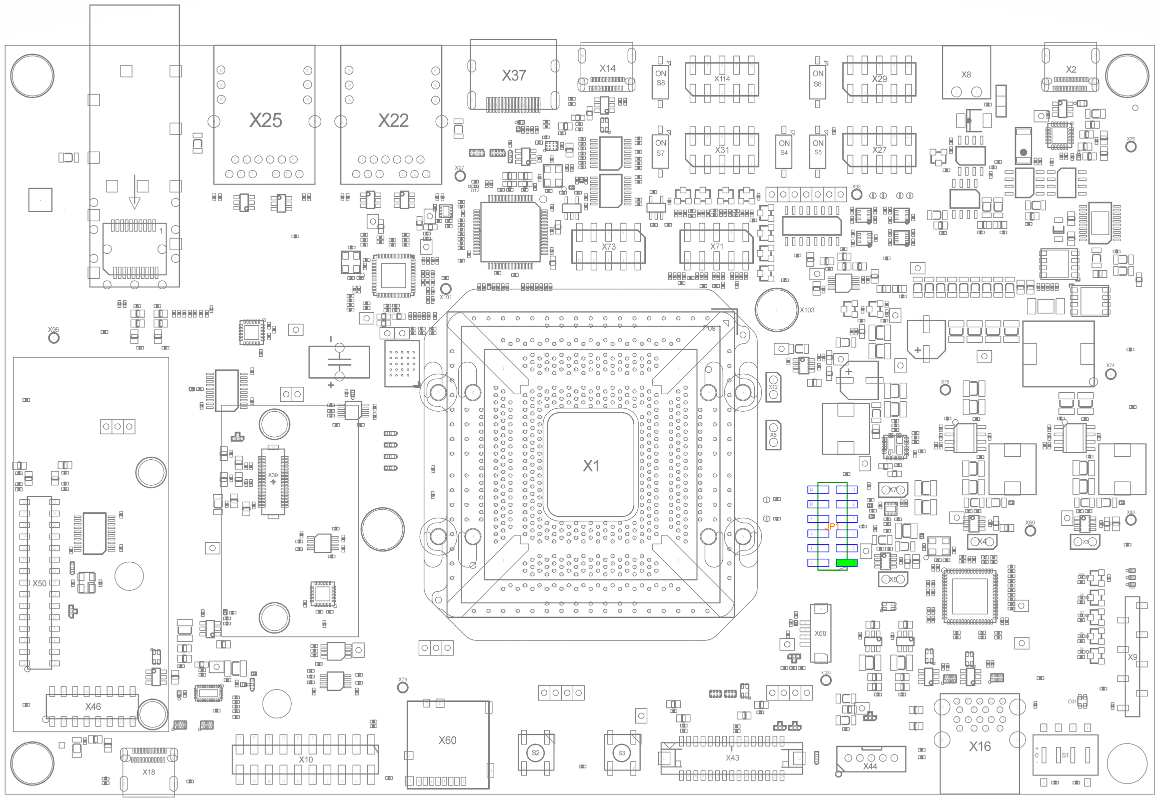


FIGURE 14: Jumper (JP1)

The Libra Development Board comes pre-configured with several removable jumpers (JP) and solder jumpers (J). These jumpers enable the flexible configuration of a limited number of features for development purposes.

> **Warning**
>
> Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Only the removable jumper (JP) is described in this section. Contact our sales team if you need jumper configurations different from the default configuration.

The function of the removable jumper on the Libra Development Board is shown below. More detailed information can be found in the appropriate section.

Jumper	Position	Default	Description	Section
JP1		1+2 3+4 5+6 9+10	UART3_RXD - USB Debug 1 UART3_TXD - USB Debug 1 UART2_RXD - USB Debug 2 UART2_TXD - USB Debug 2	

TABLE 45: Libra Development Board Jumper Settings

26.3 Libra Development Board Component Detail

This section provides a more detailed look at the Libra Development Board components. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

> **Tip**
>
> Where possible, we also provide useful information regarding design considerations for components. This can be used if you plan to design your own carrier board.

26.3.1 phyFLEX Connector (X1)

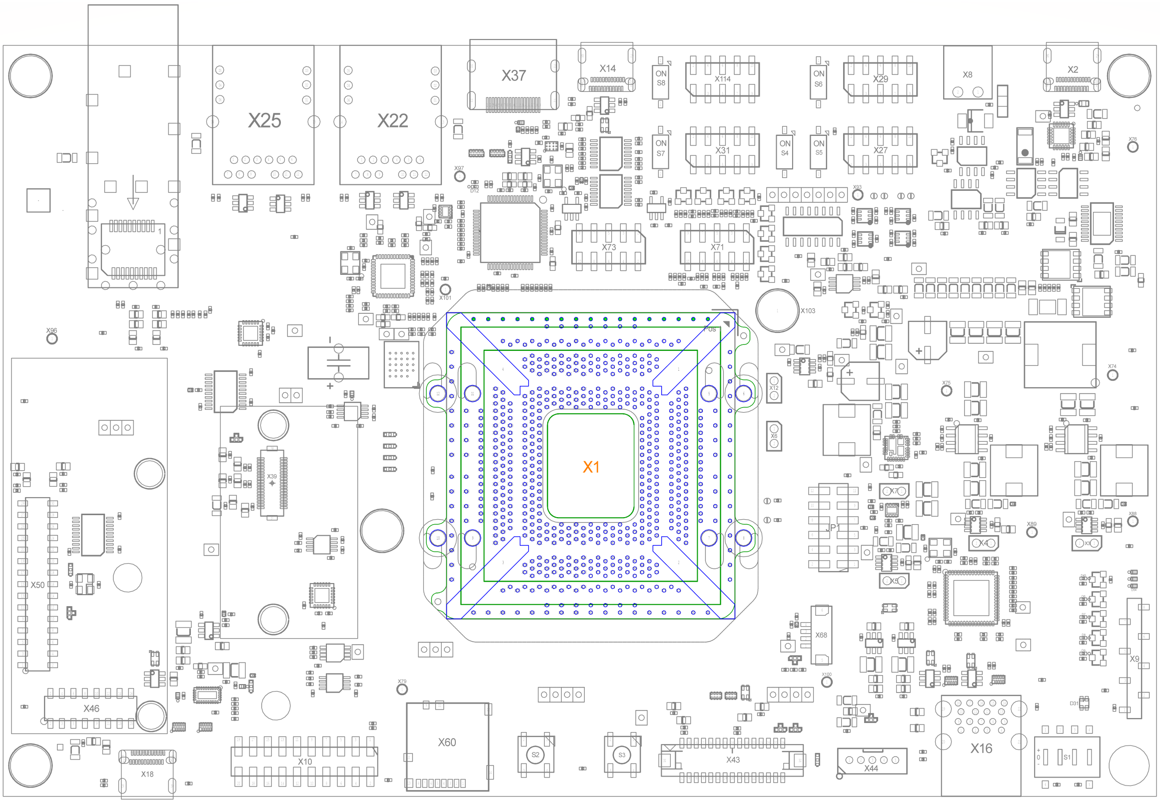


FIGURE 15: phyFLEX Connector (X1)

26.3.2 Power Supply (X2/X8)

> **Warning**
>
> Do not change modules or jumper settings while the Libra Development Board is supplied with power!

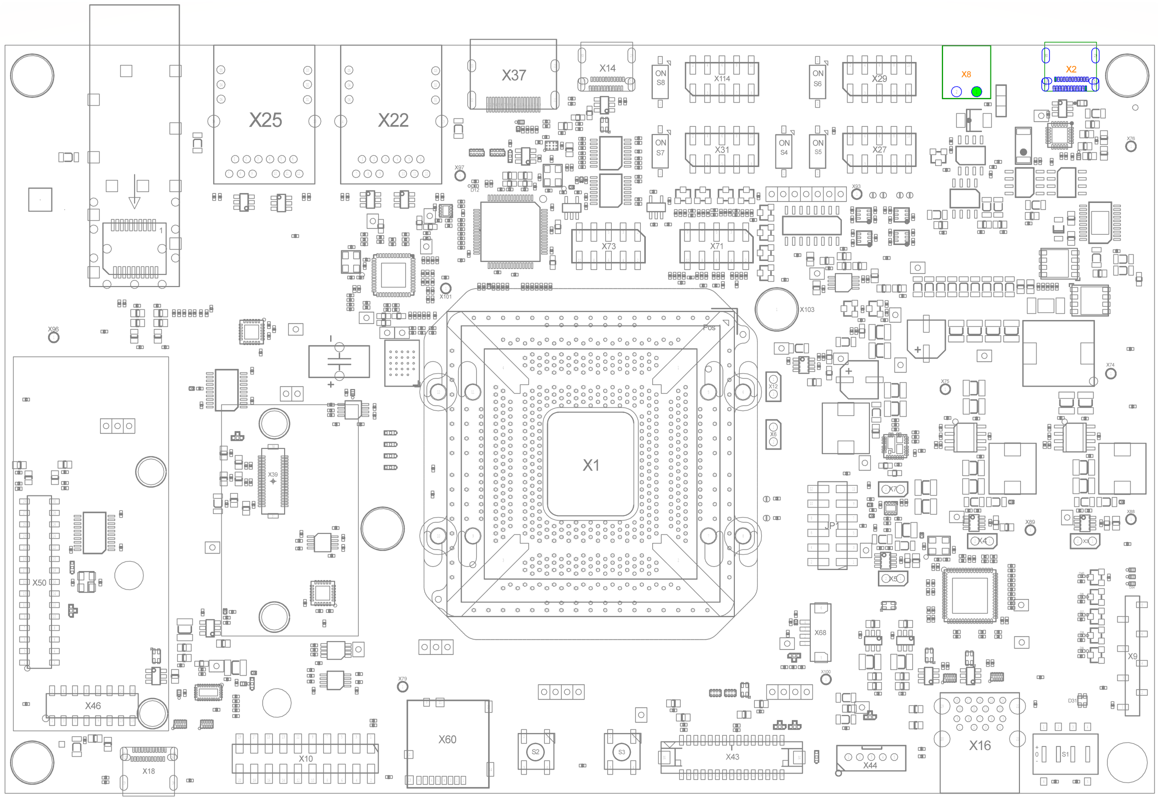


FIGURE 16: Power Supply Connectors (X2/X8)

The Libra Development Board can be powered either by a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X8) or by a USB Power Delivery Supply (X2).

> **Warning**
>
> Do not power the Libra Development Board via X2 and X8 at the same time!
> Do not connect a USB device that is not a certified USB Power Delivery supply to X8!

The Libra Development Board is available with one power supply connector, a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X8) suitable for a single 24 V supply voltage. The required capacity for all power supply solutions depends on the specific configuration of the phyFLEX-SoM mounted on the Libra Development Board, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board.

The permissible input voltage is 24 V DC if your Development Board is equipped with a 2-pole Phoenix Contact MINI COMBICON base strip. A 24 V power supply capable of providing at least 3.5 A is recommended to power the board via the 2-pole base strip. The pin assignment for power supply connector X8:

Interface Pin #	Signal	Description
1	VDD_IN_PWR_CON	24 V ± 10%, 85 W
2	GND	Ground

TABLE 46: X8 Pin Assignment

26.3.2.1 USB Power Delivery Connector (X2)

The Libra Development Board can be powered by a USB Power Delivery Supply. The Libra Development Board provides the needed voltage and current from the connected supply and enables the on-board voltages. A 85 W USB-PD supply is recommended to power the Libra Development Board.

> **Note**
>
> Please note that connector X2 is only usable as a power supply input. It doesn't offer any USB communication interface functionality. Only use a certified USB Power Delivery supply.

26.3.2.2 RTC Backup Supply

The Libra Development Board has a double-layer capacitor equipped to back up the VDD_RTC rail of the phyFLEX FPSC SoM. The capacitor is also charged through a diode circuit from VDD_3V3. The mounted 330 mF capacitor is capable of backing up the SoM RTC for at least (TBD) at 25 °C.

26.3.3 UART

The Libra Development Board features 3 UART interfaces. This paragraph describes their default and alternative purposes.

UART1 (full flow control) is configurable to provide one of three functions via 2 integrated switches (U38/U40) and one hardware switch S5. The following table explains the necessary settings for a desired UART1 target:

UART1 Target	S5	U38	U40
Bluetooth over M.2 Key-E	X	UART1_BT_RS_SEL = 1 Default = 0	X
RS232 at X27 through U37	0	UART1_BT_RS_SEL = 0	UART1_RS232_485_SEL = 1 S5 override GPIO

UART1 Target	S5	U38	U40
RS485 at X27 through U39	1	UART1_BT_RS_SEL = 0	UART1_RS232_485_SEL = 0 S5 override GPIO

TABLE 47: UART1 Target Selection

UART2 (full flow control) is connected to the USB debug channel 2 via the default setting of JP1. UART3 is connected to the USB debug channel 1 via the default setting of JP1.

26.3.3.1 UART Design Considerations

When designing a custom carrier board, remember the FPSC output TTL level is 1.8 V.

26.3.4 RS-232/RS-485 (X27)

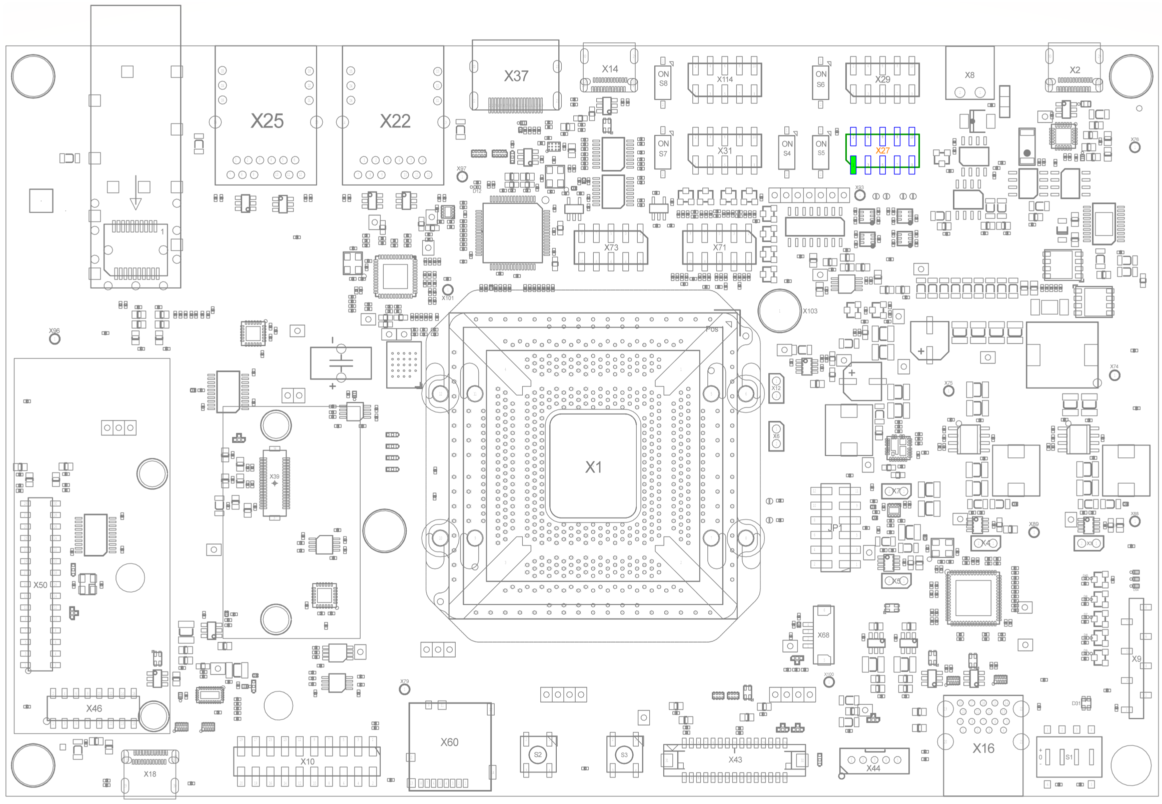


FIGURE 17: RS-232 and RS-485 Connector (X27)

Pin header connector X27 provides the UART1 signals of the phyFLEX FPSC SoM as either RS-232 or RS-485 signal. Mode is selected by routing UART1 to the applicable converter. Please refer to the UART1 Target Selection. The RS-232 interface is intended to be used as data terminal equipment (DTE) and allows for a 5-wire connection, including the signals RTS and CTS for hardware flow control. RS-485 is available in Half-Duplex (4-wire). The table below shows the signal mapping of the RS-232 and RS-485 level signals at connector X27.

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	NC	-	-	No connect
3	X_RS232_RXD	I	-	RS232 receive data
4	X_RS232_RTS	O	-	RS232 request to send
5	X_RS232_TXD	O	-	RS232 transmits data
6	X_RS232_CTS	I	-	RS232 clear to send
7	X_RS485_A	I/O	-	RS485 non-inverted
8	X_RS485_B	I/O	-	RS485 inverted
9	GND	-	0.0 V	Ground
10	GND	-	0.0 V	Ground

TABLE 48: RS-232/RS-485 (X27) Pin Assignment

26.3.5 CAN FD (X29/X31/X114)

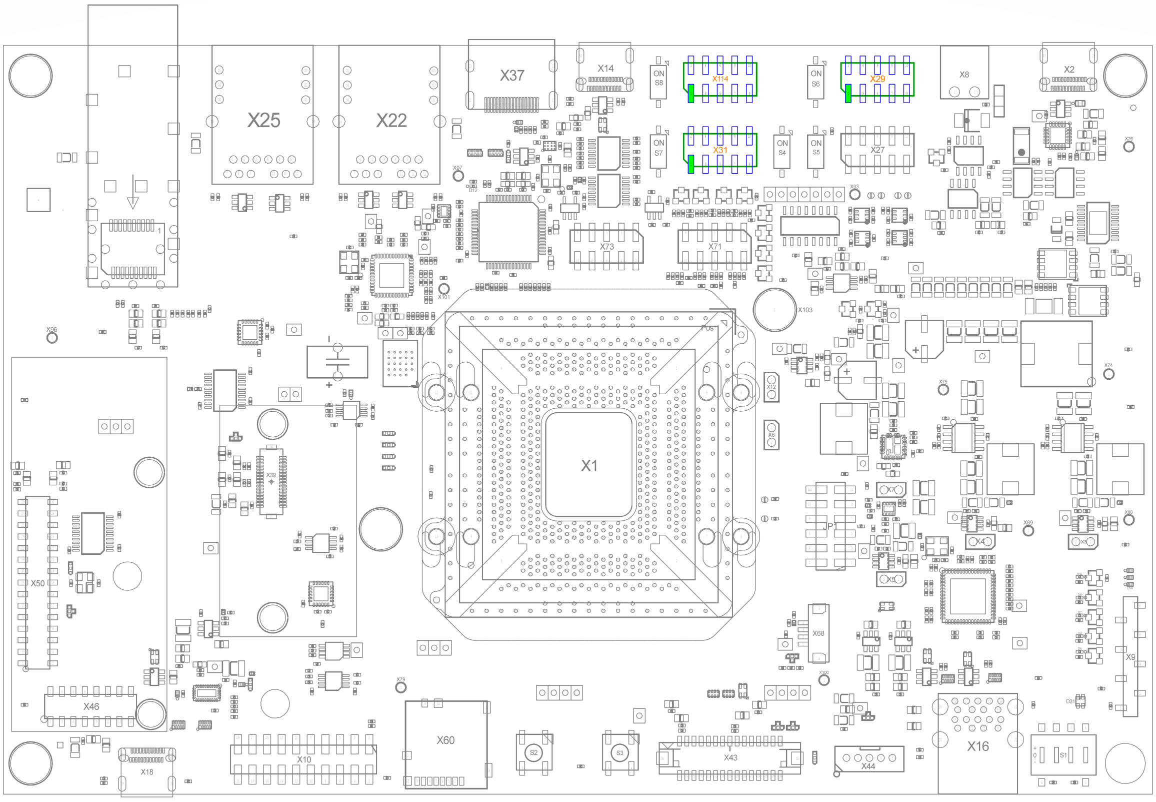


FIGURE 18: CAN FD (X29/X31/X114)

The phyFLEX FPSC SoM FLEXCAN1, FLEXCAN2, and FLEXCAN3 interfaces are brought out at X29, X31 and X114, each as CAN FD. The maximum permissible CAN FD data rate is 8 Mbit/s. For development purposes, a 120 Ω termination can be added by closing SW5 (CAN1), SW6 (CAN2) or SW8 (CAN3). For standard use, it is possible to mount a more suitable split termination in a customer-specific BOM.

The pinout is chosen to fit the official standard CAN pinout and is displayed in the table below.

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	GND	-	0.0 V	Ground
3	X_CAN1_L	CAN_I/O	-	Low-level CAN bus input/output line
4	X_CAN1_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	0.0 V	Ground
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	NC	-	-	No connect
10	NC	-	-	No connect

TABLE 49: CAN FD1 (X29) Pin Assignment

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	GND	-	0.0 V	Ground
3	X_CAN2_L	CAN_I/O	-	Low-level CAN bus input/output line
4	X_CAN2_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	0.0 V	Ground
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	NC	-	-	No connect
10	NC	-	-	No connect

TABLE 50: CAN FD2 (X31) Pin Assignment

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	GND	-	0.0 V	Ground
3	X_CAN3_L	CAN_I/O	-	Low-level CAN bus input/output line
4	X_CAN3_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	0.0 V	Ground
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	NC	-	-	No connect
10	NC	-	-	No connect

TABLE 51: CAN FD3 (X114) Pin Assignment

26.3.6 Ethernet (X22/X25)

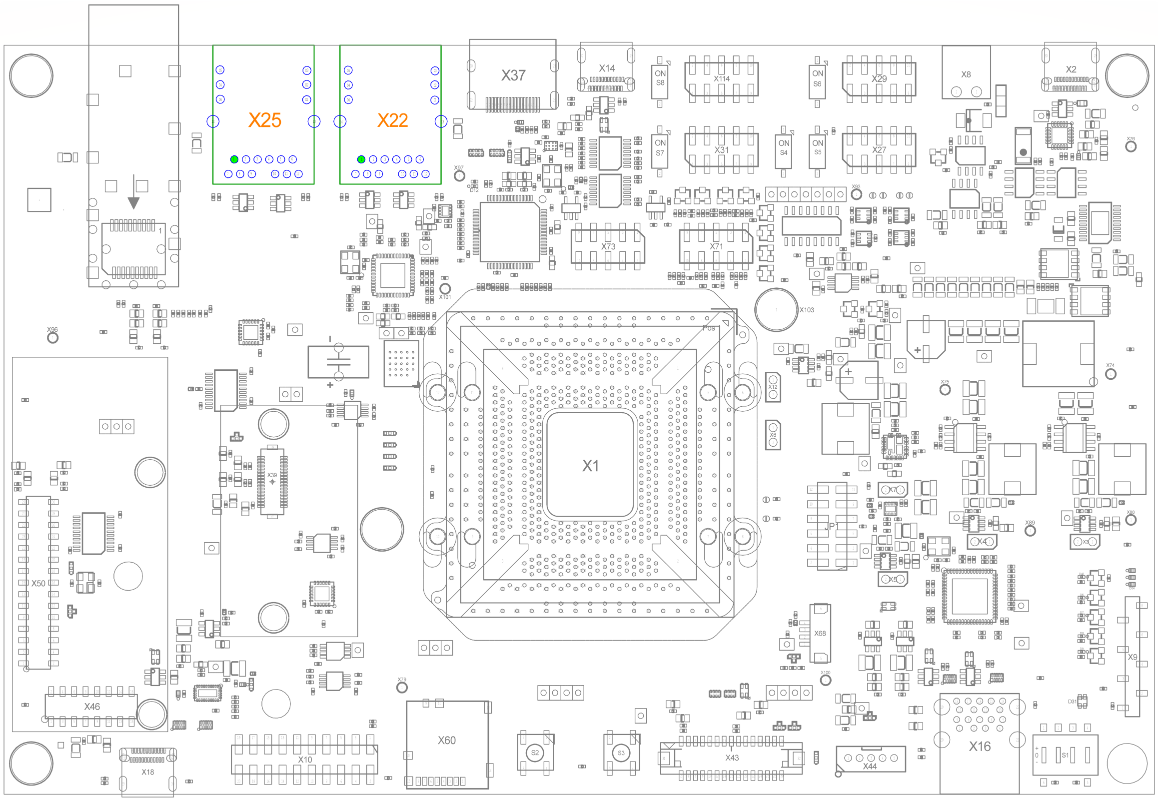


FIGURE 19: Ethernet Connectors (X22/X25)
The Libra Development Board is equipped with 2 RJ45 connectors. The table below describes the properties of each Ethernet interface:

Interface Name	Ethernet Connector	Interface Description
Ethernet2	X22	10/100/1000 Ethernet interface over a Gigabit Ethernet transceiver on a carrier board
Ethernet1	X25	10/100/1000 Ethernet interface over a Gigabit Ethernet transceiver on a mounted SoM

TABLE 52: RJ45 Ethernet connectors X22/X25
The LEDs for LINK (green) and ACTIVITY (orange) indications are integrated into the connector. The Ethernet transceivers support Auto MDI-X, eliminating the need for a direct connect LAN or cross-over path cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

26.3.6.1 Ethernet Design Considerations

The data lanes should be routed with a differential impedance of 100 Ohms. The center taps of each pair's transformer have to be connected to GND through a 100nF capacitor. The LED pins are open-drain outputs of the SoM without a resistor, so they should be connected to the cathodes of the LEDs through a resistor.

26.3.7 USB Dual Type-A 3.0 Interface (X16)

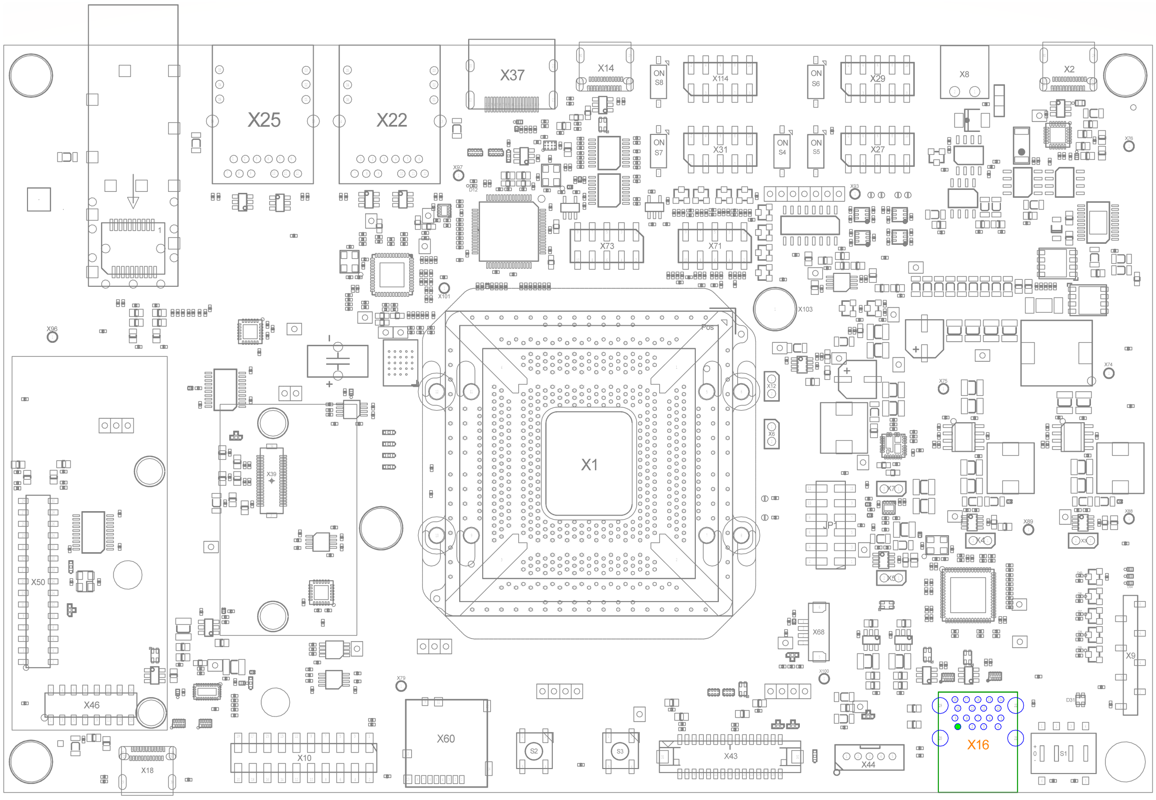


FIGURE 20: USB Dual Type-A 3.0 Connector (X16)

The Libra Development Board provides two USB 3.0 interfaces at the USB Dual Type-A connector X16. They are HOST interfaces made available through a 4-port USB HUB. USB1 will be at the connector's top and USB2 at the bottom receptacle.

26.3.8 USB-C 3.2 GEN 1 Interface (X18)

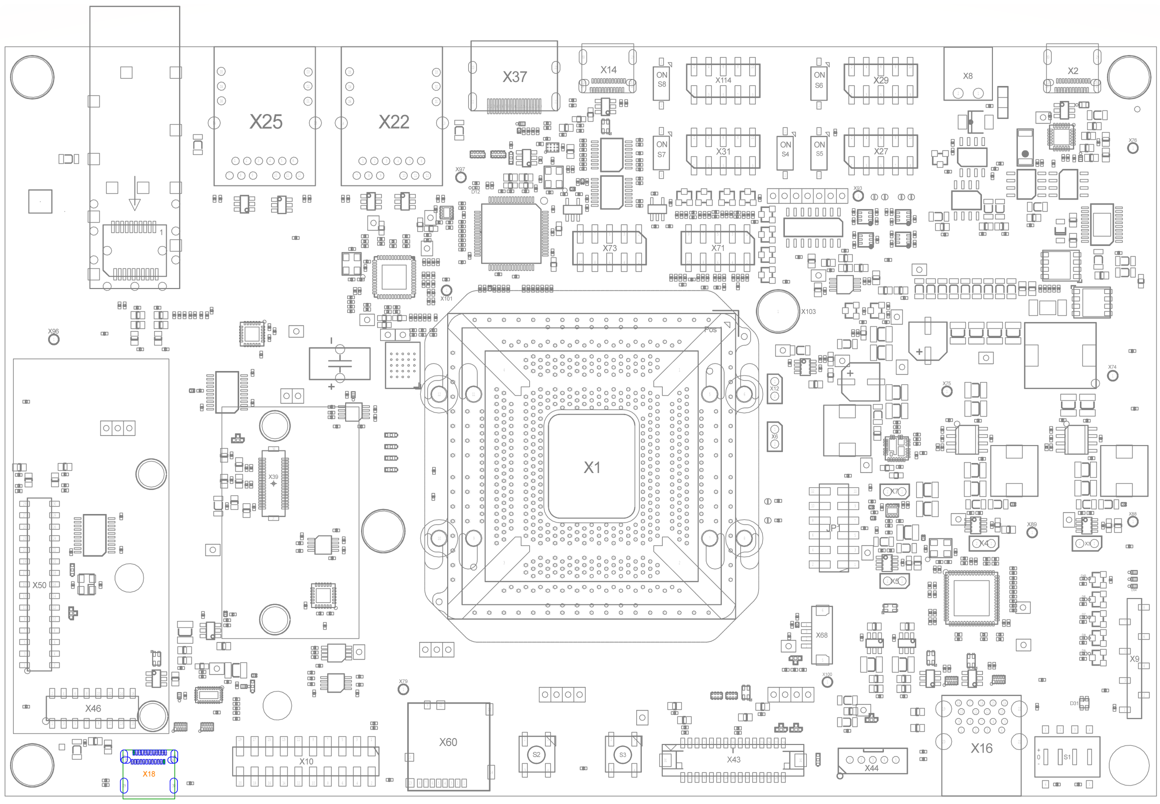


FIGURE 21: USB 3.2 Gen1 Connector (X18)

The Libra Development Board provides a USB-C 3.2 GEN 1 Dual Role interface. Muxing of super-speed differential data lanes is handled through a dedicated muxing IC (U66). The mounted SoM's USB Serial Downloader requires this interface to be able to boot from USB.

26.3.8.1 USB 3.2 Gen1 Design Considerations

Series capacitors are already present on the phyFLEX FPSC SoM. It is not necessary to provide additional series capacitors in the TX lines. Double-check the signal direction of the high-speed lines where TX is output and RX is input on the phyFLEX FPSC SoM. The TX and RX lines should be routed with an impedance of 50 Ohms to a ground plane and 100 Ohms differential impedance. Route USB 2.0 data lines with 45 Ohms to Ground and 90 Ohms differential impedance.

26.3.9 USB Debug (X14)

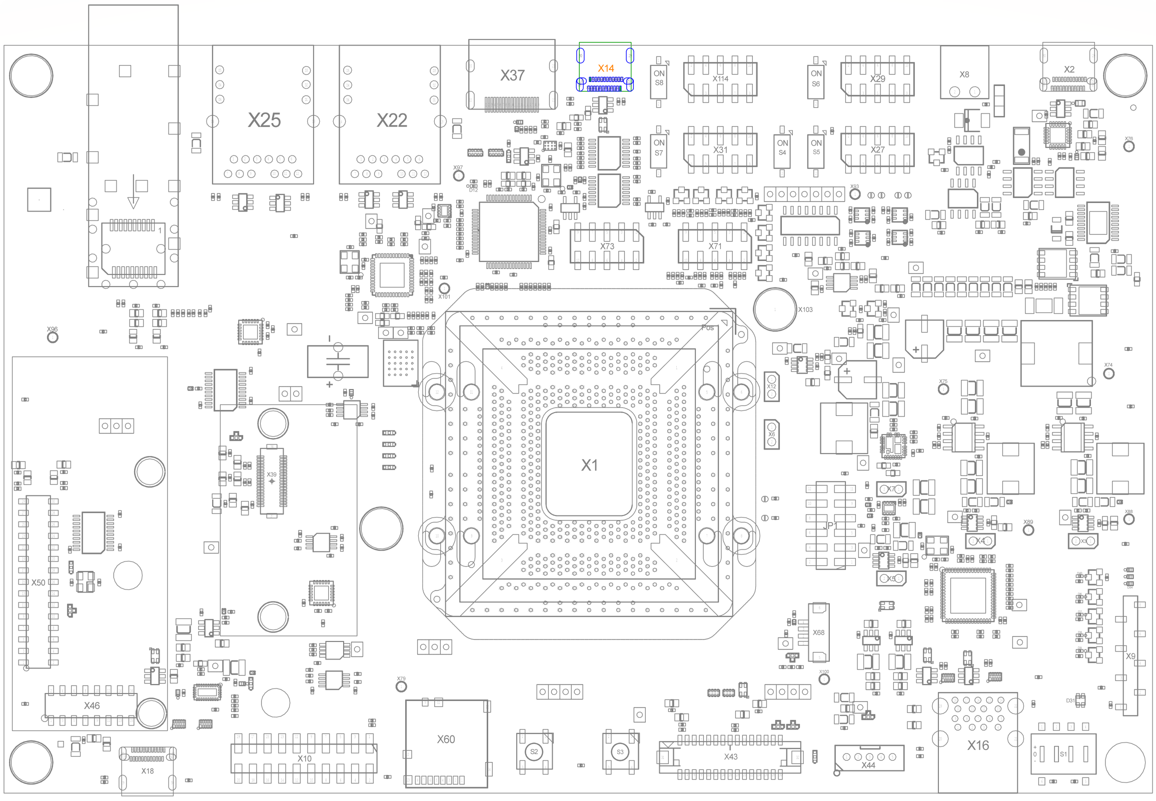


FIGURE 22: USB Debug Connector (X14)

The primary debug interface is UART3. UART2 is the special debug interface used to connect to an M-core or similar provided by the SoM. Both UART interfaces are connected to a UART-to-USB converter (U15 FTDI FT4232H). The USB 2.0 interface is brought out at a USB-C socket (X14). Use the following terminal settings to connect to the Libra Development Board serial interfaces:

- Speed: 115200 baud
- Data bits: 8
- Stop bits: 1
- Parity: None
- Flow control: None

The USB debug interface is also capable of manipulating the Boot Mode signals through FT4232H bank D and triggering a reset through FT4232H bank C. BOOT_MODE manipulation has to be enabled by pulling the signal DEBUG_BOOT_EN (DDBUS4 at U15) high.

The table below shows the pinout of the USB Debug connector:

Interface Pin #	Signal name	Signal Type	Signal Level	Description
A1	GND	-	0.0 V	Ground
A2	NC	-	-	No connect
A3	NC	-	-	No connect
A4	VBUS	I	5.0 V	USB VBUS provided by Host
A5	CC1	I/O	-	Configuration channel 5k1 pull down
A6	X_DEBUG_USB_DP	USB_I/O	-	USB Debug Data+
A7	X_DEBUG_USB_DM	USB_I/O	-	USB Debug Data-
A8	NC	-	-	No connect
A9	VBUS	I	5.0 V	USB VBUS provided by Host
A10	NC	-	-	No connect
A11	NC	-	-	No connect
A12	GND	-	0.0 V	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
B1	GND	-	0.0 V	Ground
B2	NC	-	-	No connect
B3	NC	-	-	No connect
B4	VBUS	I	5.0 V	USB VBUS provided by Host
B5	CC2	I/O	-	Configuration channel 5k1 pull down
B6	X_DEBUG_USB_DP	USB_I/O	-	USB Debug Data+
B7	X_DEBUG_USB_DM	USB_I/O	-	USB Debug Data-
B8	NC	-	-	No connect
B9	VBUS	I	5.0 V	USB VBUS provided by Host
B10	NC	-	-	No connect
B11	NC	-	-	No connect
B12	GND	-	0.0 V	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	GND	-	0.0 V	Ground
26	GND	-	0.0 V	Ground
27	GND	-	0.0 V	Ground
28	GND	-	0.0 V	Ground
29	GND	-	0.0 V	Ground
30	GND	-	0.0 V	Ground

TABLE 53: X14 Pin Assignment

26.3.10 Secure Digital Memory Card / MultiMedia Card (X60)

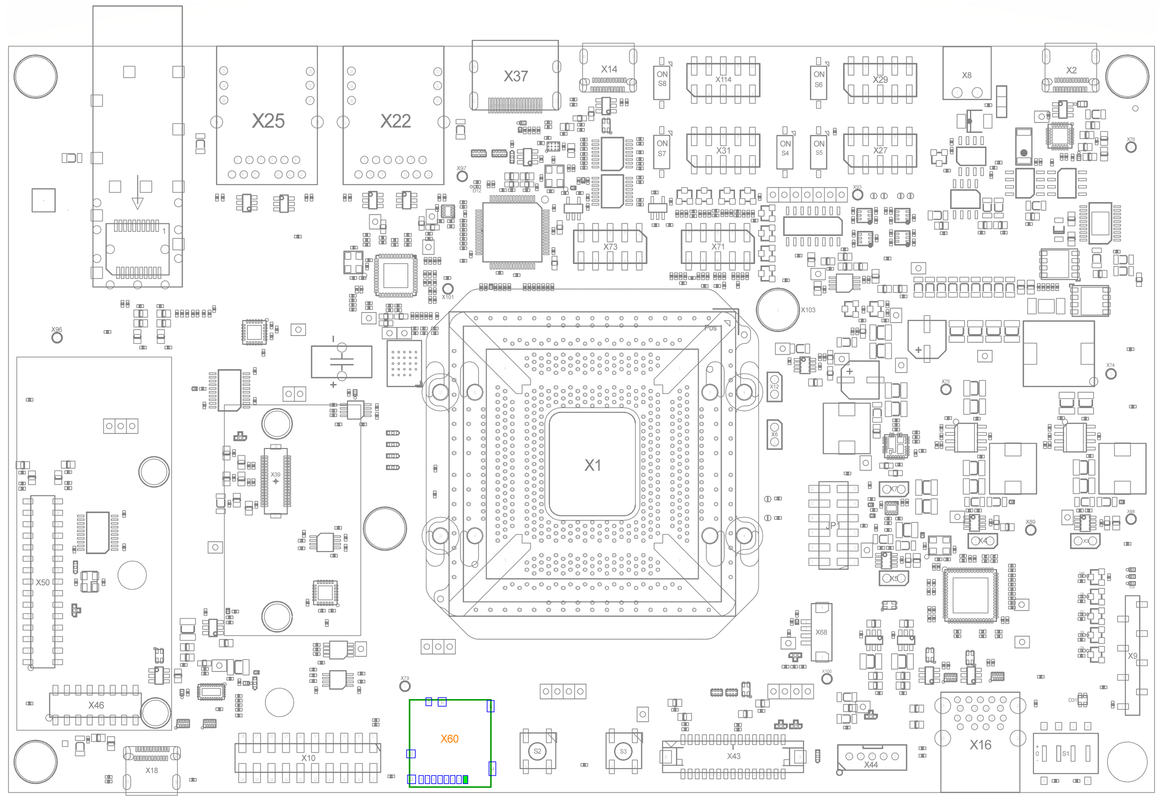


FIGURE 23: SD / MM Card Connector (X60)

The Libra Development Board provides a standard microSDHC card slot at X60 for use with SD/MMC interface cards. It allows for a fast, easy connection to peripheral devices like microSD and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC connector. It also features card detection, a lock mechanism, and a smooth extraction function by pushing the card in and out.

26.3.10.1 SD / MM Card Design Considerations

Series resistors might be required to adapt the drive strength of the card. SD interface should be routed with an impedance of 50 Ohms to a ground plane. The trace length between CLK, CMD, and DATA lanes should be matched and kept as short as possible. Avoid Vias and take care of the signal current return path.

26.3.11 M.2 Key-E (X52)

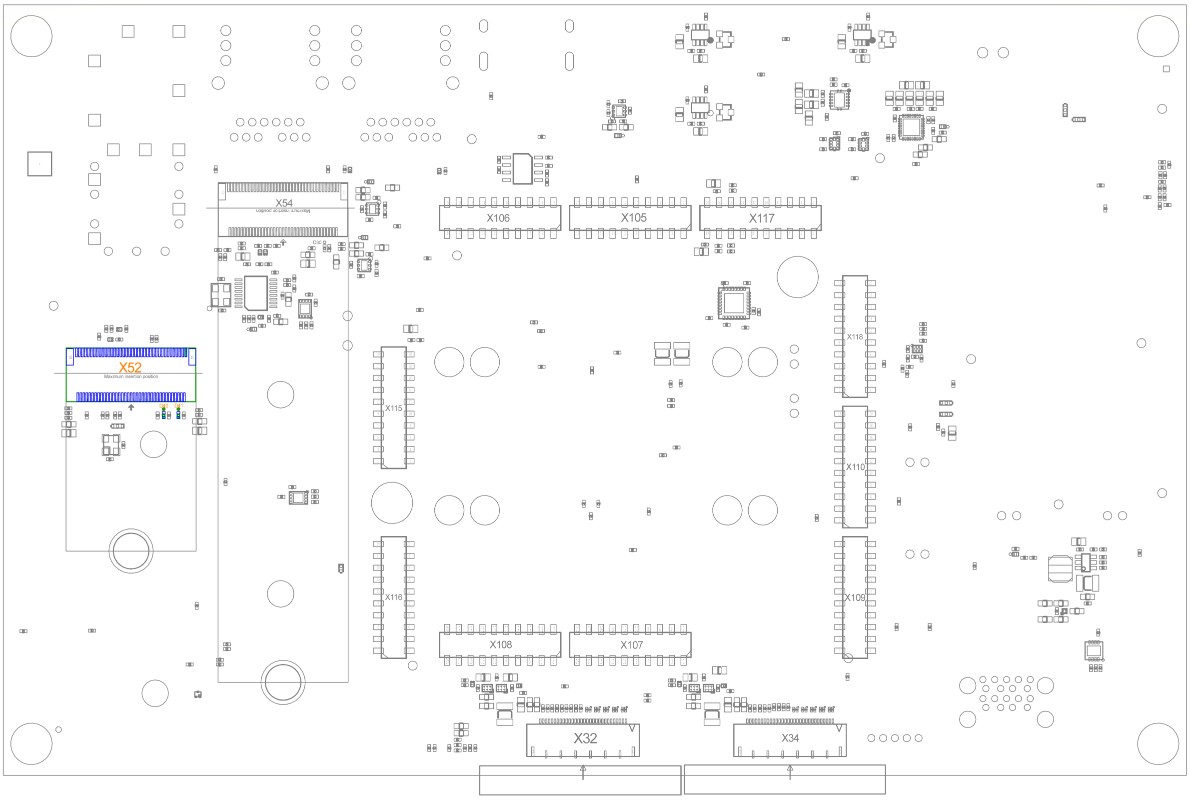


FIGURE 24: M.2 Key-E Connector (X52)

The 1-lane PCI Express interface provides PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. Various control signals are implemented with GPIOs. The PCIE1 interface is brought out at the M.2 Key-E connector X52 shown above. The M.2 Key-E connector also features UART with flow-control, SDIO, I2C and USB 2.0.

The table below shows in-depth information, such as pin assignment and signals used to implement special features of the Mini PCIe interface.

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	0.0 V	Ground
2	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
3	X_USB_HUB_DN1_P	USB_I/O	-	USB 2.0 Data+
4	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
5	X_USB_HUB_DN1_N	USB_I/O	-	USB 2.0 Data-
6	LED_1	I	3,3 V	Status LED 1
7	GND	-	0.0 V	Ground
8	NC	-	-	No connect
9	X_SDIO_CLK	O	1.8 V	SDIO clock signal
10	NC	-	-	No connect
11	X_SDIO_CMD	O	1.8 V	SDIO command signal
12	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_SDIO_D0	I/O	1.8 V	SDIO data 0 signal
14	NC	-	-	No connect
15	X_SDIO_D1	I/O	1.8 V	SDIO data 1 signal
16	LED_2	I	3.3 V	Status LED 2
17	X_SDIO_D2	I/O	1.8 V	SDIO data 2 signal
18	GND	-	0.0 V	Ground
19	X_SDIO_D3	I/O	1.8 V	SDIO data 3 signal
20	X_UART1_nWAKE	O	3.3 V	UART1 sideband platform wake signal
21	X_SDIO_nWAKE	O	1.8 V	SDIO sideband wake signal
22	X_UART1_RXD_BT	I	1.8 V	UART1 receive data signal
23	X_SDIO_nRESET	PCIE_I	1.8 V	SDIO sideband enable/disable (reset) signal
24	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	NC	-	-	No connect
27	NC	-	-	No connect
28	NC	-	-	No connect
29	NC	-	-	No connect
30	NC	-	-	No connect
31	NC	-	-	No connect
32	X_UART1_TXD_BT	O	1.8 V	UART1 transmit data signal
33	GND	-	0.0 V	Ground
34	X_UART1_CTS	I	1.8 V	UART1 clear to send signal
35	X_PCIE1_TXN_P	O	-	PCI Express 1 positive transmit data signal
36	X_UART1_RTS	O	1.8 V	USB 2.0 Data-

Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	X_PCIE1_TXN_N	O	-	PCI Express 1 negative transmit data signal
38	NC	-	-	No connect
39	GND	-	0.0 V	Ground
40	NC	-	-	No connect
41	X_PCIE1_RXN_P	I	-	PCI Express 1 positive receive data signal
42	NC	-	-	No connect
43	X_PCIE1_RXN_N	I	-	PCI Express 1 negative receive data signal
44	TP84	O	1.8 V	Test point for COEX3 signal
45	GND	-	0.0 V	Ground
46	TP85	I	1.8 V	Test point for COEX_RXD signal
47	X_PCIE1_CLK_P	O	-	PCI Express 1 positive reference clock signal
48	TP86	O	1.8 V	Test point for COEX_TXD signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
49	X_PCIE1_CLK_N	O	-	PCI Express 1 negative reference clock signal
50	X_KEY-E_32k_SUSCLK	O	3.3 V	32768 Hz suspend clock signal
51	GND	-	0.0 V	Ground
52	X_PCIE1_nPERST_3V3		3.3 V	PCI Express 1 add-in card reset
53	X_PCIE1_nCLKREQ_3V3	I/O	3.3 V	PCI Express 1 clock request signal
54	X_W_nDISABLE1	O	3.3 V	Disable radio operation on add-in card 1 signal
55	X_PCIE1_nWAKE	I/O	3.3 V	PCI Express wake signal, OBFF
56	X_W_nDISABLE2	O	3.3 V	Disable radio operation on add-in card 2 signal
57	GND	-	0.0 V	Ground
58	X_I2C3_SDA	I/O	1.8 V	I2C3 serial data signal
59	NC	-	-	No connect
60	X_I2C3_SCL	O	1.8 V	I2C3 serial clock signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
61	NC	-	-	No connect
62	X_KEY-E_nALERT	I	1.8 V	Key-E interrupt signal
63	GND	-	0.0 V	Ground
64	NC	-	-	No connect
65	NC	-	-	No connect
66	NC	-	-	No connect
67	NC	-	-	No connect
68	NC	-	-	No connect
69	GND	-	0.0 V	Ground
70	NC	-	-	No connect
71	NC	-	-	No connect
72	VDD_3V3	PWR_O	3.3 V	3.3 V power rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
73	NC	-	-	No connect
74	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
75	GND	-	0.0 V	Ground
S1	GND	-	0.0 V	Ground
S2	GND	-	0.0 V	Ground

TABLE 54: X52 Pin Assignment

26.3.11.1 PCIe Design Considerations

100nF AC coupling capacitors are placed at the output of the phyFLEX FPSC SoM in series to the TX lanes. A clock generator on the carrier board generates the PCIe clock.

26.3.12 M.2 Key-M (X54)

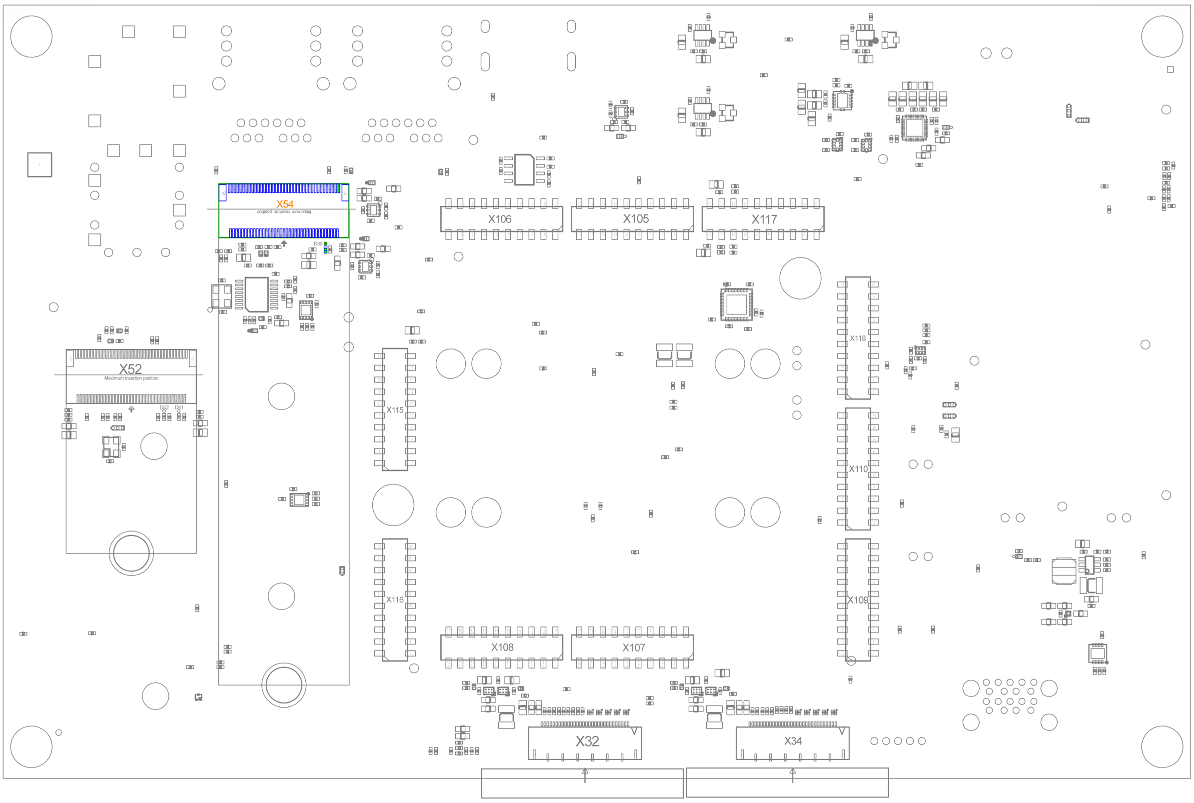


FIGURE 25: M.2 Key-M (X54)

The second 1-lane PCI Express interface provides PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. The mounted M.2 Key-M connector is mainly used for SSD cards. Various control signals are implemented with GPIOs. The PCIE2 interface is brought out at the M.2 Key-M connector X54 shown above. The PCIe clock is generated by the dedicated PCIe clock generator U51. This feature is not available for all mountable FPSC SoMs.

The table below shows in-depth information, such as pin assignment and signals used to implement special features of the M.2 Key-M interface.

Interface Pin #	**Signal name**	**Signal Type**	**Signal Level**	**Description**
1	GND	-	0.0 V	Ground
2	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
3	GND	-	0.0 V	Ground
4	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
5	NC	-	-	No connect
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	GND	-	0.0 V	Ground
10	LED1	I	3.3 V	M.2 Key-M activity LED signal
11	NC	-	-	No connect
12	VDD_3V3	PWR_O	3.3 V	3.3 V power rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	NC	-	-	No connect
14	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
15	GND	-	0.0 V	Ground
16	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
17	NC	-	-	No connect
18	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
19	NC	-	-	No connect
20	NC	-	-	No connect
21	GND	-	0.0 V	Ground
22	NC	-	-	No connect
23	NC	-	-	No connect
24	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	NC	-	-	No connect
27	GND	-	0.0 V	Ground
28	NC	-	-	No connect
29	NC	-	-	No connect
30	NC	-	-	No connect
31	NC	-	-	No connect
32	NC	-	-	No connect
33	GND	-	0.0 V	Ground
34	NC	-	-	No connect
35	NC	-	-	No connect
36	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	NC	-	-	No connect
38	NC	-	-	No connect
39	GND	-	0.0 V	Ground
40	X_I2C2_SCL	O	1.8 V	I2C2 serial clock
41	X_PCIE2_TXN_N	O	-	PCI Express 2 negative transmit data signal
42	X_I2C2_SDA	I/O	1.8 V	I2C2 serial data
43	X_PCIE2_TXN_P	O	-	PCI Express 2 positive transmit data signal
44	X_KEY-M_nALERT	I	1.8 V	Key-M interrupt signal
45	GND	-	0.0 V	Ground
46	NC	-	-	No connect
47	X_PCIE2_RXN_N	I	-	PCI Express 2 negative receive data signal
48	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
49	X_PCIE2_RXN_P	I	-	PCI Express 2 positive receive data signal
50	X_PCIE2_nCLKREQ_3V3	I/O	3.3 V	PCI Express 2 clock request signal
51	GND	-	0.0 V	Ground
52	X_PCIE2_nPERST_3V3		3.3 V	PCI Express 2 add-in card reset
53	X_PCIE2_CON_REFPAD_CLK_N	O	-	PCI Express 2 negative reference clock signal
54	X_PCIE2_nWAKE	I/O	3.3 V	PCI Express wake signal, OBFF
55	X_PCIE2_CON_REFPAD_CLK_P	O	-	PCI Express 2 positive reference clock signal
56	NC	-	-	No connect
57	GND	-	0.0 V	Ground
58	NC	-	-	No connect
59	NC	-	-	No connect
60	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
61	NC	-	-	No connect
62	NC	-	-	No connect
63	NC	-	-	No connect
64	NC	-	-	No connect
65	NC	-	-	No connect
66	NC	-	-	No connect
67	NC	-	-	No connect
68	X_KEY-M_32k_SUSCLK	O	3.3 V	32768 Hz suspend clock signal
69	NC	-	-	No connect
70	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
71	GND	-	0.0 V	Ground
72	VDD_3V3	PWR_O	3.3 V	3.3 V power rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
73	GND	-	0.0 V	Ground
74	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
75	GND	-	0.0 V	Ground
S1	GND	-	0.0 V	Ground
S2	GND	-	0.0 V	Ground

TABLE 55: X54 Pin Assignment

26.3.13 Camera Connectivity

26.3.13.1 phyCAM-M MIPI CSI Camera Connectors (X32/34)

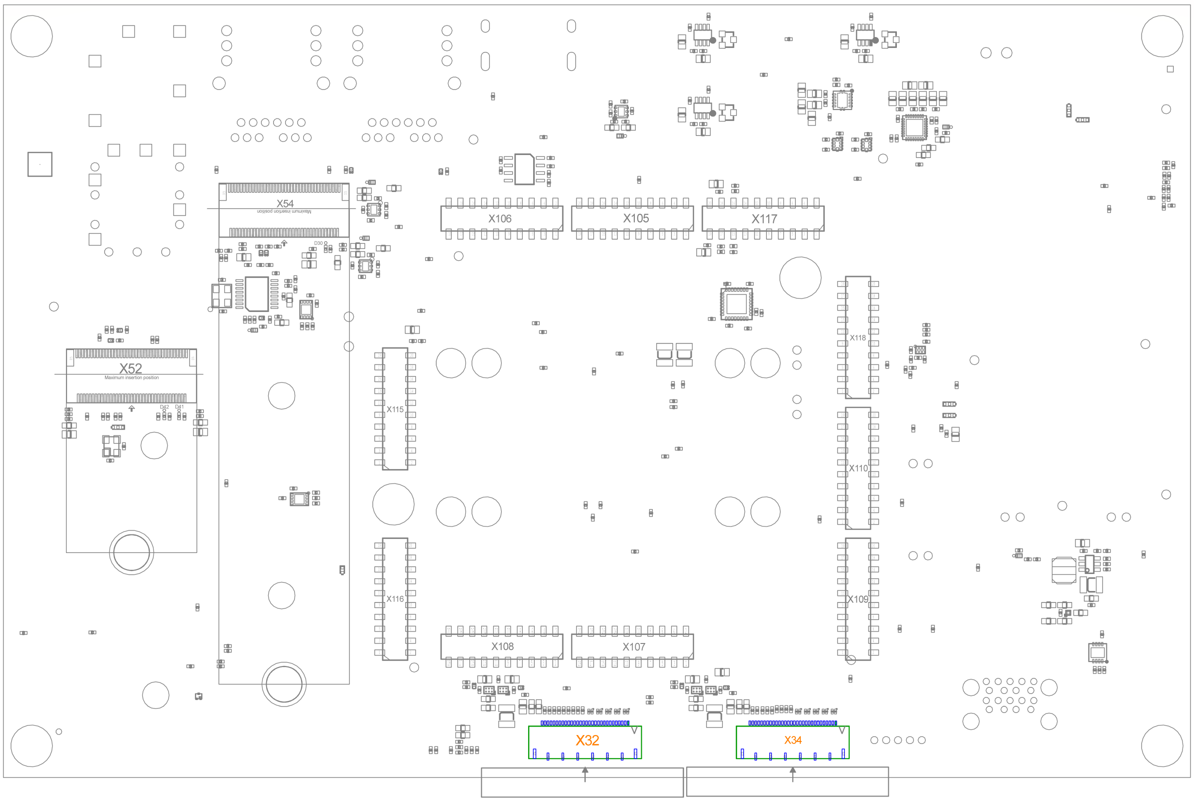


FIGURE 26: phyCAM-M MIPI CSI-2 Camera Connectors (X32/X34)

The phyFLEX FPSC SoM on the Libra Development Board offers 2 independent interfaces to connect digital camera boards with the MIPI CSI-2 interface. The 4-lane MIPI CSI-2 interfaces are brought out as phyCAM-M camera interfaces at connectors X32 and X34. The pin assignments of connectors X32 and X34 are shown below. The phyCAM-M camera connectors fit the phyCAM-M product family with various color and monochrome sensors. Suitable camera modules are, e.g., VM-016-COL-M (1 MPix) or VM-017-BW-M (5 Mpix), which can be delivered with a complete objective. Contact the PHYTEC Sales Team for advice on how to tailor a camera module to your application.

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_MIPI_CSI1_D0_P	MIPI CSI-2	-	MIPI CSI-2 data 0 positive signal
3	X_MIPI_CSI1_D0_N	MIPI CSI-2	-	MIPI CSI-2 data 0 negative signal
4	GND	-	-	Ground
5	X_MIPI_CSI1_D1_P	MIPI CSI-2	-	MIPI CSI-2 data 1 positive signal
6	X_MIPI_CSI1_D1_N	MIPI CSI-2	-	MIPI CSI-2 data 1 negative signal
7	GND	-	-	Ground
8	X_MIPI_CSI1_CLK_P	MIPI CSI-2	-	MIPI CSI-2 clock positive signal
9	X_MIPI_CSI1_CLK_N	MIPI CSI-2	-	MIPI CSI-2 clock negative signal
10	GND	-	-	Ground
11	X_MIPI_CSI1_D2_P	MIPI CSI-2	-	MIPI CSI-2 data 2 positive signal
12	X_MIPI_CSI1_D2_N	MIPI CSI-2	-	MIPI CSI-2 data 2 negative signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_MIPI_CSI1_D3_P	MIPI CSI-2	-	MIPI CSI-2 data 3 positive signal
15	X_MIPI_CSI1_D3_N	MIPI CSI-2	-	MIPI CSI-2 data 3 negative signal
16	GND	-	-	Ground
17	X_CSI1_CTRL4	OD-BI-PU	3.3 V	CSI1 control 4
18	X_CSI1_CTRL3	OD-BI-PU	3.3 V	CSI1 control 3
19	X_CSI1_CTRL2	OD-BI-PU	3.3 V	CSI1 control 2
20	X_CSI1_CTRL1	OD-BI-PU	3.3 V	CSI1 control 1
21	GND	-	-	Ground
22	X_I2C3_SCL_3V3	O	3.3 V	I2C3 serial clock
23	X_I2C3_SDA_3V3	I/O	3.3 V	I2C3 serial data
24	X_CSI1_ADDR	O	3.3 V	I2C camera address choice

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	X_CSI1_nRESET	O	3.3 V	Camera reset signal
26	X_CSI1_VDD_SELECT	OD-I-PU	3.3 V	Interface voltage selection: ▪ open = 3.3 V ▪ GND = 5 V
27	GND	-	-	Ground
28	VDD_CSI1_OUT	PWR_O	3.3 V / 5 V	Camera power supply
29	VDD_CSI1_OUT	PWR_O	3.3 V / 5 V	Camera power supply
30	VDD_CSI1_OUT	PWR_O	3.3 V / 5 V	Camera power supply

TABLE 56: MIPI CSI-2 Camera 1 (X32) Pin Assignment

Interface Pin #	**Signal name**	**Signal Type**	**Signal Level**	**Description**
1	GND	-	-	Ground
2	X_MIPI_CSI2_D0_P	MIPI CSI-2	-	MIPI CSI-2 data 0 positive signal
3	X_MIPI_CSI2_D0_N	MIPI CSI-2	-	MIPI CSI-2 data 0 negative signal
4	GND	-	-	Ground
5	X_MIPI_CSI2_D1_P	MIPI CSI-2	-	MIPI CSI-2 data 1 positive signal
6	X_MIPI_CSI2_D1_N	MIPI CSI-2	-	MIPI CSI-2 data 1 negative signal
7	GND	-	-	Ground
8	X_MIPI_CSI2_CLK_P	MIPI CSI-2	-	MIPI CSI-2 clock positive signal
9	X_MIPI_CSI2_CLK_N	MIPI CSI-2	-	MIPI CSI-2 clock negative signal
10	GND	-	-	Ground
11	X_MIPI_CSI2_D2_P	MIPI CSI-2	-	MIPI CSI-2 data 2 positive signal
12	X_MIPI_CSI2_D2_N	MIPI CSI-2	-	MIPI CSI-2 data 2 negative signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_MIPI_CSI2_D3_P	MIPI CSI-2	-	MIPI CSI-2 data 3 positive signal
15	X_MIPI_CSI2_D3_N	MIPI CSI-2	-	MIPI CSI-2 data 3 negative signal
16	GND	-	-	Ground
17	X_CSI2_CTRL4	OD-BI-PU	3.3 V	CSI2 control 4
18	X_CSI2_CTRL3	OD-BI-PU	3.3 V	CSI2 control 3
19	X_CSI1_CTRL1	OD-BI-PU	3.3 V	CSI1 control 1, Camera 2 is set up to be triggered by Camera 1 strobe output
20	X_CSI2_CTRL1	OD-BI-PU	3.3 V	CSI2 control 1
21	GND	-	-	Ground
22	X_I2C4_SCL_3V3	O	3.3 V	I2C4 serial clock
23	X_I2C4_SDA_3V3	I/O	3.3 V	I2C4 serial data
24	X_CSI2_ADDR	O	3.3 V	I2C camera address choice

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	X_CSI2_nRESET	O	3.3 V	Camera reset signal
26	X_CSI2_VDD_SELECT	OD-I-PU	3.3 V	Interface voltage selection: • open = 3.3 V • GND = 5 V
27	GND	-	-	Ground
28	VDD_CSI2_OUT	PWR_O	3.3 V / 5 V	Camera power supply
29	VDD_CSI2_OUT	PWR_O	3.3 V / 5 V	Camera power supply
30	VDD_CSI2_OUT	PWR_O	3.3 V / 5 V	Camera power supply

TABLE 57: MIPI CSI-2 Camera 2 (X34) Pin Assignment

26.3.13.2 Camera Design Considerations

Regarding camera connections when designing a customer carrier board:

1. The differential impedance should be 100 Ohms for all lanes to a Ground Plane. The lanes should be matched.
2. phyCAM-M interfaces offer 3.3 V or 5 V supply voltages (selected by interface pin 26). Both voltages should be provided by the board to guarantee full compatibility with the phyCAM-M interface.
3. Each phyCAM interface needs a different I^2C address if connected to the same I^2C Bus. Place a Pull-up resistor at pin 24 to select the secondary address.

General information and design guidelines for PHYTEC camera interfaces can be found here:

- German: L-867Bd.A9 phyCAM Basis-Spezifikation und Design-In Guide
- English: L-867Be.A9 phyCAM Basis Specification and Design-In Guide

Specific information for each PHYTEC camera module can be found on that module's download page: PHYTEC Embedded Vision (Deutsch) or PHYTEC Embedded Vision (English).

26.3.14 HDMI (X37)

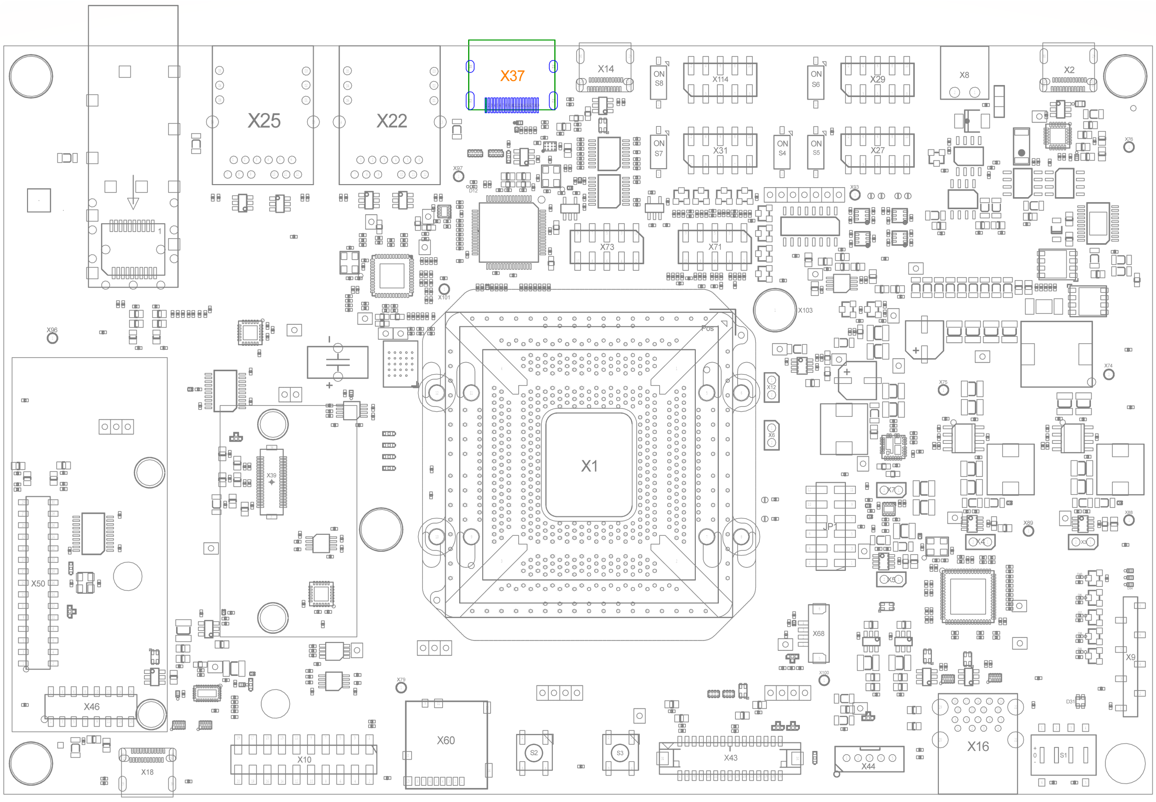


FIGURE 27: HDMI Connector (X37)

The Libra Development Board provides a High-Definition Multimedia Interface (HDMI), which is compliant with HDMI 2.0a. It supports a maximum resolution of 1920x1080p60, 1280x720p60, 720x480p60, and 640x480p60. Please refer to the applicable phyFLEX FPSC SoM Applications Processor Reference Manual for more information. This feature is not available for all mountable FPSC SoMs.

The HDMI interface is brought out at a standard HDMI type A connector (X37) on the Libra Development Board and comprises the following signal groups:

- Three pairs of data signals
- One pair of clock signals
- The Display Data Channel (DDC)
- The Consumer Electronics Control (CEC)
- The Hot Plug Detect (HPD) signal
- Audio Return Channel (ARC)

All signals are routed from the phyFLEX-Connector to the HDMI receptacle through ESD protection diodes and level shifting components.

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_HDMI_TX2_P	HDMI_O	-	HDMI data 2 positive signal
2	GND	-	0.0 V	Ground
3	X_HDMI_TX2_N	HDMI_O	-	HDMI data 2 negative signal
4	X_HDMI_TX1_P	HDMI_O	-	HDMI data 1 positive signal
5	GND	-	0.0 V	Ground
6	X_HDMI_TX1_N	HDMI_O	-	HDMI data 1 negative signal
7	X_HDMI_TX0_P	HDMI_O	-	HDMI data 0 positive signal
8	GND	-	0.0 V	Ground
9	X_HDMI_TX0_N	HDMI_O	-	HDMI data 0 negative signal
10	X_HDMI_TXC_P	HDMI_O	-	HDMI clock positive signal
11	GND	-	0.0 V	Ground
12	X_HDMI_TXC_N	HDMI_O	-	HDMI clock negative signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_HDMI_CEC	OD-BI-PU	VDD_CEC	Consumer Electronics Control
14	X_EARC_P_UTIL	-	-	Not connected by default, may be connected via resistor jumpers R518 and R519
15	X_HDMI_DDC_SCL	OD-BI-PU	5 V	I2C serial clock
16	X_HDMI_DDC_SDA	OD-BI-PU	5 V	I2C serial data
17	GND	-	0.0 V	Ground
18	VCC_5V_HDMI_OUT	PWR_O	5 V	5 V supply for an HDMI device
19	X_EARC_N_HPD	-	5 V	Audio Return Channel Negative Lane / Hot Plug detect
20	SHIELD_1	-	0.0 V	Shield connected to Ground over 100 nF and 150 pF parallel to 1 MOhm
21	SHIELD_2	-	0.0 V	
22	SHIELD_3	-	0.0 V	
23	SHIELD_4	-	0.0 V	

TABLE 58: X32 Pin Assignment

26.3.14.1 HDMI Design Considerations

The differential impedance should be 100 Ohms for all lanes to a Ground Plane. The lanes should be matched. The DDC lanes need pull-up resistors between 1.5k and 2k to 5V. The CEC lane needs a 27k pull-up resistor connected to 3.3 V through a diode. This prevents leaking current in a power-off state.

26.3.15 Audio/Video (SAI2/LVDS0)

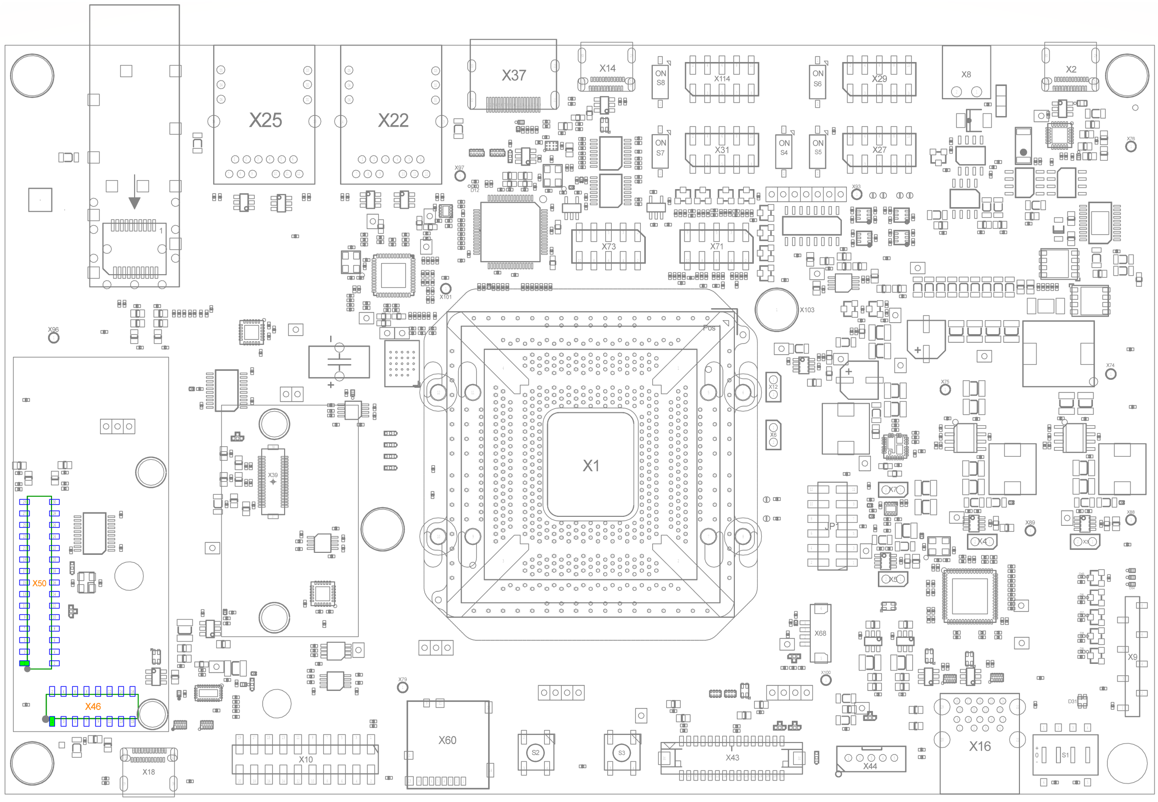


FIGURE 28: Audio/Video Connectors (X46/X50)

The phyFLEX FPSC SoM offers two LVDS display interfaces. The Audio/Video (A/V) connectors X46 and X50 provide an easy way to add typical A/V functions and features to the Libra Development Board. Standard interfaces such as 4-lane LVDS, I2S, I2C, and USB, as well as different supply voltages, are available at the two A/V female pin-sockets. The A/V connector is intended to be used with phyBOARDs and PHYTEC Development Boards to add specific audio/video connectivity with custom expansion boards. A/V connector X46 makes all signals for display connectivity available and provides a supply voltage, while X50 provides signals for audio and touchscreen connectivity as well as an I2C interface, additional control signals and supply voltages. The tables below show the pin assignment of connectors X46 and X50.

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_LVDS2_D2_P	LVDS_O	-	LVDS data 2 positive signal
3	X_LVDS2_CLK_P	LVDS_O	-	LVDS clock positive signal
4	X_LVDS2_D2_N	LVDS_O	-	LVDS data 2 negative signal
5	X_LVDS2_CLK_N	LVDS_O	-	LVDS clock negative signal
6	GND	-	-	Ground
7	GND	-	-	Ground
8	X_LVDS2_D3_P	LVDS_O	-	LVDS data 3 positive signal
9	X_LVDS2_D1_P	LVDS_O	-	LVDS data 1 positive signal
10	X_LVDS2_D3_N	LVDS_O	-	LVDS data 3 negative signal
11	X_LVDS2_D1_N	LVDS_O	-	LVDS data 1 negative signal
12	GND	-	-	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_LVDS2_D0_P	LVDS_O	-	LVDS data 0 positive signal
15	VDD_IN_AV	PWR_O	24 V	A/V power out rail, connected to the carrier board power in
16	X_LVDS2_D0_N	LVDS_O	-	LVDS data 0 negative signal

TABLE 59: X46 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_USB_HUB_DN2_P	USB_I/O	-	USB 2.0 Data+
2	X_USB_HUB_DN2_N	USB_I/O	-	USB 2.0 Data-
3	X_nRESET_OUT	OD_O_PU	3.3 V	A/V reset signal
4	GND	-	-	Ground
5	NC	-	-	No connect
6	X_USB_HUB_OVERCUR2	-	3.3 V	USB over current detection
7	X_USB_HUB_nPWRCTL2	-	3.3 V	USB power control
8	X_SAI1_RXFS_3V3	O	3.3 V	A/V Backlight enable
9	X_PWM1_LVDS_DSI_3V3	O	3.3 V	A/V Backlight PWM, choice between 3.3 V, 0 V and shared PWM signal (default) via J30
10	X_nRESET_OUT	OD_O_PU	3.3 V	Global reset output
11	GND	-	-	Ground
12	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_SAI1_TXD_3V3	O	3.3 V	SAI TXD
14	GND	-	-	Ground
15	NC	-	-	No connect
16	X_SAI1_TXC_3V3	O	3.3 V	SAI TXC
17	X_SAI1_RXC_3V3	O	3.3 V	SAI RXC
18	X_SAI1_TXFS_3V3	O	3.3 V	SAI TXFS
19	X_MCLK_AV	O	3.3 V	SAI MCLK
20	X_SAI1_RXD_3V3	I	3.3 V	SAI RXD
21	GND	-	-	Ground
22	X_I2C3_SDA_3V3	I/O	3.3 V	I2C3 serial data
23	NC	-	-	No connect
24	X_I2C3_SCL_3V3	O	3.3 V	I2C3 serial clock

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	GND	-	-	Ground
27	VDD_5V0	PWR_O	5.0 V	A/V 5.0 V power rail
28	VDD_3V3	PWR_O	3.3 V	A/V 3.3 V power rail
29	VDD_5V0	PWR_O	5.0 V	A/V 5.0 V power rail
30	VDD_3V3	PWR_O	3.3 V	A/V 3.3 V power rail

TABLE 60: X50 Pin Assignment

26.3.15.1 Audio/Video Design Considerations

The differential impedance of LVDS2 lanes should be 100 Ohm and 50 Ohm to a ground plane for all lanes. Lanes should be matched. The audio signals should have a single-ended impedance of 50 Ohms to a ground plane.

26.3.16 LVDS1 (X43/X44)

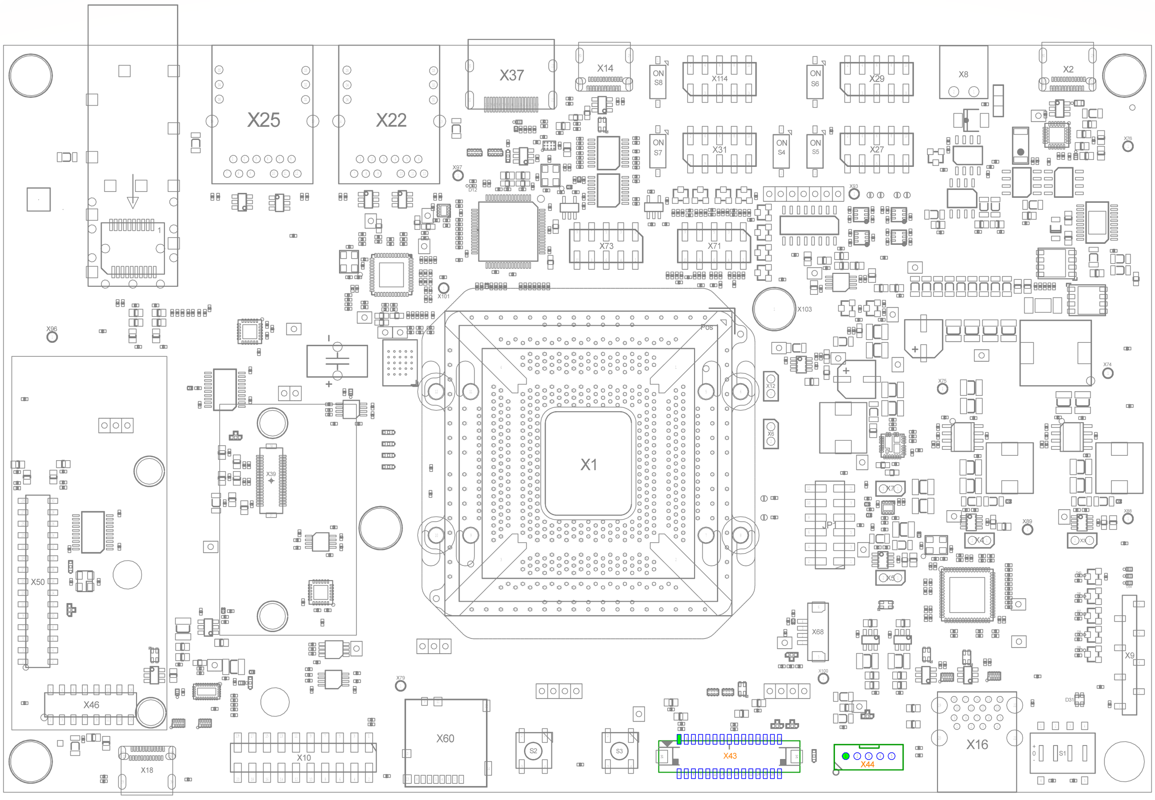


FIGURE 29: LVDS1 Connectors (X43/X44)

The phyFLEX FPSC SoM offers two LVDS display interfaces. The video connectors X43 and X44 provide an easy way to connect a display to the Libra Development Board. The pinout of both connectors fits the Glyn LVDS Display Family with different display sizes and display resolutions. In addition to the Glyn LVDS signals, there is I^2C for touch brought out at X34 as well. For USB-touch functionality please use the USB Dual Type-A connector X16. The connectors are intended to be used with PHYTEC KLCD-AC163. The tables below show the pin assignment of connectors X43 and X44.

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	NC	-	-	No connect
3	VDD_3V3	PWR_O	3.3 V	LVDS1 3.3 V power rail
4	GND	-	0.0 V	Ground
5	X_LVDS1_CLK_N	LVDS_O	-	LVDS clock negative signal
6	X_LVDS1_CLK_P	LVDS_O	-	LVDS clock positive signal
7	VDD_3V3	PWR_O	3.3 V	LVDS1 3.3 V power rail
8	GND	-	0.0 V	Ground
9	X_LVDS1_D0_N	LVDS_O	-	LVDS data 0 negative signal
10	X_LVDS1_D0_P	LVDS_O	-	LVDS data 0 positive signal
11	X_LVDS1_D1_N	LVDS_O	-	LVDS data 1 negative signal
12	X_LVDS1_D1_P	LVDS_O	-	LVDS data 1 positive signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_LVDS1_D2_N	LVDS_O	-	LVDS data 2 negative signal
14	X_LVDS1_D2_P	LVDS_O	-	LVDS data 2 positive signal
15	X_LVDS1_D3_N	LVDS_O	-	LVDS data 3 negative signal
16	X_LVDS1_D3_P	LVDS_O	-	LVDS data 3 positive signal
17	VDD_5V0	PWR_O	5.0 V	LVDS1 5.0 V power rail
18	GND	-	0.0 V	Ground
19	NC	-	-	No connect
20	NC	-	-	No connect
21	NC	-	-	No connect
22	GND	-	0.0 V	Ground
23	NC	-	-	No connect
24	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	NC	-	-	No connect
27	X_I2C3_SCL_3V3	O	3.3 V	I2C3 serial clock
28	GND	-	0.0 V	Ground
29	X_I2C3_SDA_3V3	I/O	3.3 V	I2C3 serial data
30	NC	-	-	No connect
31	NC	-	-	No connect
32	NC	-	-	No connect

TABLE 61: X43 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	VDD_12V0	PWR_O	12.0 V	LVDS1 12.0 V power rail for backlight
2	X_PWM1_LVDS_DSI_3V3	O	3.3 V	LVDS1 backlight PWM, choice between 3.3 V, 0 V and shared PWM signal (default) via J29
3	GND	-	0.0 V	Ground
4	GND	-	0.0 V	Ground
5	X_LVDS1_BL_EN	O	3.3 V	LVDS1 backlight enable

TABLE 62: X44 Pin Assignment

26.3.16.1 LVDS Design Considerations

The differential impedance of LVDS0 lanes should be 100 Ohm and 50 Ohm to a Ground-Plane for all lanes. The lanes should be matched.

26.3.17 MIPI-DSI (X39)

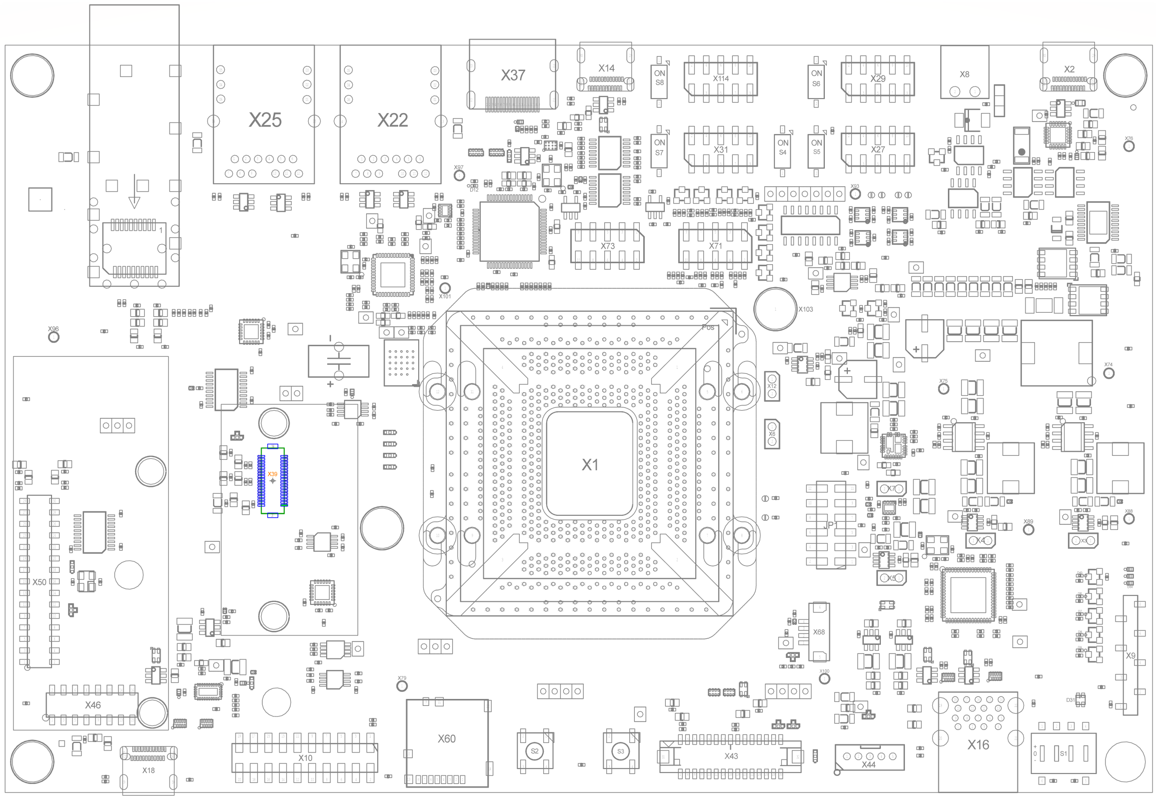


FIGURE 30: MIPI-DSI (X39)

The Libra Development Board offers one MIPI-DSI display interface. MIPI-DSI has 4 channels, supporting one display with a resolution of up to 1920 x 1080 at 60Hz. The following table shows the pin assignment of connector X39. This feature is not available for all mountable FPSC SoMs.

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	0.0 V	Ground
2	GND	-	0.0 V	Ground
3	X_MIPI_DSI1_D0_P	DSI_O	-	MIPI DSI data 0 positive signal
4	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in
5	X_MIPI_DSI1_D0_N	DSI_O	-	MIPI DSI data 0 negative signal
6	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in
7	GND	-	0.0 V	Ground
8	GND	-	0.0 V	Ground
9	X_MIPI_DSI1_D1_P	DSI_O	-	MIPI DSI data 1 positive signal
10	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in
11	X_MIPI_DSI1_D1_N	DSI_O	-	MIPI DSI data 1 negative signal
12	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	0.0 V	Ground
14	GND	-	0.0 V	Ground
15	X_MIPI_DSI1_CLK_P	DSI_O	-	MIPI DSI clock positive signal
16	VDD_5V0_MIPI_DSI	PWR_O	5.0 V	MIPI DSI 5.0 V power out rail
17	X_MIPI_DSI1_CLK_N	DSI_O	-	MIPI DSI clock negative signal
18	VDD_5V0_MIPI_DSI	PWR_O	5.0 V	MIPI DSI 5.0 V power out rail
19	GND	-	0.0 V	Ground
20	GND	-	0.0 V	Ground
21	X_MIPI_DSI1_D2_P	DSI_O	-	MIPI DSI data 2 positive signal
22	VDD_3V3_MIPI_DSI	PWR_O	3.3 V	MIPI DSI 3.3 V power out rail
23	X_MIPI_DSI1_D2_N	DSI_O	-	MIPI DSI data 2 negative signal
24	VDD_3V3_MIPI_DSI	PWR_O	3.3 V	MIPI DSI 3.3 V power out rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	GND	-	0.0 V	Ground
26	GND	-	0.0 V	Ground
27	X_MIPI_DSI1_D3_P	DSI_O	-	MIPI DSI data 3 positive signal
28	X_I2C4_SCL_3V3	O	3.3 V	I2C4 serial clock
29	X_MIPI_DSI1_D3_N	DSI_O	-	MIPI DSI data 3 negative signal
30	X_I2C4_SDA_3V3	I/O	3.3 V	I2C4 serial data
31	GND	-	0.0 V	Ground
32	GND	-	0.0 V	Ground
33	TP42	-	-	MIPI_DSI1_GPIO0 test point
34	X_PWM1_LVDS_DSI_3V3	O	3.3 V	MIPI DSI1 PWM, choice between 3.3 V, 0 V and shared PWM signal (default) via J31
35	TP43	-	-	MIPI_DSI1_GPIO1 test point
36	X_nRESET_OUT	O	3.3 V	Global reset output

Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	GND	-	0.0 V	Ground
38	GND	-	0.0 V	Ground

TABLE 63: X39 Pin Assignment

26.3.17.1 MIPI-DSI Design Considerations

The differential impedance of MIPI-DSI1 lanes should be 100 Ohm and 50 Ohm to a ground plane for all lanes. The lanes should be matched.

26.3.18 Fan (X68)

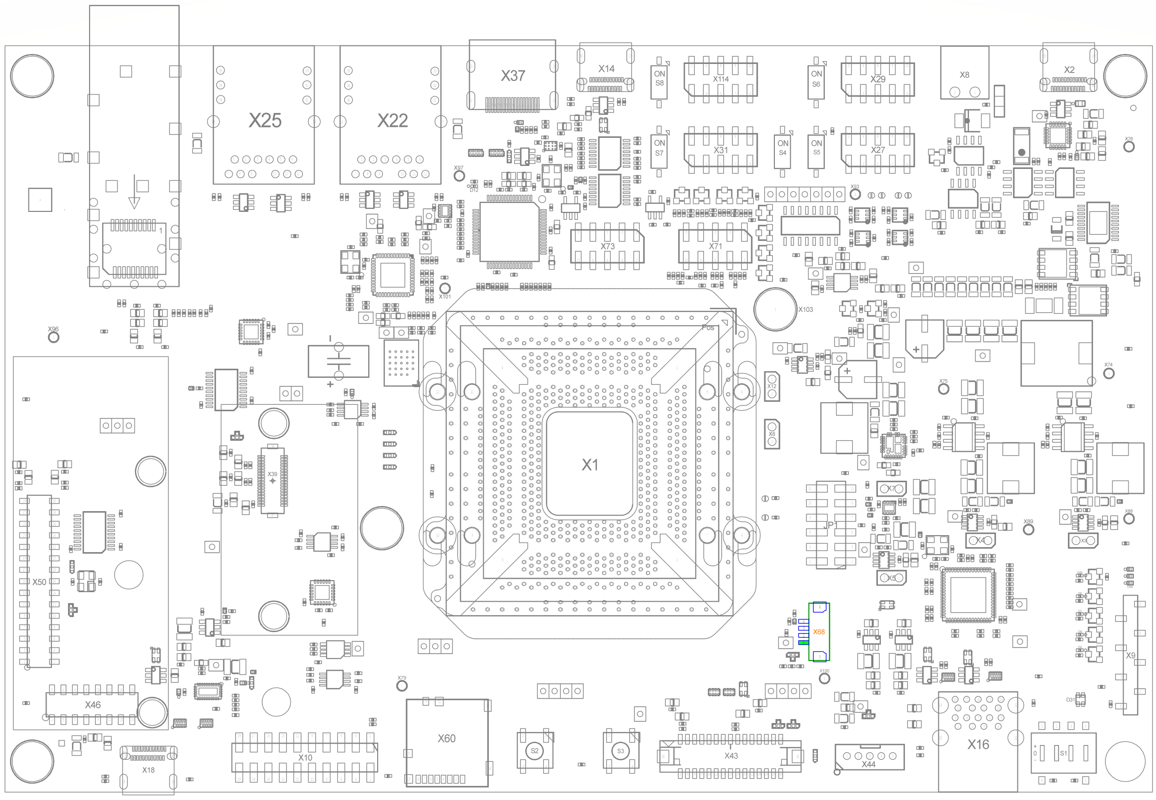


FIGURE 31: Fan (X68)

If heatsinking is required for the phyFLEX FPSC SoM, a PWM-controlled fan can be connected to the Libra Development Board. The fan's supply voltage is 5 V by default but can be changed to 12 V or VDD_IN (carrier board input voltage) via J19.The PWM signal is brought out as open drain pulled up to VDD_5V0 with a 4k7 resistor. The fan feedback signal, which can be used to monitor fan rotational frequency, is connected to X_FAN_FB and pulled up to VDD_1V8 via a 4k7 resistor.

A Hirose DF13-4P-1.25V (75) socket is used as a connector with the following pinout:

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	X_FAN_PWR	PWR_O	5.0 V	FAN power rail, choice to use 12 V or VDD_IN via J19
2	GND	-	0.0 V	Ground
3	X_FAN_FB	I	1.8 V	FAN feedback signal (2 pulses per revolution)
4	X_PWM_FAN	OD_O_PU	5.0 V	Open drain PWM out with pull-up to VDD_5V0
5	Pad1	-	0.0 V	Connected to Ground
6	Pad2	-	0.0 V	Connected to Ground

TABLE 64: X68 Fan Pinout

26.3.19 JTAG (X10)

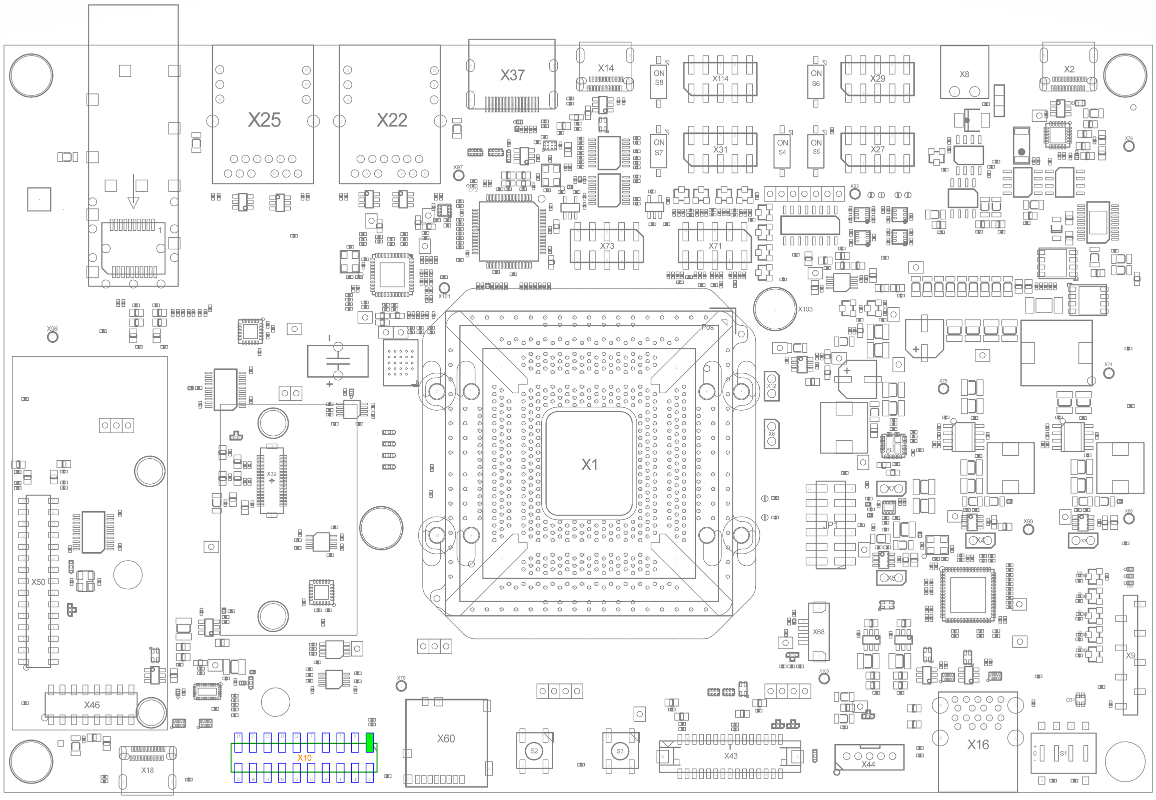


FIGURE 32: JTAG (X10)

The Libra Development Board provides a 2x10 2.54mm pin-header for JTAG connectivity. 1.8 V are available at the connector directly or with a 100R pull-up.

The JTAG connector X10 has the following pinout:

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	Pull-up VDD_1V8	PWR_O	1.8 V	100 Ω pull-up to 1.8 V power rail
2	VDD_1V8	PWR_O	1.8 V	1.8 V power rail
3	X_JTAG_TRST	I	1.8 V	Reset in signal
4	GND	-	0.0 V	Ground
5	X_JTAG_TDI	I	1.8 V	JTAG TDI
6	GND	-	0.0 V	Ground
7	X_JTAG_TMS	I	1.8 V	JTAG TMS
8	GND	-	0.0 V	Ground
9	X_JTAG_TCK	I	1.8 V	JTAG TCK
10	GND	-	0.0 V	Ground
11	X_JTAG_RTCK	I	1.8 V	JTAG Return Clock, no connect
12	GND	-	0.0 V	Ground

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
13	X_JTAG_TDO	O	1.8 V	JTAG TDO
14	GND	-	0.0 V	Ground
15	X_nRESET_IN	I	1.8 V	Reset in signal
16	GND	-	0.0 V	Ground
17	NC	-	-	No connect
18	GND	-	0.0 V	Ground
19	NC	-	-	No connect
20	GND	-	0.0 V	Ground

TABLE 65: X10 JTAG Connector Pinout

26.3.20 On-board Functionalities

26.3.20.1 Multicolor (RGB) LED (D31)

The Libra Development Board provides one multicolor (RGB) LED (D31). The LED is connected to an LED driver PCA9633TK controlled by the I2C3 bus. The location for D31 can be found in LEDs.

26.3.20.2 Factory EEPROM (U57)

The Libra Development Board provides a 2 kbit EEPROM (ST M24C02-RMC6TG) for factory data. It is connected to the I2C3 bus. The EEPROM's write protection pin is connected to TP60. Write protection can be enabled by mounting R333 (10k) pull-up resistor. In this case, the EEPROM can be written if TP60 is tied to Ground only. The EEPROM I^2C address can be fully customized by jumpers J21, 22, and 23. The default address is 0x51.

26.3.20.3 User EEPROM (U80)

The Libra Development Board provides a 2 kbit EEPROM (ST M24C02-RMC6TG) for general use. It is connected to the I2C3 bus. The EEPROM's write protection pin is connected to TP112. Write protection can be enabled by mounting R486 (10k) pull-up resistor. In this case, the EEPROM can be written if TP112 is tied to Ground only. The EEPROM I^2C address can be fully customized by jumpers J21, 22, and 23. The default address is 0x52.

26.3.20.4 Quad SPI NOR (U62)

The Libra Development Board features a 512MBit Quad SPI NOR at U62.

26.3.20.5 ADC (X73)

The Libra Development Board features 8 analog to digital channels depending on the mounted phyFLEX SOM. The inputs are used to measure carrier board voltages and currents. Maximum input voltage is 1.8 V. All input signals are available at 2.54mm pin-header X73 with the following pinout:

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VDD_1V8	PWR_O	1.8 V	1.8 V power rail
2	GND	-	0.0 V	Ground
3	ADC_AIN0	I	0.0 - 1.8 V	Analog input channel 0 - used for VDD_SOM current
4	ADC_AIN1	I	0.0 - 1.8 V	Analog input channel 1 - used for VDD_SOM voltage
5	ADC_AIN2	I	0.0 - 1.8 V	Analog input channel 2 - used for VDD_5V0 current
6	ADC_AIN3	I	0.0 - 1.8 V	Analog input channel 3 - used for VDD_5V0 voltage
7	ADC_AIN4	I	0.0 - 1.8 V	Analog input channel 4 - used for VDD_3V3 current
8	ADC_AIN5	I	0.0 - 1.8 V	Analog input channel 5 - used for VDD_3V3 voltage
9	ADC_AIN6	I	0.0 - 1.8 V	Analog input channel 6 - used for VDD_1V8 current
10	ADC_AIN7	I	0.0 - 1.8 V	Analog input channel 7 - used for VDD_1V8 voltage

TABLE 66: X73 ADC

26.3.20.6 SPI ADC (X71)

The Libra Development Board comes with an SPI-ADC U61 (MCP3208-BI/SL) with 8 channels, which are connected to carrier board current and voltage measurement devices. This SPI-ADC serves as a comparison betwenn itself and the on-board ADC, which is available depending on the mounted phyFLEX SOM. The SPI-ADCs maximum voltage is 5.0 V and the conversion method is SAR with a depth of 12 Bit. The SPI-ADC is connected to the SPI1 interface. The following table shows the pinout of pin-header X71 where all SPI-ADC input signals are available.

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VDD_5V0_REF	PWR_O	5.0 V	5.0 V reference voltage derived from precision voltage reference U78
2	GND	-	0.0 V	Ground
3	SPI_ADC_AIN0	I	0.0 - 5.0 V	Analog input channel 0 - used for VDD_SOM current
4	SPI_ADC_AIN1	I	0.0 - 5.0 V	Analog input channel 1 - used for VDD_SOM voltage
5	SPI_ADC_AIN2	I	0.0 - 5.0 V	Analog input channel 2 - used for VDD_5V0 current
6	SPI_ADC_AIN3	I	0.0 - 5.0 V	Analog input channel 3 - used for VDD_5V0 voltage
7	SPI_ADC_AIN4	I	0.0 - 5.0 V	Analog input channel 4 - used for VDD_3V3 current
8	SPI_ADC_AIN5	I	0.0 - 5.0 V	Analog input channel 5 - used for VDD_3V3 voltage
9	SPI_ADC_AIN6	I	0.0 - 5.0 V	Analog input channel 6 - used for VDD_1V8 current
10	SPI_ADC_AIN7	I	0.0 - 5.0 V	Analog input channel 7 - used for VDD_1V8 voltage

TABLE 67: X71 SPI-ADC

26.3.20.7 Temperature sensor (U56)

The Libra Development Board is equipped with a P3T1750DPZ I3C temperature sensor connected to I2C5. I2C address is 0x4F, I3C provisional ID is 0x9E.

26.3.20.8 TPM (U79)

The Libra Development Board features a Trusted Platform Module SLB9670. It is connected to SPI2 and offers TPM 2.0 functionality.

26.3.20.9 Peripheral current measurement (U5/U7/U9)

The Libra Development Board is equipped with current sensing devices which translate the momentary current load through a measurement resistor into a voltage value. This voltage value then can be interpreted by the phyFLEX SOM on-board ADC or the carrier board SPI-ADC or both at the same time. The current measurement ICs used are INA241A4QDDFRQ1 with a 0.004R 1% shunt resistor. The applicable gain factor is 100V/V. Which current measurement IC is connected to which ADC channel can be obtained from the section of the applicable ADC in this manual.

26.3.20.10 Global Board Reset (X_nRESET_OUT)

The X_nRESET_OUT signal (X_POR_B at phyFLEX FPSC SoM) is used to hold all devices with an external reset pin in the reset state. X_nRESET_OUT will be released after all board voltages are powered up and allows the phyFLEX FPSC SoM to boot. X_nRESET_OUT is brought out at several connectors.

X_nRESET_OUT Design Considerations

Note that there is a 10 kOhms pull-up resistor on the phyFLEX FPSC SoM VDD_IO voltage. It is recommended to use this signal as an open drain.

26.3.20.11 On-board Power Supplies

The Libra Development Board provides supply voltages on several connectors to power external devices. Be sure not to exceed the maximum permissible current that can be drawn from each power domain. In the table below, each source is listed with the location where a voltage connected to the source can be found:

Voltage Domain	**Locations**	**Max. recommended additional current**
VDD_IN	TP1, X39(VDD_IN_MIPI), X46(VDD_IN_AV), X117	Depends on used input power supply connected to the carrier board
VDD_12V0	TP3, X44(VDD_12V0_LVDS1), X117	TBD
VDD_SOM	TP4	TBD

Voltage Domain	Locations	Max. recommended additional current
VDD_5V0	TP6, X39(VDD_5V0_MIPI_DSI), X43(VDD_5V0_LVDS1), X50(VDD_5V0_AV), X117	TBD
VDD_3V3	TP7, X39(VDD_3V3_MIPI_DSI), X43(VDD_3V3_LVDS1), X50(VDD_3V3_AV), X52, X54, X114	TBD
VDD_3V3_OUT	X6	200 mA
VDD_1V8	TP8, X9, X10, X114	200 mA (derived from VDD_1V8_OUT, currents from both cannot exceed 200 mA cumulatively)
VDD_1V8_OUT	X7	200 mA

TABLE 68: Onboard Power Supplies

In addition to these currents, Libra Development Board delivers current for USB_VBUS of X16/X18 (3x 900 mA), phyCAM-M Interfaces (2x 1500 mA 3.3 V or 5 V depending on VCC_SELECT pin), HDMI connector (150 mA).

Warning

Drawing current may result in heating of the voltage regulator components and might require additional heat sinking.

26.3.20.12 On-board Measurement of SoM Power Consumption

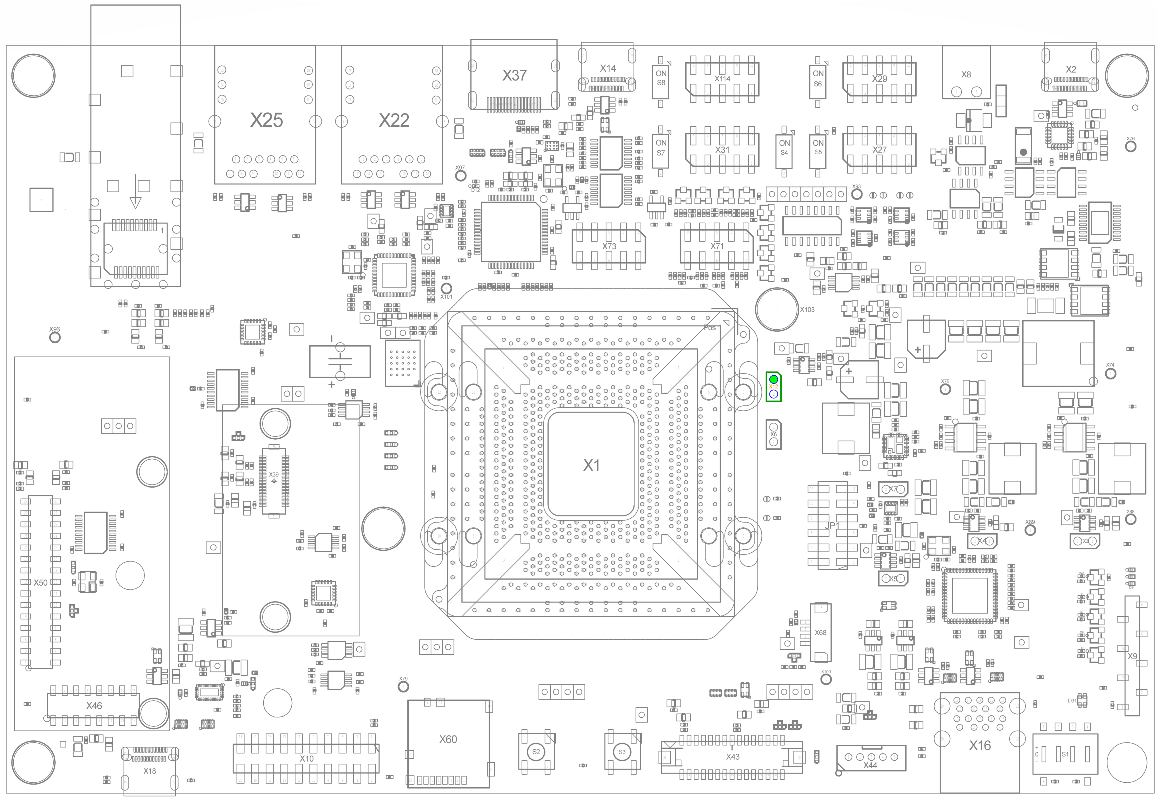


FIGURE 33: SoM Input Current Amp Header (X12)

The input current of the SoM supply rail VDD_SOM can be measured on board to determine the power consumption of the SOM. A current sense amplifier translates the supply current into a proportional voltage VOUT_CC_SOM, which can be measured at X12 (on PCB top side) and X12 (on PCB bottom side). The mounted amplifier features a gain of 100V/V. The SoM input current I_{SOM_IN} in Ampere is determined by inserting VOUT_CC_SOM into the following equation.

Subsequently, the SoM input power may be derived from I_{SOM_IN} and VOUT_CC_SOM using the following formula:

For example, measuring 400 mV at X12, the input current will be 1 A. With a SoM input voltage of 5.0 V, the input P_{SOM_IN} is 5 W.

26.3.21 Switches

The Libra Development Board has several switches and buttons for various uses. The locations for all switches can be found in Switches and Buttons.

26.3.21.1 System Reset Button (S2)

The Libra Development Board is equipped with a system reset button at S2. Pressing this button will assert reset through a voltage supervisor U11 that will pull the X_nRESET_IN pin (X1 Pin Y21) of the phyFLEX FPSC SoM low, causing the module to reset with a complete power cycle.

26.3.21.2 System ON/OFF Button (S3)

The Libra Development Board is equipped with an ON/OFF button at S3 and is connected to X_ONOFF of the phyFLEX FPSC SoM. For more information, refer to the applicable CPU's *Reference Manual*.

26.3.21.3 Boot Switch (S1)

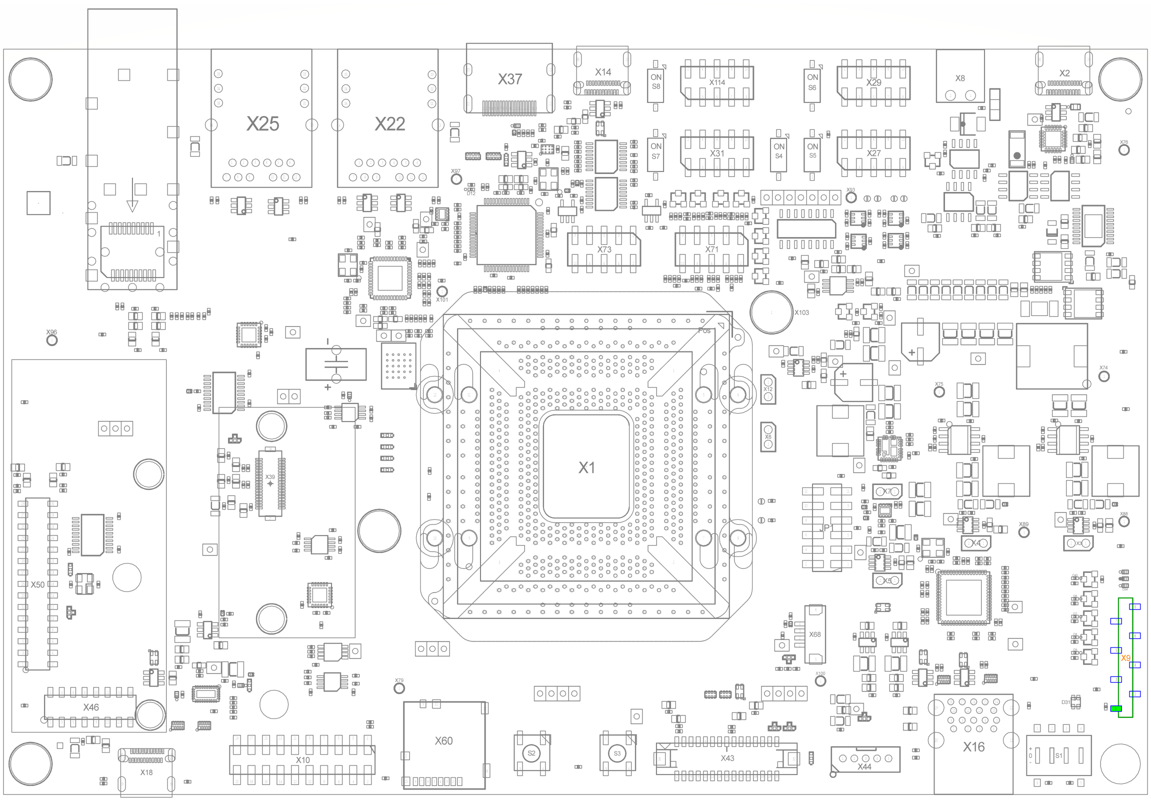


FIGURE 34: Boot Header (X9)

The Libra Development Board features a tri-state boot switch with four individually switchable ports to select the phyFLEX FPSC SoM default bootsource. The Boot_Mode signals may also be accessed through pin header X9 or USB to UART/GPIO converter U15. Descriptions of the various boot modes can be found in Boot Mode Selection. The available boot options differ depending on the mounted phyFLEX SoM. All available options are displayed in the table below. Default boot modes are marked red, the phyFLEX SOM will boot default when no boot mode alteration is engaged:

Boot Mode designation	
1	High
0	Low
X	Don't care
Boot Switch designation	
1	Pull-up
0	Pull-down
-	Middle setting, open

Mounted SoM	**Boot Target**	**Memory/Target Location**	**BOOT_MODE**				**S1 Switch Number**			
			3	**2**	**1**	**0**	**4**	**3**	**2**	**1**
PFL-G-01 (FPSC phyFLEX-i.MX 8MP)	**eMMC (SoM default)**	SOM	0	0	1	0	-	-	-	-

Mounted SoM	**Boot Target**	**Memory/Target Location**	**BOOT_MODE**				**S1 Switch Number**			
			3	**2**	**1**	**0**	**4**	**3**	**2**	**1**
	SD-Card	CarrierBoard	0	0	1	1	-	-	-	1
	QSPI NOR	CarrierBoard	0	1	1	0	-	1	-	-
	USB1 serial downloader	SOM	0	0	0	1	-	-	0	1
	Fuse boot	SOM	0	0	0	0	-	-	0	-
	JTAG mode	SOM	1	1	1	1	1	1	-	1

Mounted SoM	**Boot Target**	**Memory/Target Location**	**BOOT_MODE**				**S1 Switch Number**			
			3	**2**	**1**	**0**	**4**	**3**	**2**	**1**
PFL-G-02 (FPSC phyFLEX-i.MX 95)	**eMMC (SoM default)**	SOM	1	0	1	0	-	-	-	-
	SD-Card	CarrierBoard	1	0	1	1	-	-	-	1
	QSPI NOR	CarrierBoard	1	1	0	0	-	1	0	-
	USB1 serial downloader	SOM	1	0	0	1	-	-	0	1
	Fuse boot	SOM	1	0	0	0	-	-	0	-

Mounted SoM	Boot Target	Memory / Target Location	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
PFL-G-03 (FPSC phyFLEX-AM62L)	**MMC0 eMMC FS (SOM default)**	SOM	1	0	1	1	-	-	-	-
	USB0 Host MSC	SOM	0	1	1	1	0	1	-	-
	MMC0 eMMC FS	SOM	1	0	0	0	-	-	0	0
	FSS0 QSPI CS0	Carrier Board	1	0	0	1	-	-	0	-
	MMC1 4b UDA FS	SOM	1	0	1	1	-	-	-	-
	DEVBOOT	SOM	0	1	1	0	0	1	-	0

Mounted SoM	**Boot Target**	**Memory/Target Location**	**BOOT_MODE**				**S1 Switch Number**			
			3	**2**	**1**	**0**	**4**	**3**	**2**	**1**
	FSS0 Serial NAND		1	1	0	0	-	1	0	0
	FSS0 xSPI SFDP		1	1	0	1	-	1	0	-
	EXT. HOST UART0		1	1	1	0	-	1	-	0
	EXT. HOST USB0 DFU		1	1	1	1	-	1	-	-
PFL-G-04 (FPSC phyFLEX-STM 32MP2)	**eMMC (SoM default)**	SOM	0	0	1	0	-	-	-	-
	UART and USB	SOM	0	0	0	0	-	-	0	-
	SD-Card	CarrierBoard	0	0	0	1	-	-	0	1

Mounted SoM	Boot Target	Memory/Target Location	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
	Development	SOM	0	0	1	1	-	-	-	1
	QSPI NOR	Carrier Board	0	1	0	0	-	1	0	-
PFL-G-05 (FPSC phyFLEX-i.MX 93) A55 boot	**eMMC (SoM default)**	SOM	0	0	1	0	-	-	-	-
	USB1 serial downloader	SOM	0	0	0	1	-	-	0	1
	Fuse boot	SOM	X	0	0	0	-	-	0	-

Mounted SoM	**Boot Target**	**Memory/TargetLocation**	**BOOT_MODE**				**S1 Switch Number**			
			3	**2**	**1**	**0**	**4**	**3**	**2**	**1**
	SD-Card	CarrierBoard	0	0	1	1	-	-	-	1
	QSPI NOR	CarrierBoard	0	1	0	0	-	1	0	-

Mounted SoM	Boot Target	Memory/Target Location	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
PFL-G-05 (FPSC phyFLEX-i.MX 93) M33 boot	eMMC	SOM	1	0	1	0	1	-	-	-
	USB1 serial downloader	SOM	1	0	0	1	1	-	0	1
	Fuse boot	SOM	X	0	0	0	-	-	0	-
	SD-Card	Carrier Board	1	0	1	1	1	-	-	1

Mounted SoM	Boot Target	Memory/Target Location	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
	QSPI NOR	Carrier Board	1	1	0	0	1	1	0	-

TABLE 69: Boot Configuration Options (S1)

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VDD_1V8	PWR_O	1.8 V	1.8 V power rail
2	X_BOOT_MODE0	I	1.8 V	Boot mode 0 configuration signal
3	X_BOOT_MODE1	I	1.8 V	Boot mode 1 configuration signal
4	X_BOOT_MODE2	I	1.8 V	Boot mode 2 configuration signal
5	X_BOOT_MODE3	I	1.8 V	Boot mode 3 configuration signal
6	X_nRESET_IN	I	1.8 V	Reset in signal
7	NC	-	-	No connect
8	GND	-	0.0 V	Ground

TABLE 70: Boot Mode Configuration Header Pinout (X9)

Boot Mode Design Considerations

Bootpin voltages should be valid when X_POR_B (X_nRESET_IN at Libra Development Board) is released.

27 Additional System-Level Hardware Information

27.1 I2C Connectivity

The I2C1 interface of the phyFLEX FPSC SoM is not connected to the Libra Development Board. The table below lists the connectors and pins with I2C connectivity and on-board devices. The I²C addresses are hexadecimal in 7-bit representation of the default Linux representation.

I2C2 Interface	Location and/or Address
STUSB4500QTR	U1 - 0x28
M.2 Key-M	X54
Factory EEPROM	U57 - 0x51
User EEPROM	U80 - 0x52
TCAL6416RTW	U58 - 0x21
phyCAM-M CSI2 VM-016	X34 - 0x18, 0x57
phyCAM-M CSI2 VM-017	X34 - 0x37, 0x57
phyCAM-M CSI2 VM-020	X34 - 0x18, 0x57
MIPI-DSI / PEB-AV-12	X39 - 0x10, 0x24, 0x2C, 0xeE

TABLE 71: I2C2 Connectivity

I2C3 Interface	Location or Address
TUSB8042A	U21 - 0x44
phyCAM-M CSI1 VM-016	X32 - 0x10, 0x56
phyCAM-M CSI1 VM-017	X32 - 0x36, 0x56
phyCAM-M CSI1 VM-020	X32 - 0x10, 0x56
LVDS1 Connector	X43; connecting jumpers are not mounted by default
M.2 Key-E	X52
PCA9533/01	U55 - 0x62

I2C3 Interface	Location or Address
TCAL6416RTW	U72 - 0x21
HD3SS3220I	U66 - 0x47
PEB-AV-10 LVDS2	X50 - 0x18, 0x57, 0x5F
PEB-AV-13 LVDS2	X50 - 0x34

TABLE 72: I2C3 Connectivity

I2C4 Interface	Location or Address
SFP+	X113 - 0xA0, 0xA2

TABLE 73: I2C4 Connectivity

I2C5 Interface	Location or Address
P3T1750DPZ I2C	U56 - 0x4F
P3T1750DPZ I3C	U56 - 0x9E

TABLE 74: I2C5 Connectivity

To avoid conflicts when connecting external I2C devices to the Libra Development Board, the addresses of the onboard I2C devices must be considered. The table below lists the addresses already in use; the default address is printed in bold. The I^{2}C addresses are hexadecimal in 7-bit representation, which is the default Linux representation.

Bus	Connector	Prod. No.	Addresses
I2C3	phyCAM-M CSI1 Connector X32	VM-016-xxx-M	**0x10**, 0x18
		VM-017-xxx-M	**0x36**, 0x37
		VM-117-xxx-M	**0x36**, 0x37
		VM-017-xxx-L	**0x36**, 0x37, **0x18**
		VZ-018	**0x3D**, 0x38
I2C4	phyCAM-M CSI1 Connector X34	VM-016-xxx-M	**0x10**, 0x18
		VM-017-xxx-M	**0x36**, 0x37
		VM-117-xxx-M	**0x36**, 0x37

Bus	Connector	Prod. No.	Addresses
		VM-017-xxx-L	**0x36**, 0x37, **0x18**
		VZ-018	**0x3D**, 0x38

TABLE 75: Reserved I2C Addresses
The Libra Development Board

28 Revision History

Date	Version #	Changes in this manual
08.11.2024	L-1075e.A0	Preliminary Manual Describes the phyCORE-i.MX 95 FPSC SOM Version: 1620.0
10.01.2025	L-1075e.A1	Added: Describes the Libra Development Board PCB Version: 1618.0
02.10.2025	L-1075e.A2	Updated: SOM Version : 1620.3 Changed: phyCORE-i.MX 95 to phyFLEX-i.MX 95
01.02.2026	L-1075e.A3	Updated: PCB Version: 1618.2

TABLE 76: Revision History

29 Contact Information

If you have any questions, design considerations, or are interested in further information, please contact your nearest PHYTEC office.

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Done	James Edmisten	State	changed state to Done at 10:22 AM	v10
In Progress	James Edmisten	State	gave *Review* approval at 10:22 AM	
	James Edmisten	Edit	updated the page at 10:13 AM	
	James Edmisten	State	changed state to In Progress at 9:58 AM	v8
Done	James Edmisten	Edit	updated the page at 9:58 AM	
02 20, 2026				
	James Edmisten	State	changed state to Done at 3:19 PM	v7
In Progress	James Edmisten	State	gave *Review* approval at 3:19 PM	
		State	changed state to In Progress at 3:19 PM	v7
Done	James Edmisten	Edit	updated the page at 3:19 PM	
		State	changed state to Done at 3:18 PM	v6

02 23, 2026	Actor	Type	Activity	Version
In Progress	James Edmisten	State	gave *Review* approval at 3:18 PM	
		Edit	updated the page at 3:18 PM	
		State	changed state to In Progress at 3:16 PM	v5
Done	James Edmisten	Edit	updated the page at 3:16 PM	
10 31, 2025				
	James Edmisten	State	changed state to Done at 8:59 AM	v4
In Progress	James Edmisten	State	gave *Review* approval at 8:59 AM	
		State	changed state to In Progress at 8:56 AM	v4
Done	James Edmisten	Edit	updated the page at 8:56 AM	
10 13, 2025				
	James Edmisten	State	changed state to Done at 12:29 PM	v3
In Progress	James Edmisten	State	gave *Review* approval at 12:29 PM	
		Edit	updated the page at 12:29 PM	
10 02, 2025				

02 23, 2026	Actor	Type	Activity	Version
	James Edmisten	State	changed state to In Progress at 11:17 AM	v2
Done	James Edmisten	Edit	updated the page at 11:17 AM	
		State	changed state to Done at 10:31 AM	v1
In Progress	James Edmisten	State	gave *Review* approval at 10:31 AM	
		State	changed state to In Progress at 10:31 AM	v1
Start	James Edmisten	State	changed state to Start at 10:30 AM	v1
	James Edmisten	Edit	created the page at 10:30 AM	