Hardware Manual - phyFLEX-i.MX 91/93 FPSC/Libra Development Board (1634.0/1618.2) (L-1089e.A0)

Please Note
This is an ALPHA Hardware Manual. Changes will be made with no notice.

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Warning

This product is currently in the ALPHA stage. This is a preliminary version of the hardware manual for this product. Check back for future updates to this product and its associated documentation.

1 Information on this Manual

This hardware manual describes the PFL-G-05 System on Module, referred to as phyFLEX®-i.MX 91/93 FPSC, and the PBA-BG-41, referred to as the Libra Development Board. This manual also specifies the phyFLEX-i.MX 91/93 FPSC and Libra Development Board's design and function. Precise specifications for the NXP® Semiconductor i.MX 91/93 microcontrollers can be found in the *i.MX 91/93 Microcontroller Data Sheet/Reference Manual*.

There will be several changes and additions to this manual. New versions will be released in the future with no notice. Please make sure that you are using the latest version of this manual when working with your product.

1.1 Future Proof Solder Core

The PFL-G-05 System on Module, referred to as phyFLEX®-i.MX 91/93 FPSC is designed according to FPSC Gamma Feature Set Specifications (LAN-118e.A6). For details about designing modules with FPSC Gamma Feature set, please see our Design-In Guide - FPSC Gamma Feature Set (LAN-123e.A5).

1.2 Design Considerations

The schematics shown in this hardware manual are believed to be correct. However, correctness can not be guaranteed. The schematics have been pulled from PHYTEC's designs that have been built, tested, and are known to work. The schematics have been re-formatted to fit better in this hardware manual.

Many hardware examples and suggestions are given on the following pages. Designing the phyFLEX System on Module onto a Carrier Board is generally straightforward. However, before committing to a particular active component selection when designing a carrier board, it is wise to check out the software driver support for those components. For example, a particular device may be supported in Linux but not Windows Embedded Compact 7. Your overall project may go smoother if you pick components that are already supported in your target OS. The premade selections for our reference designs, for example, our Single Board Computers, are typically focused on using components that are well supported under Linux.

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyFLEX-i.MX 91/93 FPSC on the Libra Development Board. Be aware that not all components need to be considered when designing your carrier board.

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These manuals and more can be found in the download section of phyFLEX-i.MX 91/93 FPSC Product Page.

2 Conversions, Abbreviations, and Acronyms

Tip

Due to part maintenance for our products (which are subject to continuous changes), we refrain from providing detailed, part-specific information within this manual. Please read the section Product Change Management and Information Regarding Parts Populated on the SoM / SBC within the Preface for more information.

Tip

The BSP delivered with the phyFLEX-i.MX 91/93 usually includes drivers and/or software for controlling all components, such as interfaces, memory, etc. Programming close to hardware at the register level is not necessary in most cases. For this reason, this manual does not contain detailed descriptions of the controller's registers or information relevant to software development. Please refer to the i.MX 91/93 Reference Manual, if any information not found in this manual is needed to connect customer-designed applications.

2.1 Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or “#”character (e.g., nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g., RD), are designated as active low signals. That means their active state is when they are driven low or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB, which depends on the desired command (read (1) or write (0)), must be added to get the complete address byte. For example, if the given address in this manual is 0x41 =>, the complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables that describe all settings show the default position in **bold, blue text**.
- Text in blue indicates a hyperlink within or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.

References made to the phyFLEX-Connector always refer to the high-density Soldering pads on the underside of the phyFLEX-i.MX 91/93 System on Module.

2.2 Types of Signals

Different types of signals are brought out at the phyFLEX-Connector. The following table lists the abbreviations used to specify the type of signal.

TABLE 1: Signal Types

Signal Type	Description	Abbreviation
Power In	Supply voltage input	PWR_I
Power Out	Supply voltage output	PWR_O
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
I/O	Bidirectional input/push-pull output	I/O
Input/OD-Output	Input / open-drain output requires an external pull-up	I/OD
OC-Bidir PU	Open collector input/output with pull-up	OC-BI-PU
OC-Output	Open-collector output without a pull-up requires an external pull-up	OC
OD-Bidir PU	Open-drain input/output with pull-up	OD-BI-PU
OD-Output	Open-drain output without pull-up requires an external pull-up	OD
5 V Input PD	5 V tolerant input with pull-down	5V-PD
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI2_I
MIPI DSI-2 Output	Differential line pairs 100 Ohm MIPI DSI-2 level output	DSI2_O

Signal Type	Description	Abbreviation
CAN FD IO	Differential line pairs 120 Ohm CAN FD level bidirectional input/output	CAN_I/O

2.3 Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the following table to navigate unfamiliar terms used in this document.

TABLE 2: Abbreviations and Acronyms Used in this Manual

	Abbreviation	Definition
1	BGA	Ball Grid Array
2	BSP	Board Support Package (software delivered with the Development Kit, including an operating system (Windows or Linux) preinstalled on the module and development tools)
3	CB	Carrier board; used with the phyFLEX development kit carrier board
4	EMI	Electromagnetic Interference
5	GPI	General-purpose input
6	GPIO	General-purpose input and output
7	GPO	General-purpose output
8	IRAM	Internal RAM: the internal static RAM on the NXP® Semiconductor i.MX 91/93 microcontroller
9	J	Solder jumpers; these types of jumpers require solder equipment to remove and place
10	JP	Solderless jumpers; these types of jumpers can be removed and placed by hand with no special tools
11	OEM	Original Equipment Manufacturers
12	PCB	Printed circuit board
13	PCM	Product Change Management
14	PCN	Product Change Notification
15	PMIC	Power management IC

	Abbreviation	Definition
16	RTC	Real-time clock
17	SBC	Single Board Computer
18	SMT	Surface mount technology
19	SoM	System on Module; used in reference to the PFL-G-05/ phyFLEX®-i.MX 91/93 FPSC module
20	Sx	User button Sx (e.g., S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board
21	Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board
22	VM	Virtual Machine

3 phyFLEX-i.MX 91/93 FPSC Introduction

The phyFLEX-i.MX 91/93 belongs to PHYTEC's phyFLEX System on Module family. The phyFLEX SOMs represent the continuous development of the PHYTEC System on Module technology. Like its mini-, micro-, and nanoMODUL predecessors, phyFLEX boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

Independent research indicates that approximately 70 % of all EMI (Electromagnetic interference) problems are caused by insufficient supply voltage grounding of electronic components in high-frequency environments. The phyFLEX board design features an increased pin package, which allows for the dedication of approximately 20 % of all connector pins on the phyFLEX boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyFLEX boards, even in high-noise environments.

phyFLEX boards achieve their small size through modern SMT and multi-layer design. Due to the complexity of our modules, 0201-packaged SMT components and laser-drilled microvias are used on the boards, providing phyFLEX users with access to this cutting-edge miniaturization technology for integration into their own design.

The phyFLEX-i.MX 91/93 is a subminiature (40 mm x 37 mm) insert-ready System on Module populated with the NXP® Semiconductor i.MX 91/93 microcontroller. Its universal design enables it to be inserted into a wide range of embedded applications. All controller signals and ports extend from the controller to surface mount technology (**FPSC FTGA 1.27 mm grid**) connectors, aligning four sides of the board, allowing it to be soldered into any target application like a "big chip".

The descriptions in this manual are based on the NXP® Semiconductor i.MX 91/93. Descriptions of compatible microcontroller derivative functions are not included, as such functions are not relevant for the basic functioning of the phyFLEX-i.MX 91/93.

3.1 phyFLEX-i.MX 91/93 FPSC Features

The phyFLEX-i.MX 91/93 offers the following features:

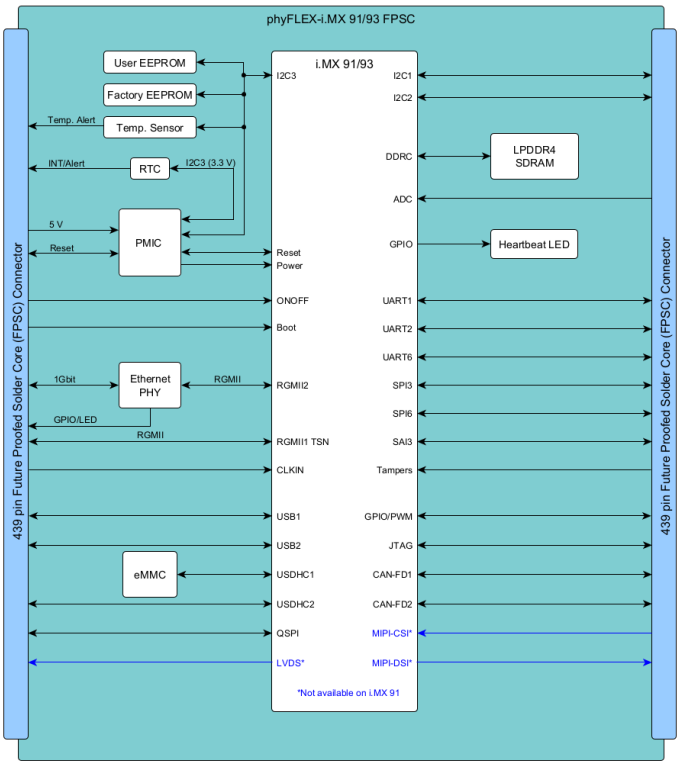
- Insert-ready, sub-miniature (40 mm x 37 mm) System on Module (SoM) subassembly in low EMI design, achieved through advanced SMD technology
- Mounted using FTGA Direct Solder Connector (FPSC FTGA)
- Populated with the NXP® Semiconductor i.MX 91/93 microcontroller (FCBGA 306 11x11 mm packaging)
- Up to 2 ARM-A55 cores (clock frequency up to 1.7 GHz) (for phyFLEX-i.MX 91 only one ARM-A55 core and clock frequency up to 1.4 GHz)
- 1x Cortex M33 core (250 MHz)[1]
- Neural Network Accelerator[1] (Arm® Ethos™ U-65 microNPU up to 0.5 TOPS)
- PXP 2D GPU: blending/composition, resizing, color space conversion[1]
- Boot from different memory devices (eMMC Flash standard)
- Single supply voltage of +5 V with on-board power management
- IO voltage between 1.8 V (default) and 3.3 V (factory assembly option)
- All controller-required supplies are generated on board using sophisticated on-board Power Management
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- up to 2 GB[2] LPDDR4/LPDDR4X[1] RAM
- up to 256 GB[2] on-board eMMC in the commercial temperature range (up to 64 GB for I-Temp)
- 1x Quad SPI, including support for SPI NOR and SPI NAND memories
- 4 kB[2] I^2C User-EEPROM and 4 kB I^2C Factory-EEPROM
- 2x USB 2.0 Type C with PHY

- 2x 1Gbit Ethernet interfaces with TSN[1] support (either one of them with Ethernet transceiver on the phyFLEX-i.MX 91/93 enabling a direct connection to an existing Ethernet network; the second as RGMII Signals at logic-level at the signal pins instead.)
- 2x I^2C (up to 8) interfaces
- 2x SPI (up to 8) interfaces
- 3x LPUART (up to 8) interfaces
- 2x CAN-FD interfaces
- 2x PWM outputs (up to 6x Timer/PWM)
- 1x MIPI CSI-2 camera interfaces[1]
- 1x MIPI DSI-2 display interface
- 1x LVDS interface[1]
- 1x 8-bit uSDHC for eMMC
- 1x 4-bit SD-Card interface
- 1x 4-bit SDIO interface or QSPI interface
- 1x SAI (up to 2) audio interface
- 1x JTAG interface
- Extreme Low Power RTC Module
- 1x temperature sensor
- Tamper detection
- All processor interfaces are available at the SoM Connector
- Available for different temperature grades (see Product Temperature Grades)

1. only for phyFLEX-i.MX 93
2. The maximum memory size is listed as of the printing of this manual.
   Please contact PHYTEC for more information about additional or new module configurations available.

3.2 phyFLEX-i.MX 91/93 FPSC Block Diagram

FIGURE 1: phyFLEX-i.MX 91/93 Block Diagram



3.3 phyFLEX-i.MX 91/93 FPSC Component Placement

FIGURE 2: phyFLEX-i.MX 91/93 FPSC Component Placement (1634.0 Top View)

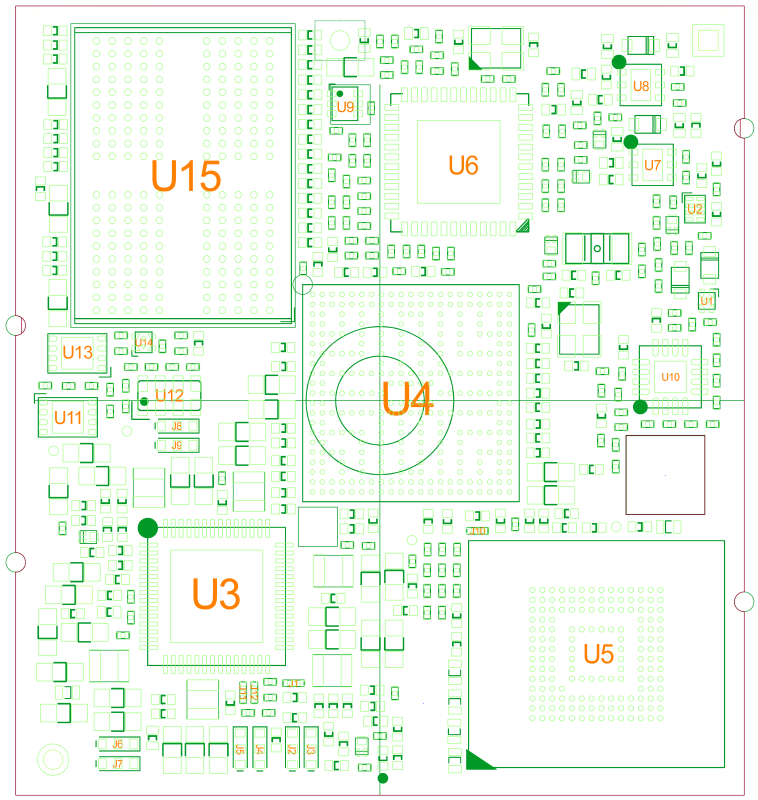
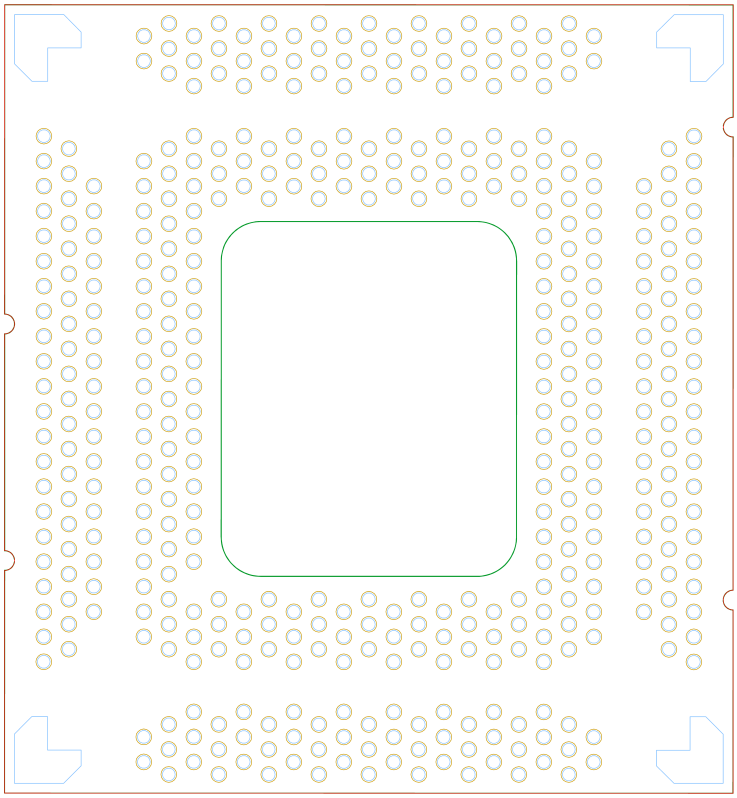


FIGURE 3: phyFLEX-i.MX 91/93 FPSC Component Placement (1634.0 Bottom View)



3.4 phyFLEX-i.MX 91/93 FPSC Minimum Operating Requirements

Warning

We recommend connecting all available VIN (+5.0 V) input contacts to the power supply system on a custom carrier board housing the phyFLEX-i.MX 91/93 FPSC. In addition, proper implementation of the phyFLEX-i.MX 91/93 FPSC module into a target application also requires connecting all GND contacts.

Refer to Power for more information.

Before the phyFLEX-i.MX 91/93 FPSC can be used; please make sure the host system meets the minimum operating requirements. These include:

- The stable and clean input power supply of 5.0 V with low ESR bulk capacitors (e.g. 2x 47 µF/16V MLCC) paired with some HF blocking capacitors (e.g. 100 nF MLCC) connected to the input pins as near as possible (phyFLEX-i.MX 91/93 Power Consumption)
- Supply voltage for externally connected peripherals should be controlled by signal X_nPWR_READY to avoid reverse currents (External Logic IO Supply Voltage)
- If external peripherals need a longer reset delay, hold the reset signal X_nRESET_IN as long as needed (Reset)
- Desired boot configuration - default configuration is "Boot from on-board eMMC" (System Boot Configuration)
- To back up the on-board I^2C-RTC, connect a buffer voltage source to input pin X_RTC_VBACKUP (Backup Power (X_RTC_VBACKUP), RTC)

4 Pin Description

Warning

Module connections **must** not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/datasheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All controller signals extend to the FPSC footprint. These contacts line four sides of the module (referred to as the FPSC footprint). This enables phyFLEX-i.MX 91/93 to be plugged into any target application like a "big chip".

PHYTEC provides a complete pinout table for the phyFLEX-i.MX 91/93 Connector (X1). This table contains a complete signal path for the phyFLEX-i.MX 91/93 and the Libra Development Board, including signal names, pin muxing paths, and descriptions specific to each pin. It also provides the appropriate voltage domain, signal type (ST), and a functional grouping of the signals. The signal type also includes information about the signal direction. A table describing the signal types can be found with the phyFLEX-i.MX 91/93 Pinout Table.

Warning

- The NXP® Semiconductor i.MX 91/93 is a multi-voltage operated microcontroller, and, as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *NXP Semiconductor i.MX 91/93 Reference Manual* for details on the functions and features of controller signals and port pins.
- As some of the signals which are brought out on the phyFLEX-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals that may affect the boot configuration are shown in the phyFLEX-Connector Boot Configuration Pins.
- It is necessary to avoid voltages at the IO pins of the phyFLEX-i.MX 91/93 FPSC, which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up or power-down. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the i.MX 91/93 are supposed to be powered while the phyFLEX-i.MX 91/93 FPSC is in suspend mode or turned off. To avoid this, bus switches are either supplied by VDD_1V8 on the phyFLEX side or have their output enabled to the SOM controlled by the X_nPWR_READY signal (see Supply Voltage for External Logic) must be used.

Pin Muxing Warning

If pin settings are changed from the PHYTEC standard configuration, make sure that the setting of the pull resistors are adjusted accordingly. Never rely on the SoC-internal pull resistor.

5 Unused Signals

Unused signals should be set according to the table below:

TABLE 3: Unused Signals

Interface	Signals	Recommendation
ADC	X_ADC_INx	Tie to GND
TAMPER	X_TAMPERx	Tie to GND
CLKIN	X_CLKIN1 X_CLKIN2	Tie to ground through 10 KΩ resistors
LVDS	X_LVDS_CLK_N X_LVDS_CLK_P X_LVDS_Dx_N X_LVDS_Dx_P	Tie to ground through 10 KΩ resistors
MIPI-CSI	X_MIPI_CSI1_CLK_P X_MIPI_CSI1_CLK_N X_MIPI_CSI1_Dx_P X_MIPI_CSI1_Dx_N	Leave unconnected
MIPI-DSI	X_MIPI_DSI1_CLK_P X_MIPI_DSI1_CLK_N X_MIPI_DSI1_Dx_P X_MIPI_DSI1_Dx_N	Leave unconnected
USB1	X_USB1_VBUS X_USB1_D_N X_USB1_D_P X_USB1_ID	Leave unconnected
USB2	X_USB2_VBUS X_USB2_D_N X_USB2_D_P X_USB2_ID	Leave unconnected
ETHERNET	X_ENET2_TX+ X_ENET2_TX- X_ENET2_RX+ X_ENET2_RX-	Leave unconnected
GPIO	All remaining single-ended signals	Leave unconnected

6 Jumpers

For configuration purposes, the phyFLEX-i.MX 91/93 FPSC (PFL-G-05) has several solder jumpers, some of which have been installed before delivery. A typical Jumper Pad Numbering Scheme illustrates the numbering of the solder jumper pads while Jumper Locations (top view) indicate the location and the default configuration of the solder jumpers on the board. There are also a few jumpers on the Libra Development Board. Information on these jumpers can be found in Jumpers.

Warning

Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Contact our sales team if you need jumper configurations different from the default configuration.

FIGURE 4: Typical Jumper Pad Numbering Scheme

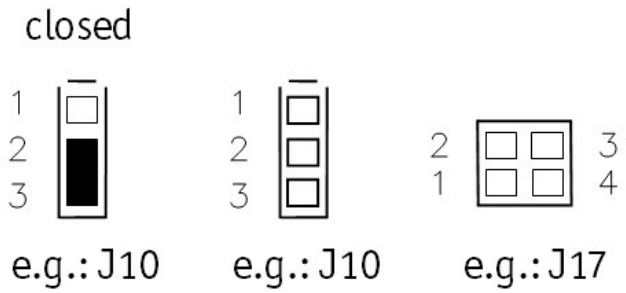
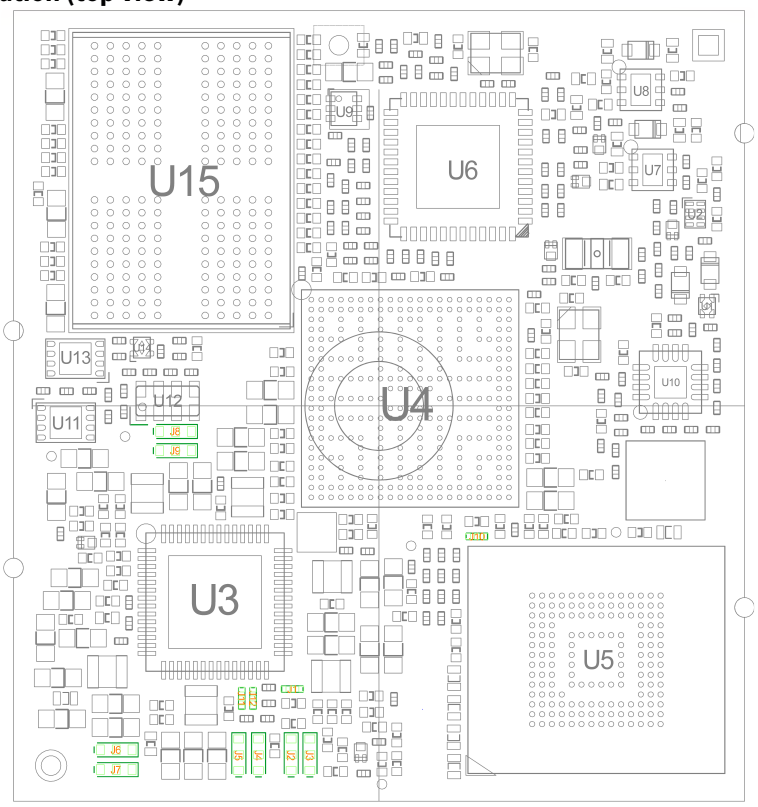


FIGURE 5: Jumper Location (top view)



Please pay special attention to the “TYPE” column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc.). The jumpers (J = solder jumper) have the following functions:

TABLE 4: Jumper Settings

Jumper	Position	Description	Type
J1		J1 selects the PMIC Mode for Buck1&2	0 Ω (0201)
	1+2	Dual Phase Mode	
	2+3	Single Phase Mode	
J2 + J3		J2 and J3 select the voltage level of the NVCC_AON	0 Ω (0402)
	1+2	NVCC_AON = 1.8 V	
	2+3	NVCC_AON = 3.3 V	
J4 + J5		J4 and J5 select the voltage level of the NVCC_WAKEUP	0 Ω (0402)
	1+2	NVCC_WAKEUP = 1.8 V	
	2+3	NVCC_WAKEUP = 3.3 V	
J6 + J7		J6 and J7 select the voltage level of the NVCC_GPIO	0 Ω (0402)
	1+2	NVCC_GPIO = 1.8 V	
	2+3	NVCC_GPIO = 3.3 V	

Jumper	Position	Description	Type
J8 + J9		J8 and J9 select the voltage level of the VDDR_IO to supply the LPDDR4 or LPDDR4X RAM device	0 Ω (0402)
	1+2	VDDR_IO = 1.1 V	
	2+3	VDDR_IO = 0.6 V	
J10		J10 Selects the signal on CPU pin Y12 depending on device type.	
	1+2	Y12 = SD1_STROBE for on Module eMMC	33 Ω (0201)
	2+3	Y12 = QSPI_DQS for NOR/NAND Flash	0 Ω (0201)
J11 + J12		J11 + J12 Selects whether I^2C3 is routed through the PMIC level shifter or connected directly to I2C3_3V3.	0 Ω (0201)
	1+2	I^2C3 = Level shifter of PMIC	
	2+3	I^2C3 = I2C3_3V3[3]	

3. Direct I2C3_3V3 option requires NVCC_GPIO to be set to 3.3 V.

7 Power

The phyFLEX-i.MX 91/93 FPSC operates off a single power supply voltage. The following section discusses the primary power pins on the phyFLEX i.MX 91/93 FPSC Connector X1 in detail.

7.1 Primary System Power (VIN_5V)

The phyFLEX-i.MX 91/93 FPSC is powered by a primary voltage supply with a nominal value of +5.0 V. On-board switching regulators generate the voltage supplies required by the i.MX 91/93 MCU and on-board components from the primary 5.0 V are supplied to the SOM.

For proper operation, the phyFLEX-i.MX 91/93 FPSC must be supplied with a voltage source of 4.75 ... 5.25 V with a maximum power consumption of a 2 A (TBD) load at the VIN_5V pins on the phyFLEX.

TABLE 5: Primary System Power

FPSC Contact	FPSC Signal	SOM Signal Name	Signal Type	Description
L24, M25, N24, L22, N22, M21, N20, P21	VCC_IN	VIN_5V	PWR_I	5 V ± 5% Power supply input of the module.
AA74, AA8, AB13, AB23, AB59, AB69, AD13, AD23, AD59, AD69, AD7, AD75, AF13, AF23, AF59, AF69, AG74, AG8, AH13, AH23, AH27, AH31, AH35, AH39, AH43, AH47, AH51, AH55, AH59, AH69, AK7, AK75, AM23, AM27, AM31, AM35, AM39, AM43, AM47, AM51, AM55, AM59, AR30, AR36, AR46, AR52, AU26, AU30, AU34, AU38, AU44, AU48, AU52, AU56, C26, C30, C34, C38, C44, C48, C52, C56, E30, E36, E46, E52, H23, H27, H31, H35, H39, H43, H47, H51, H55, H59, K7, K75, M13, M23, M27, M31, M35, M39, M43, M47, M51, M55, M59, M69, N74, N8, P13, P23, P59, P69, T13, T23, T59, T69, T7, T75, V13, V23, V59, V69, W74, W8, Y13, Y23, Y59, Y69	0V GND	GND	GND	Power and signal ground reference.

FPSC Contact	FPSC Signal	SOM Signal Name	Signal Type	Description
1, 2, 3, 4 (Corner GND)	0V GND	GND	GND	Mechanical fixing, power, and signal ground reference.

Please refer to the section Pin Description for information on additional GND Pins located at the phyFLEX i.MX 91/93 Connector X1.

For information on various power consumption scenarios that PHYTEC has run, go to phyFLEX-i.MX 91/93 FPSC Power Consumption.

Warning

As a general design rule, PHYTEC recommends connecting all GND pins to neighboring signals that are being used in the application circuitry. For maximum EMI performance, all GND pins should be connected to a solid ground plane. Additionally, take care of a solid, low impedance connection of the power supply line to avoid voltage drop. It is recommended to place a couple of bulk capacitors as near as possible to the phyFLEX's system power input (VIN_5V) to compensate for the trace inductance.

7.2 Power Management IC (PMIC) (U3)

The phyFLEX-i.MX 91/93 FPSC provides an on-board Power Management IC (PMIC) at position U3 to generate different voltages required by the microcontroller and the on-board components. The PMIC supports many different power management functionalities like dynamic voltage control, different low-power modes, and regulator supervision. It is connected to the i.MX 91/93 via the on-board I^2C bus (I^2C3). The I^2C address of the PMIC U3 is 0x25.

7.3 Power Domains

External voltages to supply the board:

- VIN_5V 5.0 V main supply voltage (4.75 .. 5.25 V / max. 4 A)
- X_RTC_VBACKUP backup supply voltage for the on-board I^2C-Bus RTC U12 (RV-3028-C7)

7.4 External Logic IO Supply Voltage

The voltage level of the phyFLEX's logic interface circuitry is VDD_1V8 (1.8 V).

The power-up and power-down sequencing is mandatory for the i.MX 91/93. External devices connected to the phyFLEX interface circuitry have to be supplied by an external power supply, which is controlled by the output signal X_nPWR_READY (OD driver) which is brought out at pin X1-U22. X_nPWR_READY should control the external supply voltage, which is used to supply the external interface circuitry connected to the phyFLEX's interfaces. X_nPWR_READY switches to GND to start the external voltage supply or to switch over a power switch. If the on-board interface voltage switches off, X_nPWR_READY is released to high impedance. To raise the signal, an external pull-up resistor (eg, 4.7 kΩ) is needed. It can be connected to voltage levels up to 10 V (used Transistor DMN1260UFA has abs. max. of 12 V), depending on the external power supply control signal requirement. Use of X_nPWR_READY ensures that external components are only supplied when the supply voltages of the i.MX 91/93 is stable and avoids undefined return currents while the system is powered down.

TABLE 6: X_nPWR_READY (OD driver)

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
Y25	Specialized	-	-	-	-	-
U22	nPWRREADY_OUT	X_nPWR_READY	-	abs. max 12 V	OD	Needs an external PU-Resistor (abs. max. 12 V). Use it to control the power sequencing of your baseboard.

Warning

PHYTEC recommends monitoring the externally generated power supply voltages using a voltage supervisor.

7.5 Backup Power (X_RTC_VBACKUP)

To back up the on-board I^2C-Bus RTC U12 (RV-3028-C7), an external voltage source must be added at Pin X1-AA22 (X_RTC_VBACKUP). The RTC has an extremely low backup current consumption of only 40 nA (@3 V).

TABLE 7: X_RTC_VBACKUP

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AA22	VCC_RTC	X_RTC_VBACKUP	-	nom. 3.3 V (max. range 1.1 V to 5.5 V)	PWR_I	Connect a gold cap or a battery here. If a battery is used, make sure that the RTC trickle charger is deactivated!

7.6 Manual Power Switch (X_ONOFF)

The signal X_ONOFF (Pin X1-R20) is used to manually switch the power of the SOM. X_ONOFF signal can be left unconnected if not used. It has a weak on-board pull-up resistor against 1.8 V (PMIC_SNVS_1V8) and is held high as long as VIN_5V is present. To drive the signal to GND, use an open collector driver or push button. For more information about ON/OFF refer to the *NXP Semiconductor i.MX 91/93 Reference Manual*.

TABLE 8: X_ONOFF

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
R20	ON/OFF	X_ONOFF (F40)	PMIC_SNVS_1V8	1.8 V	I	Wake up and power off the Processor. Intended to connect a push-button or an open-collector driver.

8 Reset

The X_nRESET_IN signal (Pin X1-Y21) on the phyFLEX-Connector is designated as a "cold reset" input. A falling edge on X_nRESET_IN (has 10 kΩ pull-up to 1.8 V supplied by PMIC_SNVS_1V8) will restart the system, performing a complete power cycle. X_nRESET_IN has a 10 ns debouncing circuit. Expanded low-level time after a recognized falling edge holds the system in the reset state. This input can be used for a mechanical reset switch button.

TABLE 9: Reset Pinout

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P15	Specialized	X_WDOG_ANY [4]	NVCC_AON	1.8 V	OD	X_WDOG_ANY is used to trigger the PMIC WDOG_B input from the i.MX 91/93 to perform a "cold reset".
Y21	nRESET_IN	X_nRESET_IN	PMIC_SNVS_1V8	1.8 V	OD	X_nRESET_IN acts as a "cold reset" input. Driving a falling edge on X_nRESET_IN to low (has a 10 kΩ pull-up to 1.8 V) will restart the system, performing a complete power cycle. X_nRESET_IN has a 10ns debouncing circuit. This input can be used for a mechanical reset switch button.
R22	nRESET_OUT	X_nRESET_OUT	PMIC_SNVS_1V8	1.8 V	OD	This pin is internally connected to the processor and the PMIC. Connect it to the reset input of your baseboard peripherals. X_nRESET_OUT has a 100 kΩ pull-up resistor to 1.8 V.

4. This pin is already assigned to other system functions, and its use as a GPIO is not recommended

9 System Boot Configuration

Most features of the i.MX 91/93 microcontrollers are configured and/or programmed during the initialization routine. Other features that impact program execution must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Boot mode selection
- Boot device selection
- Boot device configuration

The internal ROM code is the first code executed during the initialization process of the i.MX 91/93 after POR. The ROM code detects the boot mode by using the boot mode pins (BOOT_MODE[3:0]), while the boot device is selected and configured by determining the state of the eFUSEs and/or the corresponding GPIO input pins (X_BOOT_MODE[3:0]).

9.1 Boot Mode Selection

The boot mode of the i.MX 91/93 microcontroller is determined by the configuration of four boot mode inputs, BOOT_MODE[3:0], during the reset cycle of the operating system. These inputs are brought out at the phyFLEX processor pins X_BOOT_MODE[3:0] ((X1-AA7, X1-AA6, X1-AA5, X1-AA4). phyFLEX-i.MX 91/93 Boot Modes show the possible settings of pins X_BOOT_MODE[3:0] and the resulting boot configuration of the i.MX 91/93.

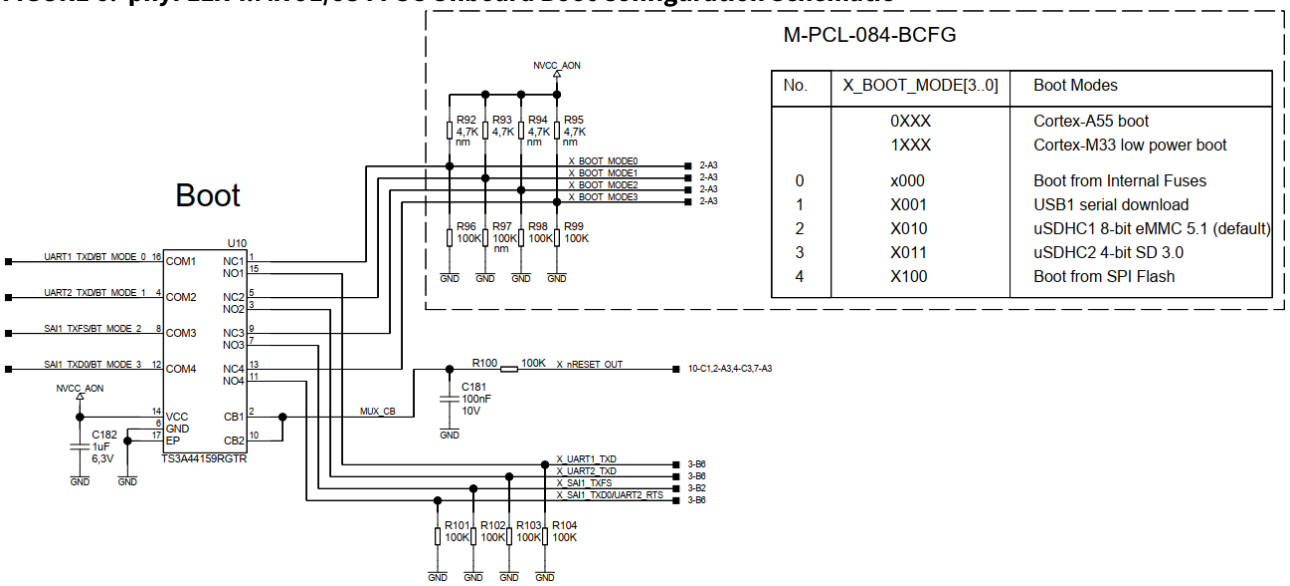
TABLE 10: phyFLEX-i.MX 91/93 FPSC Boot Modes

Boot Mode	X_BOOT_MODE3	X_BOOT_MODE2	X_BOOT_MODE1	X_BOOT_MODE0	Boot Source
	0/1				**0: A55 core (default)** 1: M33 core
0	X	0	0	0	Boot from Internal Fuses
1	0/1	0	0	1	USB1 serial download
2	**0/1**	**0**	**1**	**0**	**Boot from onboard eMMC (default)**
3	0/1	0	1	1	Boot from ext. SD-Card on SD2
4	0/1	1	0	0	Boot FlexSPI serial NOR

The X_BOOT_MODE[3,2,0] lines have 100 kΩ pull-down resistors populated (and unpopulated pull-up resistors) while X_BOOT_MODE[1] has a 4.7 kΩ pull-up resistor on the module in parallel to the internal pull-down resistors of

the i.MX 91/93. Leaving the four pins unconnected sets the controller to boot mode 2, boot from the on-board eMMC U5 memory device. The boot configuration settings can be changed by changing the populated resistors configuration on the module or by connecting configuration resistors (e.g., 4.7 kΩ pull-up) to the X_BOOT_MODE configuration signals. The pull-up resistors must be supplied by the right voltage level (default NVCC_AON=1.8 V, see section External Logic IO Supply Voltage).

FIGURE 6: phyFLEX-i.MX 91/93 FPSC Onboard Boot Configuration Schematic



The BOOT_MODE is initialized by sampling the BOOT_MODE inputs on the rising edge of the X_nRESET_OUT. After these inputs are sampled, their subsequent state does not affect the contents of the BOOT_MODE internal register. X_BOOT_MODE module input signals are connected only during the reset phase to the processor inputs. For runtime, the X_UART and X_SAI1 signals are routed through the MUX U10.

TABLE 11: phyFLEX-i.MX 91/93 FPSC Boot Configuration Pins

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P25	BOOT_MODE1	X_BOOT_MODE0 (MUX->E21)	NVCC_AON	1.8 V	I	Boot configuration pin 0 during reset has on-board 100 kΩ pull-down resistor (SMD 0201)
R24	BOOT_MODE2	X_BOOT_MODE1 (MUX->F21)	NVCC_AON	1.8 V	I	Boot configuration pin 1 during reset has on-board 4.7 kΩ pull-down resistor (SMD 0201)
T25	BOOT_MODE3	X_BOOT_MODE2 (MUX->G21)	NVCC_AON	1.8 V	I	Boot configuration pin 2 during reset has on-board 100 kΩ pull-down resistor (SMD 0201)
U24	BOOT_MODE4	X_BOOT_MODE3 (MUX->H21)	NVCC_AON	1.8 V	I	Boot configuration pin 3 during reset has on-board 100 kΩ pull-down resistor (SMD 0201)

10 System Memory

The phyFLEX-i.MX 91/93 FPSC provides four types of on-board memory:

TABLE 12: phyFLEX-i.MX 91/93 FPSC Onboard Memory Types

	Basic-Version	Kit-Version	Exclusive-Version	Maximum Available
LPDDR4(X) RAM	1 GByte	2 GByte	2 GByte	2 GByte
eMMC	8 GByte	32 GByte	128 GByte	256 GByte
I²C User EEPROM	4 kB	4 kB	4 kB	32 kB
I²C Factory EEPROM [5]	4 kB	4 kB	4 kB	32 kB

5 Factory EEPROM should not be used by the application. It contains module-specific information to identify the module during factory handling and testing.

10.1 LPDDR4(X)-RAM (U15)

The RAM interface of the phyFLEX-i.MX 91/93 FPSC supports one 16-bit LPDDR4(X)-RAM chip (U15). The memory interface supports a transfer speed of 3733 MT/s for i.MX93 and 2400 MT/s for i.MX91.

Typically, the LPDDR4(X)-RAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, the RAM must be initialized by accessing the appropriate RAM configuration registers on the i.MX 91/93 controller. Refer to the *NXP Semiconductor i.MX 91/93 Reference Manual* to access and configure these registers.

10.2 eMMC Flash Memory (U5)

The main flash memory of the i.MX 91/93 is eMMC and is populated at U5. The eMMC Flash memory is connected to the SD1 interface of the i.MX 91/93.

For more information about the eMMC Flash interface, please refer to the *NXP Semiconductor i.MX 91/93 Reference Manual*.

10.3 I²C Factory EEPROM (U11)

The phyFLEX-i.MX 91/93 FPSC is populated with a non-volatile 4 kB I²C EEPROM at U11. This memory can be used to store configuration data or other general-purpose data. This device is accessed through I²C port 3 on the i.MX 91/93 FPSC. Please see the *NXP Semiconductor i.MX 91/93 Reference Manual* for detailed information on the I²C port 3.

The three lower address bits are fixed to 0x0, which means that the EEPROM can be accessed at I^2C address 0x50. The EEPROM has a second address on 0x58, which is called the Identification Page and is reserved for internal PHYTEC use only.

The device is write-protected by default. Write protection can be deactivated by driving the signal X_EEPROM1_WC (X1-J50) to GND. The signal has a 10 kΩ pull-up resistor to NVCC_GPIO (default 1.8 V).

10.4 I^2C User EEPROM (U13)

The phyFLEX-i.MX 91/93 FPSC is populated with a non-volatile 4 kB I^2C EEPROM at U13. This memory is free for use. This device is accessed through I^2C port 3 on the i.MX 91/93. Please see the *NXP Semiconductor i.MX 91/93 Reference Manual* for detailed information on the I^2C port 3.

The three lower address bits are fixed to 0x1, which means that the EEPROM can be accessed at I^2C address 0x51. The EEPROM has a second address on 0x59, which is called the Identification Page.

The device is not write-protected by default. Write protection can be established by driving the signal X_EEPROM2_WC (X1-H49) to NVCC_GPIO (default 1.8 V). The signal has a 10 kΩ pull-down resistor.

11 Serial Interfaces

The phyFLEX-i.MX 91/93 FPSC provides numerous dedicated serial interfaces, some of which are equipped with a transceiver to enable direct connection to external devices:

1. 1x 4-bit SDIO interface (SD2) with controlled IO voltage for µSD card.
2. 1x QSPI interface or 4-bit SDIO interface (SD3)
3. 3x high-speed UARTs
4. 2x CAN-FD interfaces
5. 2x USB 2.0 Dual-Role interface with PHY
6. 2x 1 Gbit Ethernet interfaces with TSN support (ENET2 with Ethernet transceiver on the phyFLEX-i.MX 91/93 FPSC enabling a direct connection to an existing Ethernet network; ENET1 as RGMII Signals at logic-level at the signal pins instead)
7. 2x I^2C interfaces
8. 2x Serial Peripheral Interfaces (SPI)
9. 1x SAI audio interface
10. 1x LVDS display interface
11. 1x MIPI CSI-2 camera interfaces
12. 1x MIPI DSI-2 display interface

Details for each of these serial interfaces and any applicable jumper configurations are below.

11.1 SDIO Interface

The SDIO interface can be used to connect external SD cards, eMMC, or any other device requiring an SDIO interface (i.e, WiFI, I/O expansion, etc.) The phyFLEX bus features one SDIO interface on the phyFLEX-i.MX 91/93 FPSC, the interface signals extend from the second and third Ultra Secured Digital (SD2 and SD3) Host controller to the phyFLEX-Connector.

The tables below show the location of the different interface signals on the phyFLEX-Connector. The MMC/SD/SDIO Host Controller is fully compatible with the SD Memory Card Specification 3.0. The interface SD2 supports SD cards with 3.3 V and 1.8 V I/O signals.

11.2 SDIO SD2 (4-bit)

SDIO SD2 is a 4-bit wide interface with controlled I/O voltage to support high-speed modes that require 1.8 V I/O voltage. During runtime, the I/O voltage can be switched from 3.3 V (default) to 1.8 V by the processor, which controls the PMIC integrated voltage regulator. X_VDDSW_SD2 will be used exclusively to supply an external SD or MicroSD memory card. X_VDDSW_SD2 is monitored by the PMIC for overcurrent and short circuits. For more details, please refer to the PMIC data sheet provided by NXP.

TABLE 13: SDIO Interface Pinout

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
Y57	SDCARD_VCC_OUT	X_VDDSW_SD2	X_VDDSW_SD2	3.3 V	PWR_O	Controlled SD Card Supply Voltage
V57	SDCARD_nCD	X_SD2_CD_B (Y17)	NVCC_SD2	1.8 V / 3.3 V	I	SD2 Card Detect
V67	SDCARD_WP	-	-	-	-	-
W58	SDCARD_CMD	X_SD2_CMD (Y19)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Command
W60	SDCARD_CLK	X_SD2_CLK (AA19)	NVCC_SD2	1.8 V / 3.3 V	O	SD2 Clock
W62	SDCARD_DATA0	X_SD2_DATA0 (Y18)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 0
Y61	SDCARD_DATA1	X_SD2_DATA1 (AA18)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 1
U60	SDCARD_DATA2	X_SD2_DATA2 (Y20)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 2
V61	SDCARD_DATA3	X_SD2_DATA3 (AA20)	NVCC_SD2	1.8 V / 3.3 V	I/O	SD2 Data 3

11.3 Universal Asynchronous Interfaces (UARTs)

The phyFLEX-i.MX 91/93 FPSC provides three high-speed universal asynchronous interfaces. The following table shows the location of the signals on the phyFLEX-Connector.

TABLE 14: UART Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L44	UART1_RXD	X_GPIO_IO05 (L18)	NVCC_GPIO	1.8 V	I	LPUART6_RX
L42	UART1_TXD	X_GPIO_IO04 (L17)	NVCC_GPIO	1.8 V	O	LPUART6_TX
N42	UART1_RTS	X_GPIO_IO07 (L21)	NVCC_GPIO	1.8 V	O	LPUART6_RTS
M41	UART1_CTS	X_GPIO_IO06 (L20)	NVCC_GPIO	1.8 V	I	LPUART6_CTS
N46	UART2_RXD	X_UART2_RXD (F20)	NVCC_AON	1.8 V	I	LPUART2_RX (Usually used as M33 Debug)
N44	UART2_TXD	X_UART2_TXD (via boot mux to F21)	NVCC_AON	1.8 V	O	LPUART2_TX (Usually used as M33 Debug)
M45	UART2_RTS	X_SAI1_TXD0 (via boot mux to H21)	NVCC_AON	1.8 V	O	LPUART2_RTS
L46	UART2_CTS	X_SAI1_TXC (G20)	NVCC_AON	1.8 V	I	LPUART2_CTS

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AE22	UART3_RXD	X_UART1_RXD (E20)	NVCC_AON	1.8 V	I	LPUART1_RX (Usually used as A55 Debug)
AE20	UART3_TXD	X_UART1_TXD (via boot mux to E21)	NVCC_AON	1.8 V	O	LPUART1_TX (Usually used as A55 Debug)

11.4 CAN Interfaces

The CAN-FD interfaces of the phyFLEX-i.MX 91/93 FPSC is connected to the CAN modules (CAN1/CAN2) of the i.MX 91/93, which is a full implementation of the CAN FD protocol specification version 2.0B. It supports a flexible message payload, ranging from 0, 8, 12, 16, 20, 24, 32, 48, and 64 bytes. It also supports standard and extended message frames and programmable bit rates of 2, 5, and 8 Mb/s.

The following table shows the position of the signals on the phyFLEX-Connector.

TABLE 15: CAN Interface Signal Location

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
N38	CAN1_RX	X_PDM_BIT_STREAM0 (J17)	NVCC_AON	1.8 V	I	CAN1 TX
N36	CAN1_TX	X_PDM_CLK (G21)	NVCC_AON	1.8 V	O	CAN1 RX
L38	CAN2_RX	X_GPIO_IO27 (W21)	NVCC_GPIO	1.8 V	I	CAN2 TX
M37	CAN2_TX	X_GPIO_IO25 (V21)	NVCC_GPIO	1.8 V	O	CAN2 RX

11.5 USB Interfaces

The phyFLEX-i.MX 91/93 provides two USB 2.0 dual-role interfaces. USB 2.0 supports high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operation. The applicable interface signals can be found on the phyFLEX-Connector X1. If overcurrent and power enable signals are needed for the USB host interface, the functionality can be easily implemented with GPIOs.

TABLE 16: USB 1 Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AC60	USB1_VBUS	X_USB1_VBUS (via 30k resistor to F12)	VDD_3V3	3.3 V / 5 V	I	USB 1 bus voltage detection (5 V compliant)
AE60	USB1_ID	X_USB1_ID (C11)	VDD_1V8	1.8 V	I	USB 1 ID Pin
AD61	USB1_D_N	X_USB1_D_N (A14)	VDD_3V3	-	USB_I/O	USB 1 Data-
AC62	USB1_D_P	X_USB1_D_P (B14)	VDD_3V3	-	USB_I/O	USB 1 Data+
AE58	USB1_nOC	X_CCM_CLKO2 (Y3)	NVCC_WAKEUP	1.8 V	I	USB 1 over current status input
AD57	USB1_nPWR_EN	X_GPIO_IO24 (U21)	NVCC_GPIO	1.8 V	O	USB 1 power enable output

TABLE 17: USB 2 Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AA58	USB2_VBUS	X_USB2_VBUS (via 30k resistor to E14)	VDD_3V3	3.3 V / 5 V	I	USB 2 bus voltage detection (5 V compliant)
AA60	USB2_ID	X_USB2_ID (E12)	VDD_1V8	1.8 V	I	USB 2 ID Pin
AB61	USB2_D_N	X_USB2_D_N (A15)	VDD_3V3	-	USB_I/O	USB 2 Data-
AA62	USB2_D_P	X_USB2_D_P (B15)	VDD_3V3	-	USB_I/O	USB 2 Data+
AC58	USB2_nOC	X_SAI1_TXFS (via boot mux to G21)	NVCC_AON	1.8 V	I	USB 2 overcurrent status input
AB57	USB2_nPWR_EN	X_PDM_BIT_STREAM1 (G18)	NVCC_AON	1.8 V	O	USB 2 power enables output

11.6 Ethernet Interfaces ENET1 and ENET2

The phyFLEX-i.MX 91/93 FPSC provides two Ethernet Interfaces, ENET1 with TSN support and ENET2. Connection of the phyFLEX-i.MX 91/93 FPSC to the World Wide Web or a local area network (LAN) is possible using the on-board GbE PHY at U6. It is connected to the RGMII interface of ENET2. The PHY operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s. Additionally, the RGMII interface of ENET1, which is available on the phyFLEX-Connector, can be used to connect an external PHY. (ENET1 RGMII Interface).

Note

PHYTEC has chosen to make the ENET1 available as RGMII for customers to accommodate their individual needs when it comes to choosing the right PHY or switching components applicable to their network topology.
As an example, we have connected a TSN-capable Ethernet PHY to ENET1 on the carrier board, which may be used for reference in your own design. See Ethernet (X21/X22/X25) for details.

11.6.1 ENET2 Ethernet PHY (U6)

With an Ethernet PHY mounted at U6, the phyFLEX-i.MX 91/93 FPSC has been designed for use in 10Base-T, 100Base-T, and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyFLEX-Connector X1. **In a Linux environment, ENET2 interface is called eth0 as it is the port with on-board PHY.**

TABLE 18: Ethernet PHY Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AH57	GB_ETH1_A_N	X_ETH2_A_N	-	-	ETH_I/O	Gb Ethernet1 A N
AJ58	GB_ETH1_A_P	X_ETH2_A_P	-	-	ETH_I/O	Gb Ethernet1 A P
AF57	GB_ETH1_B_N	X_ETH2_B_N	-	-	ETH_I/O	Gb Ethernet1 B N
AG58	GB_ETH1_B_P	X_ETH2_B_P	-	-	ETH_I/O	Gb Ethernet1 B P
AG62	GB_ETH1_C_N	X_ETH2_C_N	-	-	ETH_I/O	Gb Ethernet1 C N
AH61	GB_ETH1_C_P	X_ETH2_C_P	-	-	ETH_I/O	Gb Ethernet1 C P
AE62	GB_ETH1_D_N	X_ETH2_D_N	-	-	ETH_I/O	Gb Ethernet1 D N
AF61	GB_ETH1_D_P	X_ETH2_D_P	-	-	ETH_I/O	Gb Ethernet1 D P
AJ68	Specialized	X_ETH2_GPIO0	NVCC_AON	1.8 V	I/O	1588 RX/TX SFD
AJ70	Specialized	X_ETH2_GPIO1	NVCC_AON	1.8 V	I/O	1588 RX/TX SFD

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ60	GB_ETH1_LED_LINK	X_ETH2_LED0_LINK	-	-	OD	Gb Ethernet1 LED Link
AG60	GB_ETH1_LED_ACT	X_ETH2_LED2_ACT	-	-	OD	Gb Ethernet1 LED Activity

11.6.1.1 Ethernet Signal Locations of ENET2

The on-board GbE PHY supports HP Auto-MDIX technology, eliminating the need for a direct-connect LAN or crossover patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an auto-negotiation to automatically determine the best speed and duplex mode.

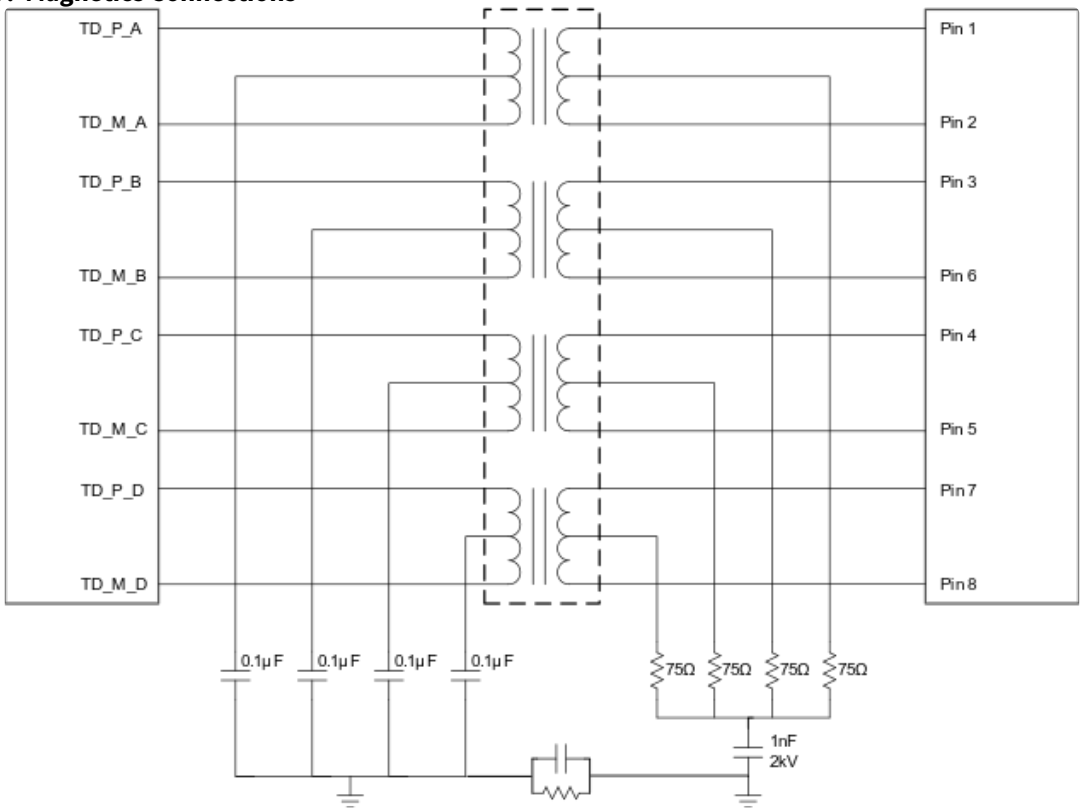
The Ethernet PHY is connected to the RGMII interface ENET2 of the i.MX 91/93. Please refer to the *NXP Semiconductor i.MX 91/93 Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network, some external circuitry is required. The required termination resistors on the analog signals (ETH_A±, ETH_B±, ETH_C±, ETH_D±) are integrated into the chip, so there is no need to connect external termination resistors to these signals. Connection to external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+/C-, and D+/D- signals should be routed as 100-ohm differential pairs. The same applies to the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Warning

Please refer to the Ethernet PHY datasheet when designing the Ethernet transformer circuitry or request the schematic of the applicable carrier board (Libra Development Board i.MX 91/93).

FIGURE 7: Magnetics Connections



11.6.2 Reset of the Ethernet Controller

The reset input of the Ethernet PHY at U6 is connected to the system reset X_nRESET_OUT.

11.6.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the internet, a table is used to convert the assigned IP address to the hardware's MAC address. In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyFLEX-i.MX 91/93 FPSC is located on the barcode sticker attached to the module. This number is a 12-digit HEX value.

11.6.4 ENET1 RGMII Interface

In order to use an external Ethernet PHY, the RGMII interface (ENET1) of the phyFLEX-i.MX 91/93 FPSC is brought out at phyFLEX-Connector X1. ENET1 supports TSN network operation. For that use case, an external TSN-ready Ethernet switch device is used. **In a Linux environment, the ENET1 interface is called eth1 as it is the port with the external PHY.**

TABLE 19: RGMII Interface Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ44	RGMII2_EVENT_OUT	X_CCM_CLKO1[4] (AA1)	NVCC_WAKEUP	1.8 V	O	TSN Event Out
AH45	RGMII2_EVENT_IN	X_ENET1_MDC (AA11)	NVCC_WAKEUP	1.8 V	I	TSN Event In
AG48	RGMII_nINT	X_ENET1_MDIO (AA10)	NVCC_WAKEUP	1.8 V	I	PHY IRQ Input
AG44	RGMII2_MDIO	X_ENET2_MDIO (AA6)	NVCC_WAKEUP	1.8 V	I/O	Management Data
AG46	RGMII2_MDC	X_ENET2_MDC (Y7)	NVCC_WAKEUP	1.8 V	O	Management Clock
AJ50	RGMII2_TX_D0	X_ENET1_TD0 (T8)	NVCC_WAKEUP	1.8 V	O	Transmit Data 0
AJ48	RGMII2_TX_D1	X_ENET1_TD1 (U8)	NVCC_WAKEUP	1.8 V	O	Transmit Data 1
AH49	RGMII2_TX_D2	X_ENET1_TD2 (V8)	NVCC_WAKEUP	1.8 V	O	Transmit Data 2

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ46	RGMII2_TX_D3	X_ENET1_TD3 (T10)	NVCC_WAKEUP	1.8 V	O	Transmit Data 3
AG50	RGMII2_TX_CTL	X_ENET1_TX_CTL (V10)	NVCC_WAKEUP	1.8 V	O	Transmit Control
AG52	RGMII2_TXC	X_ENET1_TXC (U10)	NVCC_WAKEUP	1.8 V	O	Transmit Clock
AG54	RGMII2_RX_CTL	X_ENET1_RX_CTL (Y8)	NVCC_WAKEUP	1.8 V	I	Receive Control
AG56	RGMII2_RXC	X_ENET1_RXC (AA7)	NVCC_WAKEUP	1.8 V	I	Receive Clock
AJ56	RGMII2_RX_D0	X_ENET1_RXD0 (AA8)	NVCC_WAKEUP	1.8 V	I	Receive Data 0
AJ54	RGMII2_RX_D1	X_ENET1_RXD1 (Y9)	NVCC_WAKEUP	1.8 V	I	Receive Data 1

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ52	RGMII2_RX_D2	X_ENET1_RXD2 (AA9)	NVCC_WAKEUP	1.8 V	I	Receive Data 2
AH53	RGMII2_RX_D3	X_ENET1_RXD3 (Y10)	NVCC_WAKEUP	1.8 V	I	Receive Data 3

11.7 SPI Interface

The Serial Peripheral Interface (SPI) is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyFLEX provides two SPI on the phyFLEX-Connector X1. The SPI provides one chip select signal for each interface. The Low Power SPI (LPSPI) of the i.MX 91/93 has eight separate modules (LPSPI1 to LPSPI8), which support clock rates of up to 60 MHz. The interface signals of two modules (LPSPI3, LPSPI6) are made available on the phyFLEX-Connector. These modules are master/slave configurable. The following table lists the SPI signals on the phyFLEX-Connector.

TABLE 20: SPI Interface Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L34	SPI1_nCS	X_GPIO_IO00 (J21)	NVCC_GPIO	1.8 V	O	LPSPI6 Chip Select
N32	SPI1_MOSI	X_GPIO_IO01 (K20)	NVCC_GPIO	1.8 V	O	LPSPI6 Master Out
N34	SPI1_MISO	X_GPIO_IO02 (J20)	NVCC_GPIO	1.8 V	I	LPSPI6 Master In
M33	SPI1_SCLK	X_GPIO_IO03 (K21)	NVCC_GPIO	1.8 V	O	LPSPI6 Clock
N30	SPI2_nCS	X_GPIO_IO08 (M20)	NVCC_GPIO	1.8 V	O	LPSPI3 Chip Select
L30	SPI2_MOSI	X_GPIO_IO10 (N17)	NVCC_GPIO	1.8 V	O	LPSPI3 Master Out
L32	SPI2_MISO	X_GPIO_IO09 (M21)	NVCC_GPIO	1.8 V	I	LPSPI3 Master In
M29	SPI2_SCLK	X_GPIO_IO11 (N18)	NVCC_GPIO	1.8 V	O	LPSPI3 Clock

11.8 QSPI Interface

The Quad Serial Peripheral Interface (QSPI) is a bidirectional serial bus with up to 4 data lanes that provides a simple and efficient method for data exchange among devices. The phyFLEX provides QSPI on the phyFLEX-Connector X1. The QSPI provides one chip select signal for the interface. The FlexSPI of the i.MX 91/93 supports single, dual and quad mode in single data rate (SDR) and double data rate (DDR) transfer mode. The interface signals of FlexSPI mode are made available on the phyFLEX-Connector. The following table lists the QSPI signals on the phyFLEX-Connector.

TABLE 21: QSPI Interface Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AG24	Mandatory	X_SD3_CLK (V16)	NVCC_WAKEUP	1.8 V	O	FlexSPI clock[6]
AJ24	Mandatory	X_SD3_CMD (U16)	NVCC_WAKEUP	1.8 V	O	FlexSPI chip select
AF21	Mandatory	X_SD3_DATA0 (T16)	NVCC_WAKEUP	1.8 V	I/O	FlexSPI data lane 0
AG20	Mandatory	X_SD3_DATA1 (V14)	NVCC_WAKEUP	1.8 V	I/O	FlexSPI data lane 1
AG22	Mandatory	X_SD3_DATA2 (U14)	NVCC_WAKEUP	1.8 V	I/O	FlexSPI data lane 2
AH21	Mandatory	X_SD3_DATA3 (T14)	NVCC_WAKEUP	1.8 V	I/O	FlexSPI data lane 3
AJ22	Optional	X_QSPI_DQS (via 0R J10 to SD1_STROBE Y12)	NVCC_WAKEUP	1.8 V	O	FlexSPI data strobe

4. This pin is already assigned to other system functions, and its use as a GPIO is not recommended
6. The maximum frequency supported is 52 MHz when operating in the voltage domain at 3.3 V.

11.9 I^2C / I^3C Interface

The (Improved) Inter-Integrated Circuit (I^2C / I^3C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX 91/93 contains eight identical and independent Multimaster fast-mode I^2C modules and two I^3C modules. The interface of the two modules (LPI2C1, LPI2C2) is available on the phyFLEX-Connector X1. LPI2C3 is reserved for controlling the SOM, and LPI2C1 supports the I^3C protocol.

Tip

To ensure the proper functioning of the I^2C interface, external pull resistors matching the load at the interface must be connected. There are no pull-up resistors mounted on the module. For detailed information on the voltage levels for the pull-up resistors, please refer to the *i.MX 91/93 Datasheet.*

The following table lists the I^2C / I^3C ports on the phyFLEX-Connector:

TABLE 22: I2C / I3C Interface Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L60	I2C2_SCL	X_I2C1_SCL (C20)	NVCC_AON	1.8 V	I/OD	LPI^{2}C1/I^{3}C Clock
L58	I2C2_SDA	X_I2C1_SDA (C21)	NVCC_AON	1.8 V	I/OD	LPI^{2}C1/I^{3}C Data
M61	I2C3_SCL	X_I2C2_SCL (D20)	NVCC_AON	1.8 V	I/OD	LPI^{2}C2 Clock
N60	I2C3_SDA	X_I2C2_SDA (D21)	NVCC_AON	1.8 V	I/OD	LPI^{2}C2 Data
L26	I2C1_SCL_DNU	X_GPIO_IO29 (E45)	NVCC_GPIO	1.8 V	I/OD	LPI^{2}C3 Clock used for on-board communication to PMIC. Do not connect
L28	I2C1_SDA_DNU	X_GPIO_IO28 (E43)	NVCC_GPIO	1.8 V	I/OD	LPI^{2}C3 Data used for on-board communication to PMIC. Do not connect

11.10 Audio Interface

The i.MX 91/93 supports multiple audio interfaces. One of them is available by default as listed below:

TABLE 23: phyFLEX-i.MX 91/93 FPSC Audio Interfaces

Interface	RX Data Line	TX Data Line
SAI3	1	1

11.10.1 I²S Audio Interface (SAI)

The phyFLEX-i.MX 91/93 FPSC features a Synchronous Audio Interface that supports full-duplex serial interfaces with frame synchronization, such as I2S, AC97, and TDM. The interface is divided into three sub-interfaces: SAI1, SAI2, and SAI3. SAI3 is routed directly to the phyFLEX-Connector X1 by default.

The tables below show the signal locations of the SAI3 interface.

TABLE 24: SAI Interface Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level**	Signal Type	Muxing / Description
AJ32	SAI1_MCLK	X_GPIO_IO17 (R20)	NVCC_GPIO	1.8 V	O	SAI3 MCLK
AH29	SAI1_TX_BCLK	X_GPIO_IO16 (R21)	NVCC_GPIO	1.8 V	O	SAI3 TX BCLK
AJ30	SAI1_TX_SYNC	X_GPIO_IO26 (V20)	NVCC_GPIO	1.8 V	O	SAI3 TX SYNC
AJ28	SAI1_TX_DATA	X_GPIO_IO21 (T21)	NVCC_GPIO	1.8 V	O	SAI3 TXD0
AG28	SAI1_RX_BCLK	X_GPIO_IO18 (R18)	NVCC_GPIO	1.8 V	I	SAI3 RXC
AG32	SAI1_RX_SYNC	X_GPIO_IO19 (R17)	NVCC_GPIO	1.8 V	I	SAI3 RXFS
AG30	SAI1_RX_DATA	X_GPIO_IO20 (T20)	NVCC_GPIO	1.8 V	I	SAI3 RXD0

12 General Purpose I/Os

All pins that are not used by any of the other interfaces specifically described in this manual can be used as GPIO without affecting other features of the phyFLEX-i.MX 91/93 FPSC. These pins are listed below:

TABLE 25: GPIO Pin Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
N40	GPIO1	X_GPIO_IO14 (P20)	NVCC_GPIO	1.8 V	I/O	GPIO2_IO14
L40	GPIO2	X_GPIO_IO15 (P21)	NVCC_GPIO	1.8 V	I/O	GPIO2_IO15
AL32	GPIO3	X_GPIO_IO22 (U18)	NVCC_GPIO	1.8 V	I/O	GPIO2_IO22
AL34	GPIO4	X_GPIO_IO23 (U20)	NVCC_GPIO	1.8 V	I/O	GPIO2_IO23
AN30	GPIO5	-	-	-	-	-
AN32	GPIO6	-	-	-	-	-
AN34	GPIO7	-	-	-	-	-
N48	PWM1	X_GPIO_IO12 (N20)	NVCC_GPIO	1.8 V	O	TPM3_2
N58	PWM2	X_GPIO_IO13 (N21)	NVCC_GPIO	1.8 V	O	TPM4_2

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
BD11	PWM3	-	-	-	-	-
BE17	PWM4	-	-	-	-	-

Besides these pins, most of the i.MX 91/93 signals, which are connected directly to the module connector, can be configured to act as GPIOs due to the multiplexing functionality of most controller pins.

13 Debug Interface

The phyFLEX-i.MX 91/93 FPSC is equipped with a JTAG interface to download program code into the external flash, internal controller RAM, or any debugging programs being executed. The location of the JTAG pins on the phyFLEX-Connector X1 is below:

TABLE 26: Debug Interface Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AC20	JTAG_TCK	X_JTAG_TCK (Y1)	NVCC_WAKEUP	1.8 V	I	JTAG clock signal
AC22	JTAG_TDI	X_JTAG_TDI (W1)	NVCC_WAKEUP	1.8 V	I	JTAG data in signal
AD25	JTAG_TDO	X_JTAG_TDO (Y2)	NVCC_WAKEUP	1.8 V	O	JTAG data out signal
AC24	JTAG_TMS	X_JTAG_TMS (W2)	NVCC_WAKEUP	1.8 V	I	JTAG test mode select signal
AD21	JTAG_Reserved	-	-	-	-	-

13.1 UART Debug

The default debug UART interface is FPSC UART3 (i.MX 91/93 LPUART1) for Cortex-A55 Cores and FPSC UART2 (i.MX 91/93 LPUART2) for Cortex-M33 Core. FPSC UART3 is accessible on connector X1 pins AE22 (RXD) and AE20 (TXD), and FPSC UART2 on pins N46 (RXD) and N44 (TXD).

For more information, also refer to Universal Asynchronous Interfaces (UARTs).

14 Display Interfaces

14.1 Low Voltage Differential Signal Display Interface (LVDS)

The phyFLEX-i.MX 91/93 FPSC offers one LVDS display interface. LVDS has 4 channels, supporting one display with a resolution of up to 1366 x 768 at 60 Hz or 1280 x 800 at 60 Hz.

The locations of the LVDS signals are shown below:

TABLE 27: Display Interface LVDS Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
N52	LVDS1_CLK_N	X_LVDS_CLK_N (A3)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 Clock-
N50	LVDS1_CLK_P	X_LVDS_CLK_P (B3)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 Clock+
L52	LVDS1_DATA0_N	X_LVDS_D0_N (A5)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA0-
L50	LVDS1_DATA0_P	X_LVDS_D0_P (B5)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA0+
L54	LVDS1_DATA1_N	X_LVDS_D1_N (A4)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA1-
M53	LVDS1_DATA1_P	X_LVDS_D1_P (B4)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA1+
N56	LVDS1_DATA2_N	X_LVDS_D2_N (A2)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA2-
N54	LVDS1_DATA2_P	X_LVDS_D2_P (B2)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA2+
M57	LVDS1_DATA3_N	X_LVDS_D3_N (B1)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA3-
L56	LVDS1_DATA3_P	X_LVDS_D3_P (C1)	VDD_LVDS_1P8	LVDS	LVDS_O	LVDS0 DATA3+

14.2 MIPI-DSI Display Interface (DSI)

The phyFLEX-i.MX 91/93 FPSC offers one MIPI-DSI display interface. MIPI-DSI has 4 channels, supporting one display with a resolution of up to 1920 x 1080 at 60 Hz.

The locations of the MIPI-DSI signals are shown below:

TABLE 28: Display Interface MIPI / DSI Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AN46	DSI1_CLK_N	X_MIPI_DSI1_CLK_N (D6)	VDDA_1V8	LVDS	DSI2_O	DSI Clock-
AN48	DSI1_CLK_P	X_MIPI_DSI1_CLK_P (E6)	VDDA_1V8	LVDS	DSI2_O	DSI Clock+
AL48	DSI1_D0_N	X_MIPI_DSI1_D0_N (A6)	VDDA_1V8	LVDS	DSI2_O	DSI DATA0-
AL50	DSI1_D0_P	X_MIPI_DSI1_D0_P (B6)	VDDA_1V8	LVDS	DSI2_O	DSI DATA0+
AM49	DSI1_D1_N	X_MIPI_DSI1_D1_N (A7)	VDDA_1V8	LVDS	DSI2_O	DSI DATA1-
AN50	DSI1_D1_P	X_MIPI_DSI1_D1_P (B7)	VDDA_1V8	LVDS	DSI2_O	DSI DATA1+
AN44	DSI1_D2_N	X_MIPI_DSI1_D2_N (A8)	VDDA_1V8	LVDS	DSI2_O	DSI DATA2-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AM45	DSI1_D2_P	X_MIPI_DSI1_D2_P (B8)	VDDA_1V8	LVDS	DSI2_O	DSI DATA2+
AL44	DSI1_D3_N	X_MIPI_DSI1_D3_N (A9)	VDDA_1V8	LVDS	DSI2_O	DSI DATA3-
AL46	DSI1_D3_P	X_MIPI_DSI1_D3_P (B9)	VDDA_1V8	LVDS	DSI2_O	DSI DATA3+

14.3 Parallel Display Interface

The phyFLEX-i.MX 91/93 FPSC provides the option to configure a parallel display interface. This interface is available at the phyFLEX-Connector. An LCD with up to 24-bit bus width, supporting one display with a resolution of up to 1366 x 768 at 60 Hz or 1280 x 800 60 Hz.

Warning

1. The parallel display interface is not a standard option, but it can be enabled through pin multiplexing of the SoC's available pins.
2. Only possible if no parallel camera signals are used.

Note

There is no signal length matching implemented for the display signals on the module. Trace length matching and proper routing must be performed on the carrier board to ensure reliable operation.

The following table shows the location of the parallel display signals at the phyFLEX-Connector and their signal lengths on the phyFLEX-i.MX 91/93 Modul.

TABLE 29: Parallel Display Interface Signal Locations and Lengths

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L34	SPI1_CS	X_GPIO_IO00 (J21)	25.552	NVCC_GPIO	1.8 V	O	LCD clock[5]

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
N32	SPI1_MOSI	X_GPIO_IO01 (K20)	20.174	NVCC_GPIO	1.8 V	O	LCD enable

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
N34	SPI1_MISO	X_GPIO_IO02 (J20)	20.287	NVCC_GPIO	1.8 V	O	LCDVSYNC

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
M33	SPI1_SCLK	X_GPIO_IO03 (K21)	25.004	NVCC_GPIO	1.8 V	O	LCDHSYNC

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L42	UART1_TXD	X_GPIO_IO04 (L17)	23.158	NVCC_GPIO	1.8 V	O	LCDDATA0

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L44	UART1_RXD	X_GPIO_IO05 (L18)	21.605	NVCC_GPIO	1.8 V	O	LCDDATA1

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
M41	UART1_CTS	X_GPIO_IO06 (L20)	21.401	NVCC_GPIO	1.8 V	O	LCDDATA2

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
N42	UART1_RTS	X_GPIO_IO07 (L21)	20.502	NVCC_GPIO	1.8 V	O	LCDDATA3

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
N30	SPI2_CS	X_GPIO_IO08 (M20)	20.232	NVCC_GPIO	1.8 V	O	LCDDATA4

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L32	SPI2_MISO	X_GPIO_IO09 (M21)	22.978	NVCC_GPIO	1.8 V	O	LCDDATA5

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L30	SPI2_MOSI	X_GPIO_IO10 (N17)	27.056	NVCC_GPIO	1.8 V	O	LCDDATA6

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
M29	SPI2_SCLK	X_GPIO_IO11 (N18)	22.029	NVCC_GPIO	1.8 V	O	LCDDATA7

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
CA18	PWM1	X_GPIO_IO12 (N20)	19.615	NVCC_GPIO	1.8 V	O	LCDDATA8

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
CB19	PWM2	X_GPIO_IO13 (N21)	46.032	NVCC_GPIO	1.8 V	O	LCDDATA9

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AL32	GPIO1	X_GPIO_IO14 (P20)	18.515	NVCC_GPIO	1.8 V	O	LCDDATA10

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AN30	GPIO2	X_GPIO_IO15 (P21)	22.845	NVCC_GPIO	1.8 V	O	LCDDATA11

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AH29	SAI1_TX_BCLK	X_GPIO_IO16 (R21)	13.791	NVCC_GPIO	1.8V	O	LCDDATA12

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AJ32	SAI1_MCLK	X_GPIO_IO17 (R20)	15.213	NVCC_GPIO	1.8V	O	LCDDATA13

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AG28	SAI1_RX_BCLK	X_GPIO_IO18 (R18)	19.761	NVCC_GPIO	1.8V	O	LCDDATA14

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AG32	SAI1_RX_SYNC	X_GPIO_IO19 (R17)	12.590	NVCC_GPIO	1.8V	O	LCDDATA15

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AG30	SAI1_RX_DATA	X_GPIO_IO20 (T20)	13.930	NVCC_GPIO	1.8V	O	LCDDATA16

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AJ28	SAI1_TX_DATA	X_GPIO_IO21 (T21)	14.339	NVCC_GPIO	1.8V	O	LCDDATA17

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AN32	GPIO3	X_GPIO_IO22 (U18)	13.317	NVCC_GPIO	1.8 V	O	LCDDATA18

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L40	GPIO4	X_GPIO_IO23 (U20)	10.778	NVCC_GPIO	1.8 V	O	LCDDATA19

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AD57	USB1_PWR_EN	X_GPIO_IO24 (U21)	18.937	NVCC_GPIO	1.8 V	O	LCDDATA20

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
M37	CAN2_TX	X_GPIO_IO25 (V21)	22.511	NVCC_GPIO	1.8 V	O	LCDDATA21

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
AJ30	SAI1_TX_SYNC	X_GPIO_IO26 (V20)	9.766	NVCC_GPIO	1.8V	O	LCDDATA22

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing/Description
L38	CAN2_RX	X_GPIO_IO27 (W21)	23.946	NVCC_GPIO	1.8 V	O	LCDDATA23

15 Camera Connections

15.1 MIPI-CSI Camera Interface (CSI)

The phyFLEX-i.MX 91/93 FPSC offers one MIPI-CSI interface to connect a digital camera. The MIPI-CSI-2 camera interface of the i.MX 91/93 extends to the phyFLEX-Connector X1 with 2 data lanes and one clock lane.

The locations of the MIPI-CSI signals are shown below:

TABLE 30: Camera Interface MIPI / CSI-2 Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
R62	CSI1_CLK_N	X_MIPI_CSI1_CLK_N (D10)	MIPI_CSI1_VPH	LVDS	CSI2_I	CSI1 Clock-
R60	CSI1_CLK_P	X_MIPI_CSI1_CLK_P (E10)	MIPI_CSI1_VPH	LVDS	CSI2_I	CSI1 Clock+
T57	CSI1_D0_N	X_MIPI_CSI1_D0_N (A11)	MIPI_CSI1_VPH	LVDS	CSI2_I	CSI1 DATA0-
U58	CSI1_D0_P	X_MIPI_CSI1_D0_P (B11)	MIPI_CSI1_VPH	LVDS	CSI2_I	CSI1 DATA0+
T61	CSI1_D1_N	X_MIPI_CSI1_D1_N (A10)	MIPI_CSI1_VPH	LVDS	CSI2_I	CSI1 DATA1-
U62	CSI1_D1_P	X_MIPI_CSI1_D1_P (B10)	MIPI_CSI1_VPH	LVDS	CSI2_I	CSI1 DATA1+

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
P57	CSI1_D2_N	-	-	-	-	-
R58	CSI1_D2_P	-	-	-	-	-
N62	CSI1_D3_N	-	-	-	-	-
P61	CSI1_D3_P	-	-	-	-	-

15.2 Parallel Camera Interface

The phyFLEX-i.MX 91/93 FPSC provides the option to configure a parallel camera interface. This interface is available at the phyFLEX-Connector with 10 data bits, HSYNC, VSYNC, MCLK, PIXCLK, and I²C Bus.

Warning

1. The parallel camera interface is not a standard option, but it can be enabled through pin multiplexing of the SoC's available pins.
2. Only possible if no parallel display signals are used.

Note

There is no signal length matching implemented for the camera signals on the module. Trace length matching and proper routing must be performed on the carrier board to ensure reliable operation.

The following table shows the location of the parallel camera signals at the phyFLEX-Connector and their signal lengths on the phyFLEX-i.MX 91/93 Module.

TABLE 31: Parallel Camera Interface Signal Locations and Lengths

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L34	SPI1_CS	X_GPIO_IO00 (J21)	25.552	NVCC_GPIO	1.8 V	O	CAM pixel clock[5]
N32	SPI1_MOSI	X_GPIO_IO01 (K20)	20.174	NVCC_GPIO	1.8 V	O	CAM Frame Valid
N34	SPI1_MISO	X_GPIO_IO02 (J20)	20.287	NVCC_GPIO	1.8 V	O	CAM Line Valid
M33	SPI1_SCLK	X_GPIO_IO03 (K21)	25.004	NVCC_GPIO	1.8 V	I	CAM DATA0
N42	UART1_RTS	X_GPIO_IO07 (L21)	20.502	NVCC_GPIO	1.8 V	I	CAM DATA1
N30	SPI2_CS	X_GPIO_IO08 (M20)	20.232	NVCC_GPIO	1.8 V	I	CAM DATA2
L32	SPI2_MISO	X_GPIO_IO09 (M21)	22.978	NVCC_GPIO	1.8 V	I	CAM DATA3

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Signal Length [mm]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L30	SPI2_MOSI	X_GPIO_IO10 (N17)	27.056	NVCC_GPIO	1.8 V	I	CAM DATA4
M29	SPI2_SCLK	X_GPIO_IO11 (N18)	22.029	NVCC_GPIO	1.8 V	I	CAM DATA5
AL32	GPIO1	X_GPIO_IO14 (P20)	18.515	NVCC_GPIO	1.8 V	I	CAM DATA6
AN30	GPIO2	X_GPIO_IO15 (P21)	22.845	NVCC_GPIO	1.8 V	I	CAM DATA7
AH29	SAI1_TX_BCLK	X_GPIO_IO16 (R21)	13.791	NVCC_GPIO	1.8V	I	CAM DATA8
AJ32	SAI1_MCLK	X_GPIO_IO17 (R20)	15.213	NVCC_GPIO	1.8V	I	CAM DATA9

5. Factory EEPROM should not be used by the application. It contains module-specific information to identify the module during factory handling and testing.

16 ADC Inputs

The phyFLEX i.MX 91/93 FPSC provides a 4-channel, 12-bit SAR ADC with 4 single-ended inputs.

TABLE 32: ADC Inputs Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
R16	ADC1	X_ADC_IN0 (B19)	VDDA_1V8	1.8 V	I	ADC Analog Inut 0
T15	ADC2	X_ADC_IN1 (A20)	VDDA_1V8	1.8 V	I	ADC Analog Inut 1
U16	ADC3	X_ADC_IN2 (B20)	VDDA_1V8	1.8 V	I	ADC Analog Inut 2
U14	ADC4	X_ADC_IN3 (B21)	VDDA_1V8	1.8 V	I	ADC Analog Inut 3
V15	ADC5	-	-	-	-	-
W16	ADC6	-	-	-	-	-
W14	ADC7	-	-	-	-	-
Y15	ADC8	-	-	-	-	-

17 FPSC Reserved Target-Specific Proprietary Signals

The following signals are not defined according to FPSC Gamma Feature Set Specifications (LAN-118e.A6). These signals are processor-specific and should only be used in an application if no direct compatibility between different SOMs is required.

TABLE 33: FPSC Reserved Target-Specific Proprietary Signals

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
V25	Specialized	nc	-	-	-	-
W22	Specialized	nc	-	-	-	-
W24	Specialized	nc	-	-	-	-
N28	Specialized	nc	-	-	-	-
P15	Specialized	X_WDOG_ANY[4] (J18)	NVCC_AON	1.8 V	OD	X_WDOG_ANY is connected to PMIC and is used to drive a cold reset.
Y25	Specialized	nc	-	-	-	-
AH67	Specialized	nc	-	-	-	-
AG66	Specialized	nc	-	-	-	-
AH71	Specialized	nc	-	-	-	-
AG70	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AA66	Specialized	nc	-	-	-	-
Y67	Specialized	nc	-	-	-	-
AA70	Specialized	nc	-	-	-	-
Y71	Specialized	nc	-	-	-	-
E26	Specialized	nc	-	-	-	-
E28	Specialized	nc	-	-	-	-
E32	Specialized	nc	-	-	-	-
E34	Specialized	nc	-	-	-	-
E38	Specialized	nc	-	-	-	-
E40	Specialized	nc	-	-	-	-
E42	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
E44	Specialized	nc	-	-	-	-
E48	Specialized	nc	-	-	-	-
E50	Specialized	nc	-	-	-	-
E54	Specialized	nc	-	-	-	-
E56	Specialized	nc	-	-	-	-
H75	Specialized	nc	-	-	-	-
J74	Specialized	nc	-	-	-	-
L74	Specialized	nc	-	-	-	-
M75	Specialized	nc	-	-	-	-
P75	Specialized	nc	-	-	-	-
R74	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
U74	Specialized	nc	-	-	-	-
V75	Specialized	nc	-	-	-	-
Y75	Specialized	nc	-	-	-	-
AB75	Specialized	nc	-	-	-	-
AC74	Specialized	nc	-	-	-	-
AE74	Specialized	nc	-	-	-	-
AF75	Specialized	nc	-	-	-	-
AH75	Specialized	nc	-	-	-	-
AJ74	Specialized	nc	-	-	-	-
AL74	Specialized	nc	-	-	-	-
H7	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
G20	Specialized	nc	-	-	-	-
G22	Specialized	nc	-	-	-	-
G24	Specialized	nc	-	-	-	-
G26	Specialized	nc	-	-	-	-
G28	Specialized	nc	-	-	-	-
G30	Specialized	nc	-	-	-	-
G32	Specialized	nc	-	-	-	-
G34	Specialized	nc	-	-	-	-
G36	Specialized	nc	-	-	-	-
G46	Specialized	X_TAMPER1 (F14)	VDD_1V8	1.8 V	I	TAMPER1 Input.
G48	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
G50	Specialized	nc	-	-	-	-
G52	Specialized	X_CLKIN1 (B17)	VDD_1V8	1.8 V	I	Clock Input. Has a 100 kΩ pull-down.
L70	Specialized	nc	-	-	-	-
M71	Specialized	nc	-	-	-	-
H25	Specialized	nc	-	-	-	-
H29	Specialized	nc	-	-	-	-
H33	Specialized	nc	-	-	-	-
H37	Specialized	nc	-	-	-	-
H49	Specialized	X_EEPROM2_WC	NVCC_GPIO	1.8 V	I	Write Control Input of the User EEPROM. EEPROM is write-unprotected by default. Has a 10 kΩ pull-down.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
H53	Specialized	X_CLKIN2 (A18)	VDD_1V8	1.8 V	I	Clock Input. Has a 100 kΩ pull-down.
L68	Specialized	nc	-	-	-	-
N68	Specialized	nc	-	-	-	-
R68	Specialized	nc	-	-	-	-
U68	Specialized	nc	-	-	-	-
W68	Specialized	nc	-	-	-	-
AA68	Specialized	nc	-	-	-	-
AC68	Specialized	nc	-	-	-	-
J28	Specialized	nc	-	-	-	-
J30	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J32	Specialized	nc	-	-	-	-
J34	Specialized	nc	-	-	-	-
J36	Specialized	nc	-	-	-	-
J46	Specialized	X_TAMPER0 (B16)	VDD_1V8	1.8 V	I	TAMPER0 Input. Has a 100 kΩ pull-down.
J48	Specialized	nc	-	-	-	-
J50	Specialized	X_EEPROM1_WC	NVCC_GPIO	1.8 V	I	Write Control Input of the Factory EEPROM. EEPROM is write-protected by default. Has a 10 kΩ pull-up.
J52	Specialized	X_nTEMP_ALERT	NVCC_GPIO	1.8 V	OD	ALERT wired-or outputs of the Temperature Sensors U15-U18. X_nTEMP_ALERT has a 10 kΩ pull-up to NVCC_GPIO.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J54	Specialized	X_RTC_EVI	VDD_3V3 or X_RTC_VBACKUP	3.3 V or X_RTC_VBACKUP voltage level	I	Event Input of the RTC RV-3028-C7 U12. X_RTC_EVI has a 100 kΩ pull-down and can be left unconnected. Input high level is 0.8xVDD determined by VDD_3V3 or the voltage level at X_RTC_VBACKUP in backup mode. For more information, refer to the Micro Crystal RV-3028-C7 App-Manual
M67	Specialized	nc	-	-	-	-
N66	Specialized	nc	-	-	-	-
P67	Specialized	nc	-	-	-	-
AJ42	Specialized	nc	-	-	-	-
AJ40	Specialized	nc	-	-	-	-
AJ38	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ36	Specialized	nc	-	-	-	-
AJ34	Specialized	nc	-	-	-	-
AJ26	Specialized	nc	-	-	-	-
M49	Specialized	nc	-	-	-	-
AH41	Specialized	nc	-	-	-	-
AH37	Specialized	nc	-	-	-	-
AM75	Specialized	nc	-	-	-	-
AR56	Specialized	nc	-	-	-	-
AR54	Specialized	nc	-	-	-	-
AR50	Specialized	nc	-	-	-	-
AR48	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AR44	Specialized	nc	-	-	-	-
AR42	Specialized	nc	-	-	-	-
AR40	Specialized	nc	-	-	-	-
AR38	Specialized	nc	-	-	-	-
AR34	Specialized	nc	-	-	-	-
AR32	Specialized	nc	-	-	-	-
AR28	Specialized	nc	-	-	-	-
AR26	Specialized	nc	-	-	-	-
AM7	Specialized	nc	-	-	-	-
AL8	Specialized	nc	-	-	-	-
AJ8	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AH7	Specialized	nc	-	-	-	-
AF7	Specialized	nc	-	-	-	-
AE8	Specialized	nc	-	-	-	-
AC8	Specialized	nc	-	-	-	-
AB7	Specialized	nc	-	-	-	-
Y7	Specialized	nc	-	-	-	-
V7	Specialized	nc	-	-	-	-
U8	Specialized	nc	-	-	-	-
R8	Specialized	nc	-	-	-	-
P7	Specialized	nc	-	-	-	-
M7	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
L8	Specialized	nc	-	-	-	-
J8	Specialized	nc	-	-	-	-
N70	Specialized	nc	-	-	-	-
P71	Specialized	nc	-	-	-	-
R70	Specialized	nc	-	-	-	-
AD71	Specialized	nc	-	-	-	-
AJ70	Specialized	X_ETH2_GPIO1	NVCC_WAKEUP	1.8 V	I/O	GPIO_1 (Pin 40) from the Ethernet PHY DP83867IRRGZ.
AN62	Specialized	nc	-	-	-	-
AN20	Specialized	nc	-	-	-	-
W12	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
V11	Specialized	nc	-	-	-	-
U12	Specialized	nc	-	-	-	-
T11	Specialized	nc	-	-	-	-
R12	Specialized	nc	-	-	-	-
P11	Specialized	nc	-	-	-	-
N12	Specialized	nc	-	-	-	-
M11	Specialized	nc	-	-	-	-
L12	Specialized	nc	-	-	-	-
H21	Specialized	nc	-	-	-	-
AE68	Specialized	nc	-	-	-	-
AG68	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AJ68	Specialized	X_ETH2_GPIO0	NVCC_WAKEUP	1.8 V	I/O	GPIO_0 (Pin 39) from the Ethernet PHY DP83867IRRGZ. It is used for the 4-Strap config. Do not drive this signal when the reset is active.
AM53	Specialized	nc	-	-	-	-
AM37	Specialized	nc	-	-	-	-
AM33	Specialized	nc	-	-	-	-
AM29	Specialized	VDD_0V8	VDD_0V8	0.8 V	-	Do not connect. For factory use only.
R14	Specialized	nc	-	-	-	-
N14	Specialized	nc	-	-	-	-
L14	Specialized	nc	-	-	-	-
J24	Specialized	VDD_1V1	VDD_1V1	1.1 V	-	Do not connect. For factory use only.

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J26	Specialized	nc	-	-	-	-
R66	Specialized	nc	-	-	-	-
T67	Specialized	nc	-	-	-	-
U66	Specialized	nc	-	-	-	-
W66	Specialized	nc	-	-	-	-
AD67	Specialized	nc	-	-	-	-
AL30	Specialized	VDD_SOC	VDD_SOC	0.8 V	-	Do not connect. For factory use only.
AL28	Specialized	VDDR_IO	VDDR_IO	0.6 V / 1.1 V	-	Do not connect. For factory use only.
AA16	Specialized	nc	-	-	-	-
N16	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
M15	Specialized	nc	-	-	-	-
L36	Specialized	nc	-	-	-	-
L48	Specialized	nc	-	-	-	-
AH33	Specialized	nc	-	-	-	-
AH25	Specialized	nc	-	-	-	-
AG42	Specialized	nc	-	-	-	-
AG40	Specialized	nc	-	-	-	-
AG38	Specialized	nc	-	-	-	-
AG36	Specialized	nc	-	-	-	-
AG34	Specialized	nc	-	-	-	-

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
AG26	Specialized	X_SAI1_RXD0/ IRQ_B[4] (H20)	VDD_AON	1.8 V	OD	X_SAI1_RXD0/IRQ_B is connected to support PMIC IRQ. X_SAI1_RXD0/ IRQ_B has a 100 kΩ pull-up.
AF25	Specialized	nc	-	-	-	-
W70	Specialized	nc	-	-	-	-
V71	Specialized	nc	-	-	-	-
U70	Specialized	nc	-	-	-	-
T71	Specialized	nc	-	-	-	-

4. This pin is already assigned to other system functions, and its use as a GPIO is not recommended

18 RTC

The phyFLEX i.MX 91/93 has an on-board, externally mounted RTC. The RV-3028-C7 is the newest generation of RTC from Micro Crystal with an extremely low backup current, typically 40 nA at 25 degrees. PHYTEC uses the most optimal implementation in each phyFLEX design to give the most optimal usage for all customers.

The RTC is accessible over I^2C3 on Address 0x52. In a normal operation state, the RTC power is supplied from the SOM voltage VDD_3V3. If the SOM is not powered and RTC backup is needed, the VBACKUP Pin of the RTC can be supplied over the X_RTC_VBACKUP pin X1-AC7. The RTC provides an interrupt output signal (X_RTC_INT), which is fed to the module connector X1-AC5. This signal is an open drain (OD). The on-board pull-up resistor is, by default, not mounted. To use the X_RTC_INT signal, add an external pull-up resistor (e.g., 10 kΩ) to an appropriate I/O voltage level (e.g., X_RTC_VBACKUP).

Furthermore, the RTC is able to supply a programmable clock output signal (push-pull), RTC_CLKOUT. Frequencies of 1/32/64/1024/8192 Hz and 32.768 Hz (default) are programmable. The RTC_CLKOUT signal is fed to the module connector at X1-AC6. For a detailed description of the programming capabilities of the RTC, refer to the *Micro Crystal RV-3028-C7 App-Manua*l. The RTC supports an external event input signal (X_RTC_EVI at X1-DD20), which can be used, e.g., for interrupt generation or timestamp functions. A 100 kΩ pull-down resistor is connected to this signal. For a detailed description of the programming capabilities of the RTC, refer to the *Micro Crystal RV-3028-C7 App-Manua*l.

TABLE 34: RTC Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball)	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
U20	RTC_CLKOUT	X_RTC_CLKOUT	VDD_1V8	1.8 V	O	RTC 32 kHz clock
T21	RTC_nINT	X_RTC_INT	-	-	OD	RTC IRQ output. Needs an external pull-up resistor.
AA22	VCC_RTC	X_RTC_VBACKUP	-	3.3 V (1.1 V to 5.5V)	PWR_I	3.3 V backup voltage input. If not needed, pull with 10 kΩ to GND
J54	Specialized	X_RTC_EVI	VDD_3V3 or X_RTC_VBACKUP	3.3 V or X_RTC_VBACKUP voltage level	I	Event Input of the RTC RV-3028-C7 U12. X_RTC_EVI has a 100 kΩ pull-down and can be left unconnected. Input high level is 0.8 x VDD determined by VDD_3V3 or the voltage level at X_RTC_VBACKUP in backup mode. For more information, refer to the Micro Crystal RV-3028-C7 App-Manual

19 Temperature Sensor

The phyFLEX-i.MX 91/93 FPSC supports two internally sensored thermal zones in the i.MX 91/93 CPU as well as one externally sensored thermal zone for monitoring board-level temperature. The presence of the sensor depends on the delivery variant of the module.

TABLE 35: Temperature Sensors Signal Locations

SOM Connector Pin / Libra Development Board Carrier Board Connector Pin	FPSC Signal Mandatory Optional Specialized	SOM Signal Name (CPU Ball]	SOM Voltage Domain	Signal Level	Signal Type	Muxing / Description
J52	Specialized	X_nTEMP_ALERT	NVCC_GPIO	1.8 V	OD	ALERT wired-or outputs of the Temperature Sensors U15-U18. X_nTEMP_ALERT has a 10 kΩ pull-up to NVCC_GPIO.

The external temperature sensors are located at the following positions.

Temperature Sensor Locations

The TMP102 temperature sensor devices used are connected to the I^2C3 bus. TMP102 measures temperatures from -40 °C to +125 °C. For a more detailed description of TMP102, refer to the Texas Instruments *TMP102 Datasheet*.

TABLE 36: I2C3 Temperature Sensor Slave Addresses

Sensor	I^2C slave address
U9	0x48

20 CPU Core Frequency Scaling

The phyFLEX-i.MX 91/93 FPSC is able to scale the clock frequency and voltage. This is used to save power and reduce heat dissipation when the full performance of the CPU is not needed. Scaling the frequency and voltage is referred to as 'Dynamic Voltage and Frequency Scaling' (DVFS). The phyFLEX-i.MX 91/93 FPSC BSP supports the DVFS feature. The *Linux* kernel provides a DVFS framework that allows each CPU core to have a min/max frequency as well as the applicable voltage and a governor that governs these values depending on the system load. Depending on the i.MX 91/93 variant used; several different frequencies are supported. Further details on how to configure this governor can be found in the phyFLEX-i.MX 91/93 BSP Manual.

21 Technical Specifications

Warning

Due to changes in functionality and design that are currently being developed, there are several values that cannot be determined in time for the release of this manual. All values with "TBD (To Be Determined)" are currently being evaluated. These values will be added to future manual editions.

The module's profile is max. 5 mm thick, with a maximum component height of 1 mm on the bottom side of the PCB and approximately 1.2 mm on the top side (microcontroller). The board itself is approximately 2 mm thick. The phyFLEX-i.MX 91/93 FPSC Footprint can be seen below.

phyFLEX-i.MX 91/93 FPSC Footprint (top to bottom view; unit in mm)

phyFLEX-i.MX 91/93 FPSC Footprint (bottom view top down; unit is mm)

Tip

For a downloadable version of the phyFLEX-i.MX 91/93 FPSC footprint, go to the download section of our product website: phyFLEX-i.MX 91/93 FPSC Download Page.

Additional specifications:

TABLE 37: Technical Specifications

Dimensions:	(40 x 37) mm
Weight:	ca. 17 g
Storage Temperature:	-40 to +85 °C
Operating Temperature:	i.MX 91/93 Product Temperature Grades
Humidity:	10 % - 90 % (non-condensing)
Operating Voltage:	4.75 V .. 5.25 V
Power Consumption:	phyFLEX-i.MX 91/93 FPSC Power Consumption

These specifications describe the standard configuration of the phyFLEX-i.MX 91/93 FPSC as of the printing of this manual.

21.1 phyFLEX-i.MX 91/93 FPSC Power Consumption

The values listed in the table below are guidelines to determine the required dimensions of the power supply circuitry on a carrier board. They do not take application-specific load situations into account. These values have been generated by looking at the maximum power consumption measured using different load scenarios and

adding a voltage source of 5.0 V. These values are based on internal PHYTEC testing. Customers need to consider their application power requirements to ensure they do not generate a load greater than the values listed here.

TABLE 38: phyFLEX-i.MX 91/93 FPSC Power Consumption

Required Supply Voltage	5.0 V
Ramp-Up Time (10 %-90 %)	100 µs to 10 ms
Allowed Tolerance of Supply Voltage	4.75 V .. 5.25 V (Abs. max 5.5 V)
Max. current consumption	2 A

For power measurement, a SOM (PFL-G-05) with 2 GB RAM, 32GB eMMC, ETH0, and a PIMX9596AVZXNAB was used together with PDx.x.x.

Warning

These tests are currently ongoing. Due to this, the table below has been intentionally left blank. These values will be available in future versions of this manual.

TABLE 39: phyFLEX-i.MX 91/93 FPSC Power Consumption Test Scenarios

	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
eMMC-Boot system idle DVFS ondemand	TBD	TBD	TBD	TBD	TBD	TBD
iperf3 client eth0 (~900MBit/s)	TBD	TBD	TBD	TBD	TBD	TBD
CPU-Load (4x dd from /dev/urandom to /dev/null)	TBD	TBD	TBD	TBD	TBD	TBD
RAM-Load (memtester)	TBD	TBD	TBD	TBD	TBD	TBD
GPU-Load (qt5-opengles2-test)	TBD	TBD	TBD	TBD	TBD	TBD
VPU-Load (video 1080p)	TBD	TBD	TBD	TBD	TBD	TBD
Power Consumption [Watt]	TBD	TBD	TBD	TBD	TBD	TBD
CPU Thermal Zone 0 [°C]	TBD	TBD	TBD	TBD	TBD	TBD
CPU Thermal Zone 1 [°C]	TBD	TBD	TBD	TBD	TBD	TBD
CPU Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
RAM Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
Eth-PHY Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
PMIC Surface Temperature [°C]	TBD	TBD	TBD	TBD	TBD	TBD
Ambient [°C]	TBD	TBD	TBD	TBD	TBD	TBD

Additionally, there are some values that cannot be tested. Situations such as suspending to RAM, suspend freeze, and standby mode must be tested on a case-by-case basis to ensure the application's power consumption stays within the guidelines stated above.

Tip

For further information and assistance regarding your application's power consumption, please contact PHYTEC sales.

21.2 Product Temperature Grades

Warning

The right temperature grade for the module greatly depends on the use case. It is necessary to determine if the use case suits the temperature range of the chosen module (see below). A heat spreader can be used if temperature compensation is required.

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high-performance microcontrollers and other active parts, such as the ones described within this manual, are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about minimum or maximum ambient temperature ratings for the described SOM is not possible. However, the above-mentioned parts are available at different temperature qualification levels by the producers. We offer our SOMs in different configurations, making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration, we have categorized our SOMs into three temperature grades.

The table below describes these grades in detail. This table describes a set of components that, in combination, add up to a useful set of product options with different temperature grades. This enables us to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the minimum or maximum qualification levels are met within an application, the following conditions must be defined by considering the use case:

- Determined the processing load for the given software use case
- Maximum temperature ranges of components (table below)
- Power consumption resulting from a baseload and the calculating power required (in consideration of peak loads as well as time periods for system cooldown)
- Surrounding temperatures and existing airflow in case the system is mounted into a housing
- Heat resistance of the heat dissipation paths within the system along with the considered usage of a heat spreader or a heat sink to optimize heat dissipation

TABLE 40: Product Temperature Grades

Product Temperature Grade	Controller Range (Junction Temperature)	RAM (Case Temperature)	Other (Ambient)
I	Industrial: -40 °C to +105 °C	Industrial: -40 °C to +95 °C	Industrial: -40 °C to +85 °C
C	Commercial: 0 °C to +95 °C	Consumer: 0 °C to +95 °C	Consumer: 0 °C to +70 °C

22 FPSC Footprint on the phyFLEX-i.MX 91/93 FPSC

For information on the footprint, mating baseboard footprint, numbering schema, etc., please refer to the corresponding FPSC Gamma Feature Set Specifications (LAN-118e.A6).

Pin numbering schema:

FPSC Gamma Feature Set Specifications (LAN-118e.A6) - Pin Numbering

Mating FPSC Baseboard Footprint;

FPSC Gamma Feature Set Specifications (LAN-118e.A6) - Baseboard

23 Interface Signal Trace Length

PHYTEC recommends a control delay and trace length for the high-speed interface signals. Signal delay and trace length of the high-speed interface signals routed on the front of the phyFLEX-i.MX 91/93 FPSC are listed in the following table. Take these values into consideration for the calculation of the overall delay and trace length budgets.

TABLE 41: Interface Signal Trace Length

Signal	Delay [ps]	Length [mm]	Signal	Delay [ps]	Length [mm]
MIPI DSI			LVDS		
X_MIPI_DSI1_CLK_N	170	25,97	X_LVDS_CLK_N	86	15,14
X_MIPI_DSI1_CLK_P	170	25,99	X_LVDS_CLK_P	86	15,13
X_MIPI_DSI1_D0_N	168	25,75	X_LVDS_D0_N	94	15,11
X_MIPI_DSI1_D0_P	168	25,72	X_LVDS_D0_P	94	15,13
X_MIPI_DSI1_D1_N	169	25,78	X_LVDS_D1_N	94	15,25
X_MIPI_DSI1_D1_P	169	25,83	X_LVDS_D1_P	94	15,20
X_MIPI_DSI1_D2_N	168	25,71	X_LVDS_D2_N	87	15,17
X_MIPI_DSI1_D2_P	168	25,71	X_LVDS_D2_P	87	15,19
X_MIPI_DSI1_D3_N	169	25,79	X_LVDS_D3_N	94	15,20
X_MIPI_DSI1_D3_P	169	25,77	X_LVDS_D3_P	94	15,21
MIPI CSI			SD2		

X_MIPI_CSI1_CLK_N	129	20,09	X_SD2_CLK	175	28,94
X_MIPI_CSI1_CLK_P	129	20,11	X_SD2_CMD	168	28,12
X_MIPI_CSI1_D0_N	125	19,85	X_SD2_DATA0	169	28,19
X_MIPI_CSI1_D0_P	127	19,86	X_SD2_DATA1	170	28,16
X_MIPI_CSI1_D1_N	126	19,88	X_SD2_DATA2	172	28,35
X_MIPI_CSI1_D1_P	127	19,88	X_SD2_DATA3	170	28,10
ETH2			SD3		
X_ETH2_A_N	39	7,29	X_SD3_CMD	133	21,09
X_ETH2_A_P	40	7,35	X_SD3_CLK	140	21,77
X_ETH2_B_N	13	3,57	X_SD3_DATA0	134	21,16
X_ETH2_B_P	12	3,48	X_SD3_DATA1	136	21,12
X_ETH2_C_N	22	4,94	X_SD3_DATA2	134	21,09
X_ETH2_C_P	22	4,83	X_SD3_DATA3	136	21,28

X_ETH2_D_N	17	4,17	X_QSPI_DQS	134	22,11
X_ETH2_D_P	16	4,12	-	-	-
ETH1			SD1		
X_ENET_RGMII_RD0	19	31,53	SD1_CLK	169	25,60
X_ENET_RGMII_RD1	19	31,27	SD1_CMD	158	24,93
X_ENET_RGMII_RD2	188	31,24	SD1_DATA0	160	24,95
X_ENET_RGMII_RD3	19	30,60	SD1_DATA1	158	24,13
X_ENET_RGMII_RX_CTL	19	30,86	SD1_DATA2	160	25,00
X_ENET_RGMII_RXC	195	31,91	SD1_DATA3	163	23,67
X_ENET_RGMII_TD0	131	28,75	SD1_DATA4	164	23,76
X_ENET_RGMII_TD1	127	28,22	SD1_DATA5	164	23,78
X_ENET_RGMII_TD2	117	28,05	SD1_DATA6	165	23,98
X_ENET_RGMII_TD3	125	28,28	SD1_DATA7	164	23,77

X_ENET_RGMII_TX_CTL	121	30,25	SD1_STROBE	155	23,01
X_ENET_RGMII_TXC	130	31,20	-	-	-
USB1			USB2		
X_USB1_D_N	74	12,31	X_USB2_D_N	89	14,56
X_USB1_D_P	73	12,19	X_USB2_D_P	90	14,64

24 Hints for Integrating and Handling the phyFLEX-i.MX 91/93 FPSC

24.1 Integrating the phyFLEX-i.MX 91/93 FPSC

Besides this hardware manual, more information is available to facilitate the integration of the phyFLEX-i.MX 91/93 FPSC into customer applications.

1. The design of the Libra Development Board can be used as a reference for any customer application.
2. Many answers to common questions can be found at: https://www.phytec.de/produkte/system-on-modules/phyflex-imx-91/93-fpsc/#downloads/
3. The link “Carrier Board” within the category Dimensional Drawing leads to the layout data phyFLEX-i.MX 91/93 FPSC Footprint. It is available in different file formats. The use of this data allows the user to integrate the phyFLEX-i.MX 91/93 FPSC SOM as a single component into their design.
4. Different support packages are available for support in all stages of embedded development. Please visit https://www.phytec.de/support/support-pakete/ or https://www.phytec.eu/support/support-packages/ or contact our sales team for more details.

24.2 Handling the phyFLEX-i.MX 91/93 FPSC

24.2.1 phyFLEX Module Modifications

The removal of various components, such as the microcontroller or the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered components need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, hot air rework station, or other desoldering method is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

Warning

If any modifications to the module are performed, regardless of their nature, the manufacturer's guarantee may be null and void.

24.2.2 Integrating the phyFLEX into a Target Application

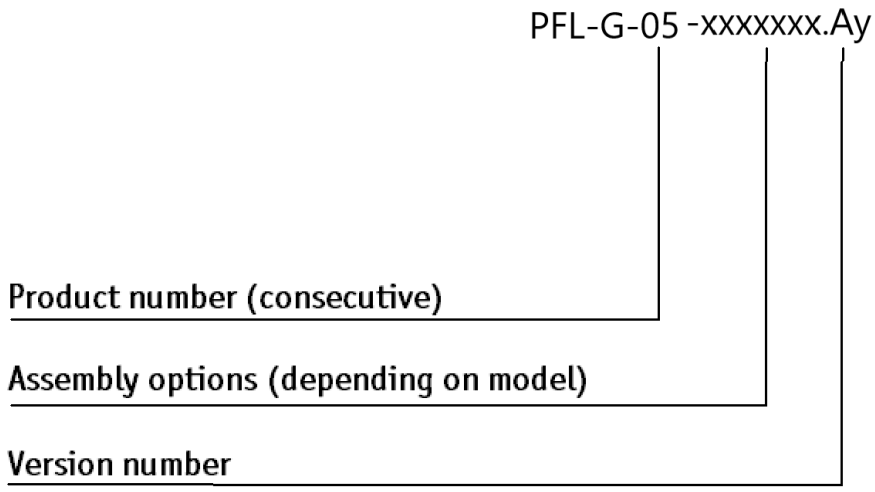
Successful integration in the user target circuitry greatly depends on adherence to the layout design rules for the GND connections of the phyFLEX module. For maximum EMI performance, PHYTEC recommends, as a general design rule, connecting all GND pins to a solid ground plane. At a minimum, all GND pin neighboring signals that are being used in the application circuitry should be connected to GND.

Tip

Specific details may need to be considered when designing a customer-specific carrier board. For design information on carrier board components, please check the ***Design Considerations*** in each component section of phyFLEX-i.MX 91/93 FPSC on the Libra Development Board. Be aware that not all components need to be considered when designing your own carrier board.

24.3 Ordering Information

The part numbering of the phyFLEX PFL-G-05 has the following structure:



The part numbering for the DSC module of the phyFLEX PFL-G-05 follows the same numbering schema.

24.4 Product Specific Information and Technical Support

In order to receive product-specific information on all future changes and updates, we recommend registering at: http://www.phytec.de/support/registrierung.html or http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our website, which provides product-specific information, such as errata sheets, application notes, FAQs, etc.
https://www.phytec.de/produkte/system-on-modules/phyflex-imx-91-93/
or
https://www.phytec.de/produkte/system-on-modules/phyflex-imx-91-93/

Note

Assembly Options include a choice of Controller, RAM (Size/Type), interfaces available, vanishing, temperature range, and other features. Please contact our sales team to get more information on the ordering options available.

25 phyFLEX-i.MX 91/93 FPSC on the Libra Development Board

25.1 Hardware Overview

The Libra Development Board for phyFLEX-i.MX 91/93 FPSC is a low-cost, feature-rich software development platform supporting the NXP Semiconductors i.MX 91/93 microcontroller. Due to numerous standard interfaces, the Libra Development Board i.MX 91/93 can serve as the bedrock for any application. At the core of the Libra Development Board is the PFL-G-05 phyFLEX-i.MX 91/93 FPSC System On Module (SOM) containing the processor, LPDDR4(X) RAM, eMMC Flash, power regulation, supervision, transceivers, and other core functions required to support the i.MX 91/93 processor. Surrounding the SOM is the PBA-BG-41/Libra Development Board carrier board, adding power input, buttons, connectors, signal breakout, and Ethernet connectivity, along with other peripherals.

25.2 Libra Development Board Concept

PHYTEC phyFLEX carrier boards are fully equipped with all the mechanical and electrical components necessary for a fast, secure start-up. Subsequent communication to and programming of applicable PHYTEC System on Modules (SOM) is made easy. phyFLEX carrier boards are designed for evaluation, testing, and prototyping of PHYTEC System on Modules in laboratory environments prior to their use in customer-designed applications.

This modular development platform concept includes the following components:

- The **phyFLEX-i.MX 91/93 FPSC Module** populated with the i.MX 91/93 microcontroller and all applicable SOM circuitry such as LPDDR4(X) SDRAM, eMMC-Flash, Ethernet-PHY, PMIC, etc.
- The **Libra Development Board Carrier Board** offers all essential components and connectors for a start-up, including a power supply for 24 V input voltage and interface connectors such as **SD-Card**, **USB,** and **Ethernet**, which enable the use of the SOM's interfaces with a standard cable.

The carrier board can also serve as a reference design for developing custom target hardware in which the phyFLEX SOM can be deployed. Carrier board schematics are available under a Non-Disclosure Agreement (NDA). The reuse of carrier board circuitry enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

SBCplus Concept

The SBCplus concept was developed to meet the many small differences in customer requirements with little development effort. This greatly reduces the time-to-market. The core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a large number of function blocks (so-called "building blocks") that are continuously being refined and updated.

Recombining these function blocks allows PHYTEC to develop a customer-specific SBC within a short time. We are able to deliver production-ready custom single-board computers within a few weeks at very low costs. The already developed SBCs, such as the Libra Development Board, each represent a combination of different customer wishes. This means all necessary interfaces are already available on the standard versions, allowing PHYTEC SBCs to be integrated into a large number of applications without modification.

For any necessary detail adjustment, extension connectors are available which enable a wide variety of functions to be added.

25.3 Libra Development Board Features

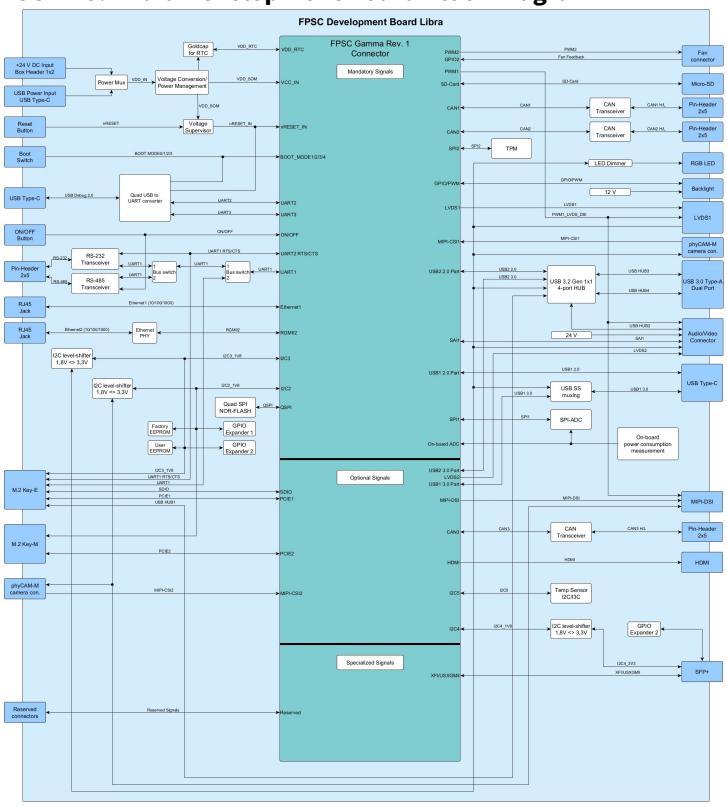
supports the following features:
[1]

- Developed under PHYTEC's FPSC concept
- Implements FPSC Featureset Gamma Rev. 1
- Populated with PHYTEC's phyFLEX FPSC SoM (see phyFLEX SoM Feature List)
- Dimensions of 200 mm × 130 mm
- Boot from eMMC, SD Card, or over USB with the Serial Downloader
- 24 V input voltage
- USB-C input power
- 64 MByte QSPI-NOR
- 2 kBit EEPROM
- 2x RJ45 jack for 10/100/1000 Mbps Ethernet
- 1x SFP+ receptacle for 10/100/1000/2500/5000/10000 Mbps Ethernet
- 1x Dual USB 3.0 Type-A connector (Actual USB speed depends on mounted SoM)
- 1x USB-C 3.2 interface connected to phyFLEX FPSC SoM (Actual USB speed depends on mounted SoM)
- 1x Secure Digital / MultiMedia Memory Card interface brought out to a Micro SD-Card receptacle
- 1x HDMI interface brought out to a standard Type-A connector (HDMI availability depends on mounted SoM)
- 1x MIPI-DSI brought out to be used with PEB-AV-12 (MIPI-DSI availability depends on the mounted SoM)
- 2x MIPI-CSI-2 camera interfaces brought out as a phyCAM-M interface (MIPI-DSI availability depends on mounted SoM)
- 1x M.2 Key-E connector with (Key-E interface availability depends on the mounted SoM):
    - 1x PCIe
    - 1x SDIO
    - 1x UART with flow-control
    - 1x I2C
    - 1x USB 2.0 (no protective circuitry on carrier board)
- 1x M.2 Key-M connector with (Key-M interface availability depends on the mounted SoM):
    - 1x PCIe
    - 1x I2C
- RS-232 or RS-485 available at 2x5 pin header 2.54 mm RS-232 (up to Mbps) including a handshake and RS-485 Half-Duplex (up to Mbps)
- Up to 8 ADC input pins (Number of useable ADC input signals depends on the mounted SoM)
- 8-Bit SPI-ADC
- Reset button
- ON/OFF button
- 1x multicolor LED
- 1x PHYTEC Audio/Video connector for PEB-AV-10/13 with:
    - 1x LVDS (LVDS interface availability depends on the mounted SoM)
    - 1x Synchronous Audio Interface
    - 1x USB 2.0 (no protective circuitry on carrier board)
- SAI Audio brought out via an A/V connector
- 1x JTAG at 2x10 pin socket 2.54 mm
- Goldcap backup supply for SoM RTC
- On-board measurement of SoM Power Consumption
- I2C/I3C Temperature Sensor (Temperature Sensor availability depends on I2C capabilities of mounted SoM)
- Trusted Platform Module (TPM)

1. PCM-937-L

25.4 Block Diagram

FIGURE 8: Libra Development Board Block Diagram



25.5 SoM Feature List on the Libra Development Board

There are several SoMs that can be used with the Libra Development Board. Below is a comprehensive list of features that each SoM contains and can be used with the Libra Development Board. For more information, please contact your PHYTEC representative (Contact Information).

TABLE 42: FPSC Gamma Feature Set Signals

		phyFLEX-i.MX 95	phyFLEX-i.MX 8M Plus	phyFLEX-STM32MP2	phyFLEX-AM62Lx	phyFLEX-i.MX 93	phyFLEX-i.MX 91
	Featureset	**Gamma**	**Gamma**	**Gamma**	**Gamma**	**Gamma**	**Gamma**
	Subclass	**1 / 2 / 3**	**1 / 2 / 3**	**1 / 2 / 3**	**2 / 3**	**1 / 2 / 3**	**3**
Mandatory Signals	RGMII	x	x	x	x	x	x
	Ethernet	x	x	x	x	x	x
	USB 2.x	x	x	x	x	x	x
	USB 2.x	x	x	x	x	x	x
	LVDS	x	x	x	x	x	NA
	MIPI-CSI-2 (2 or 4 lanes)	x	x	x	NA	x	NA
	SD Card	x	x	x	x	x	x
	QSPI	x	x	x	x	x	x
	CAN(-FD) (2)	x	x	x	x	x	x
	UART+Flow (2)	x	x	x	x	x	x
	UART	x	x	x	x	x	x
	SPI+CS (2)	x	x	x	x	x	x
	I2C (2)	x	x	x	x	x	x

	PWM (2)	x	x	x	x	x	x
	SAI 2-Lane	x	x	x	x	x	x
	JTAG	x	x	x	x	x	x
	PWR_IN	x	x	x	x	x	x
	Control/ Misc	x	x	x	x	x	x
	GPIO (4)	x	x	x	x	x	x
Optional Signals	USB 3.x (1-2)	1	2	1	0	0	0
	LVDS	1	1	1	0	0	0
	MIPI-DSI	1	1	1	1	1	0
	MIPI-CSI (2 or 4 lanes)	1	1	0	0	0	0
	HDMI/eARC	0	1	0	0	0	0
	PCIe 2-Lane (1-2)	2	1	1	0	0	0
	CAN(-FD)	0	0	0	1	0	0
	SDIO4	1	1	1	1	0	0
	SPI+CS	1	1	1	1	0	0
	I2C (1-2)	1	1	2	1	0	0
	PWM (1-2)	2	2	2	2	0	0
	ADC (1-8)	8	0	4 (5)	4	4	4
	GPIO (1-3)	3	3	3	3	0	0

Specialized Signals	10G Ethernet	1	0	0	0	0	0
	USB 3 SS Signals	1	0	1 (or PCIe)	0	0	0
	GPIO	1	4	4	4	0	0

25.6 Temperature Range

Most components on the Libra Development Board have an operating temperature range of -40 °C to 85 °C. The following components are the exception:

TABLE 43: Libra Development Board Component Temperature Range

BOM No.	Component Description	Temperature Range	Advice
C111	Double-layer capacitor for RTC Backup	-25 °C to 70 °C	
X37	HDMI Connector	-25 °C to 85 °C	There is no replacement available
X43	LVDS1 Data Connector	-35 °C to 85 °C	There is no replacement available
X44	LVDS1 Backlight Connector	-25 °C to 85 °C	There is no replacement available
X68	Fan Connector	-35 °C to 85 °C	
X60	Micro SD-Card Slot	-25 °C to 85 °C	The SD-Card slot can be used in the range of -40 °C to 85 °C without mechanical changes

For this reason, the operation temperature range for the kit variant is: -25 °C to 70 °C. The storage temperature range is -40 °C to 85 °C.

25.7 Mechanical Dimensions

For detailed dimensions, refer to the provided CAD data (e.g., DXF file) in the download section of our specific FPSC SoMs:

- phyFLEX-i.MX 95 FPSC
- phyFLEX-i.MX 8M Plus FPSC
- phyFLEX-STM32MP2x FPSC
- phyFLEX-AM62Lx FPSC
- phyFLEX-AM62P FPSC (COMING SOON)

26 Libra Development Board Components

Tip

For high-resolution pictures of the Libra Development Board, please go to the download section of our specific FPSC SoMs.

Note

For easy reference, Pin 1 for each component has been highlighted.

26.1 Libra Development Board Component Placement Diagram

FIGURE 9: Libra Development Board Components (Top)

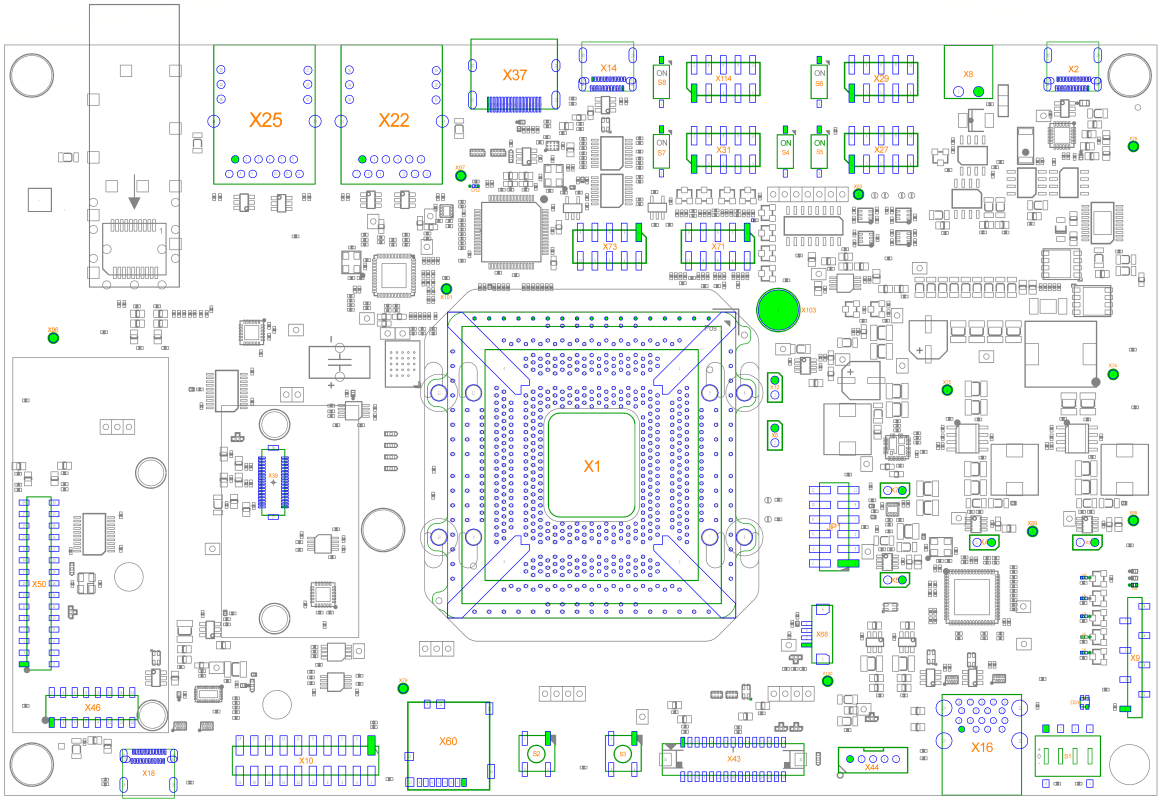
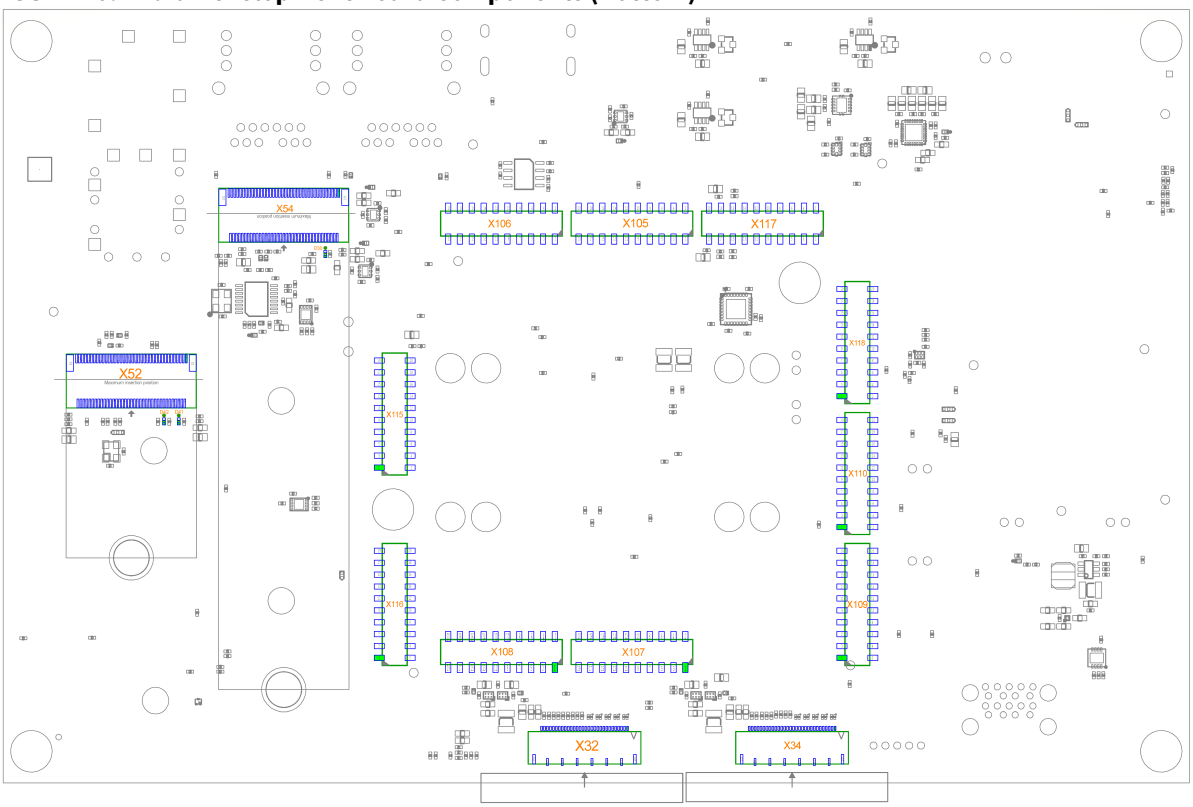


FIGURE 10: Libra Development Board Components (Bottom)



26.2 Libra Development Board Component Overview

The Libra Development Board features many interfaces and is equipped with the components listed in the table Connectors and Pin Header. For a more detailed description of each component, refer to the appropriate section listed in the table below. Libra Development Board Components (Top) and Libra Development Board Components (Bottom) highlight the location of each component for easy identification.

26.2.1 Connectors and Pin Header

The table below lists all available connectors on the Libra Development Board.

TABLE 44: Libra Development Board Connectors and Pin Headers

Reference Designator	Description	Section
X1	SoM FPSC solder connection	phyFLEX Connector (X1)
X2	Carrier board power in USB-C	Power Supply (X2/X8)
X3	VDD_5V0 current amp header 2,54 mm (not mounted)	

Reference Designator	Description	Section
X4	VDD_3V3 current amp header 2,54 mm(not mounted)	
X5	VDD_1V8 current amp header 2,54 mm(not mounted)	
X6	SoM 3,3 V output header 2,54 mm(not mounted)	
X7	SoM 1,8 V output header 2,54 mm (not mounted)	
X8	Carrier board power in a 2-pin connector	Power Supply (X2/X8)
X9	Boot Mode manipulation header	Boot Header (X9)
X10	JTAG header 2,54 mm voltage level 1,8 V	JTAG (X10)
X12	SoM input current amp header 2,54 mm(not mounted)	SoM Input Current Amp Header (X12)
X14	USB-C-Debug	USB Debug (X14)
X16	Dual USB-A 3.0	USB Type-A 3.0 Interface (X16)
X18	Dual-role USB-C 3.2	USB-C 3.2 GEN 1 Interface (X18)
X22	Ethernet Gigabit RJ-45	Ethernet (X22/X25)
X25	Ethernet Gigabit RJ-45	
X27	RS232/RS485 10-pin header 2,54 mm	RS-232/RS-485 (X27)
X29	CAN-FD1 10-pin header 2,54 mm	CAN FD (X29/X31/X114)
X31	CAN-FD2 10-pin header 2,54 mm	

Reference Designator	Description	Section
X114	CAN-FD3 10-pin header 2,54 mm	
X32	phyCAM-M CSI1	phyCAM-M MIPI CSI Camera Connectors (X32/34)
X34	phyCAM-M CSI2	
X37	HDMI	HDMI (X37)
X39	MIPI-DSI 36-pin board-to-board	MIPI-DSI (X39)
X43	LVDS1 data connector	LVDS1 (X43/X44)
X44	LVDS1 backlight connector	
X46	LVDS2 AV-Connector display data 16-pin header 2 mm	Audio/Video (LVDS2/SAI1)
X50	AV-Connector audio + control 30-pin header 2 mm	
X52	M.2 Key-E	M.2 Key-E (X52)
X54	M.2 Key-M	M.2 Key-M (X54)
X60	Micro SD-Card receptacle	Secure Digital Memory Card / MultiMedia Card (X60)
X68	Fan Connector 4-pin	Fan (X68)
X71	SPI-ADC input 10-pin header 2,54 mm	SPI-ADC (X71)
X73	ADC input 10-pin header 2,54 mm	ADC (X73)
X74, X75, X76, X79, X88, X89, X92, X93, X96, X97, X100, X101	GND Stud	
X105-X110, X115-X118	FPSC reserved a 20-pin socket 2 mm	

Warning

Ensure that all module connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, the user must take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

26.2.2 LEDs

FIGURE 11: Libra Development Board LEDs (Top)

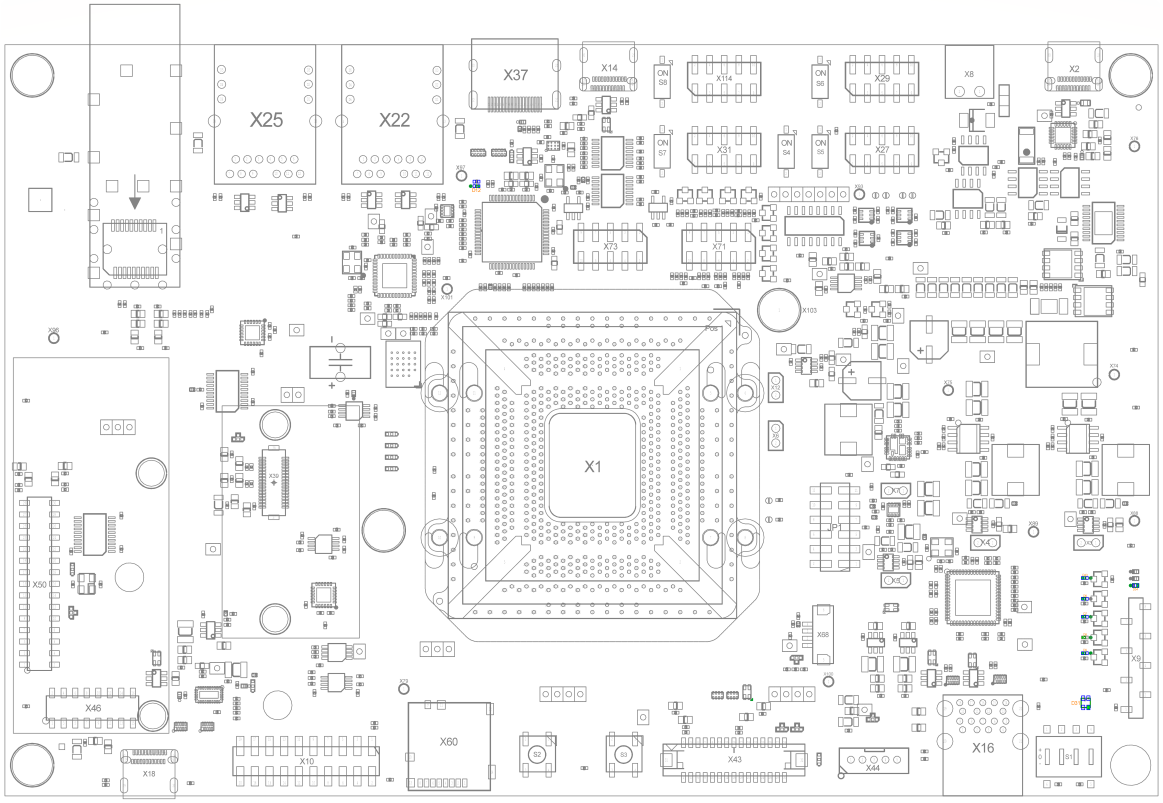
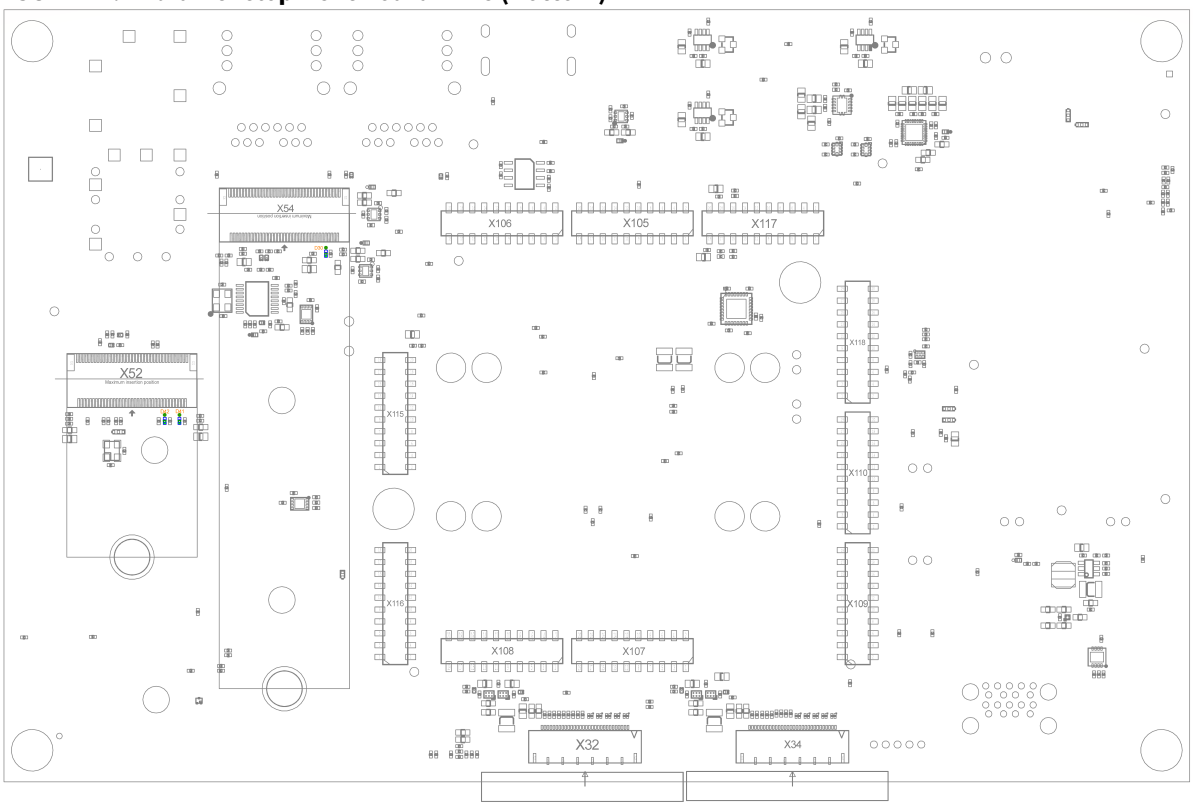


FIGURE 12: Libra Development Board LEDs (Bottom)



The Libra Development Board is populated with 7 LEDs. Libra Development Board Components (Top) and Libra Development Board Components (Bottom) show the location of the LEDs. Their functions are listed in the table below:

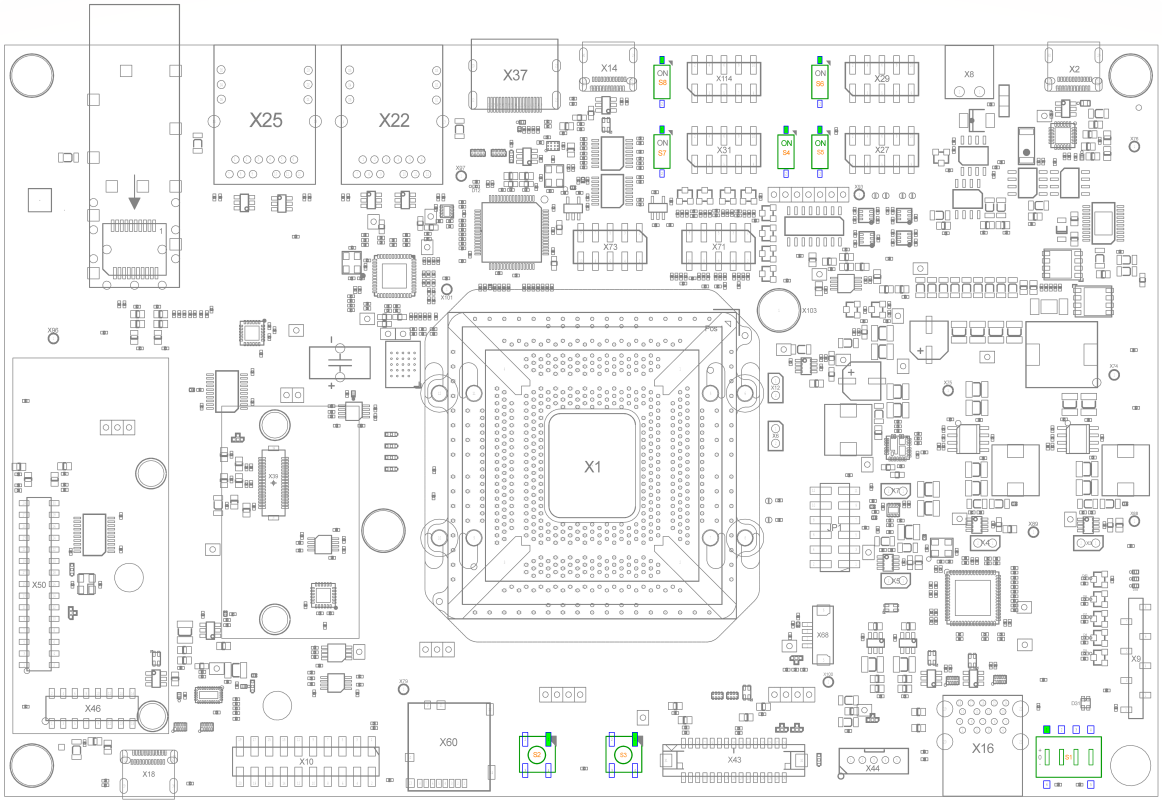
TABLE 45: Libra Development Board LED Descriptions

LED	Color	Description	Section
D6	Blue	VDD_5V0 good indicator	
D7	Blue	VDD_3V3 good indicator	
D8	Blue	VDD_1V8 good indicator	
D9	Blue	VDD_SOM good indicator	
D12	Red	Debug USB-C VBUS good indicator	
D30	Yellow	M.2 SSD activity indicator	
D31	RGB	Multi-color LED user-controllable	Multicolor (RGB) LED (D31)

LED	Color	Description	Section
D41	Yellow	M.2 status LED 1#	
D42	Yellow	M.2 status LED 2#	
D43	Blue	VDD_12V0 good indicator	

26.2.3 Switches and Buttons

FIGURE 13: Libra Development Board Switch Locations



The Libra Development Board is populated with multiple switches and buttons. The table below shows their functions:

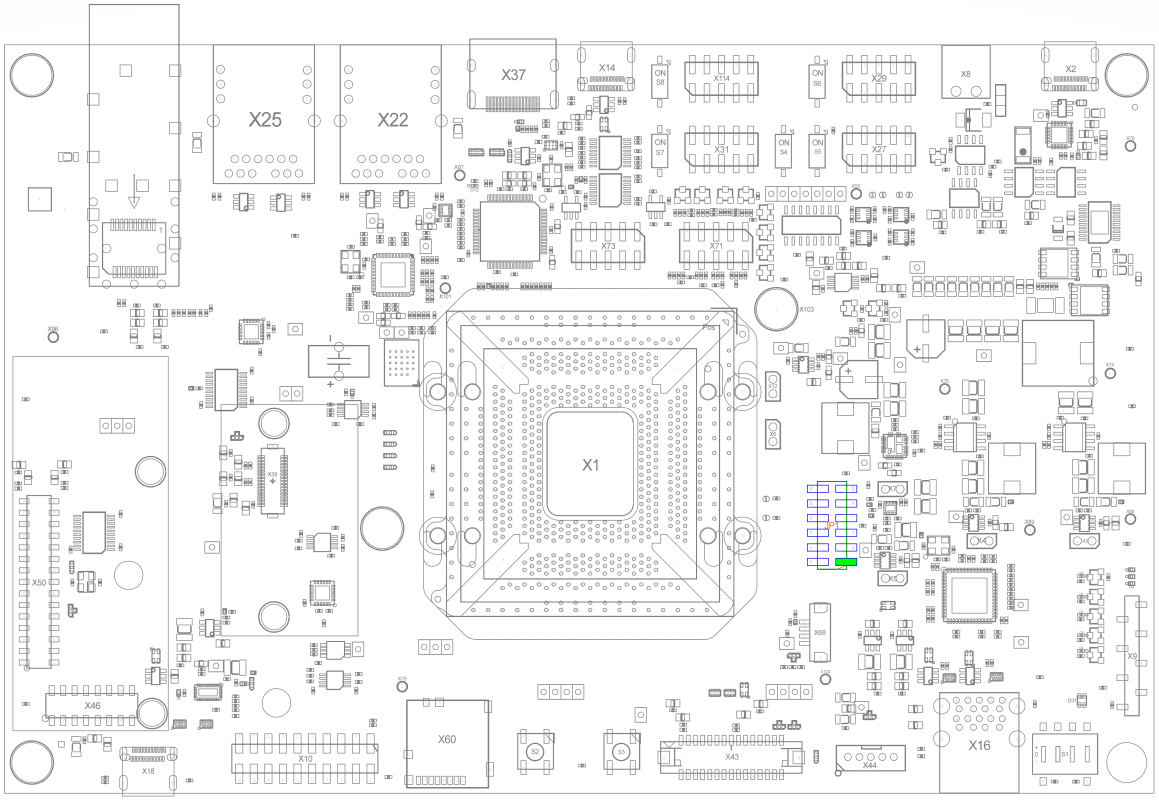
TABLE 46: Libra Development Board Switches

Switch	Description	Section
S1	4-port tri-state Boot Mode switch	Boot Switch (S1)
S2	Reset push button	System Reset Button (S2)
S3	ON/OFF push button	System ON/OFF Button (S3)
S4	RS485 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	
S5	UART1 target switch ON: UART1 is converted to RS232 OFF: UART1 is converted to RS485	

Switch	Description	Section
S6	CAN FD1 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	
S7	CAN FD2 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	
S8	CAN FD3 termination switch ON: Bus is terminated with 120 Ω OFF: Bus is not terminated	

26.2.4 Jumpers

FIGURE 14: Jumper (JP1)



The Libra Development Board comes pre-configured with several removable jumpers (JP) and solder jumpers (J). These jumpers enable the flexible configuration of a limited number of features for development purposes.

Warning

Due to the small footprint of the solder jumpers (J), PHYTEC does not recommend manual jumper modifications. This may also render the warranty invalid. Only the removable jumper (JP) is described in this section. Contact our sales team if you need jumper configurations different from the default configuration.

The function of the removable jumper on the Libra Development Board is shown below. More detailed information can be found in the appropriate section.

TABLE 47: Libra Development Board Jumper Settings

Jumper	Position	Default	Description	Section
JP1		1+2 3+4 5+6 9+10	UART3_RXD - USB Debug 1 UART3_TXD - USB Debug 1 UART2_RXD - USB Debug 2 UART2_TXD - USB Debug 2	

26.3 Libra Development Board Component Detail

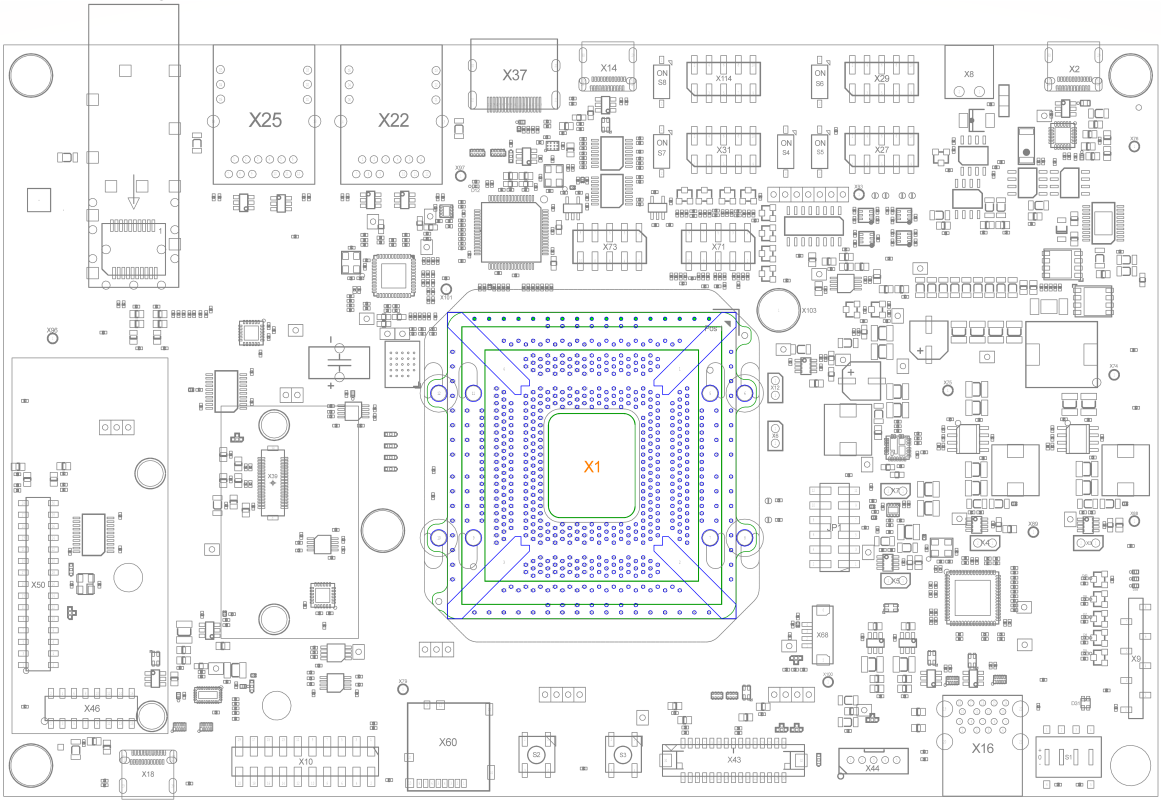
This section provides a more detailed look at the Libra Development Board components. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

Tip

Where possible, we also provide useful information regarding design considerations for components. This can be used if you plan to design your own carrier board.

26.3.1 phyFLEX Connector (X1)

FIGURE 15: phyFLEX Connector (X1)

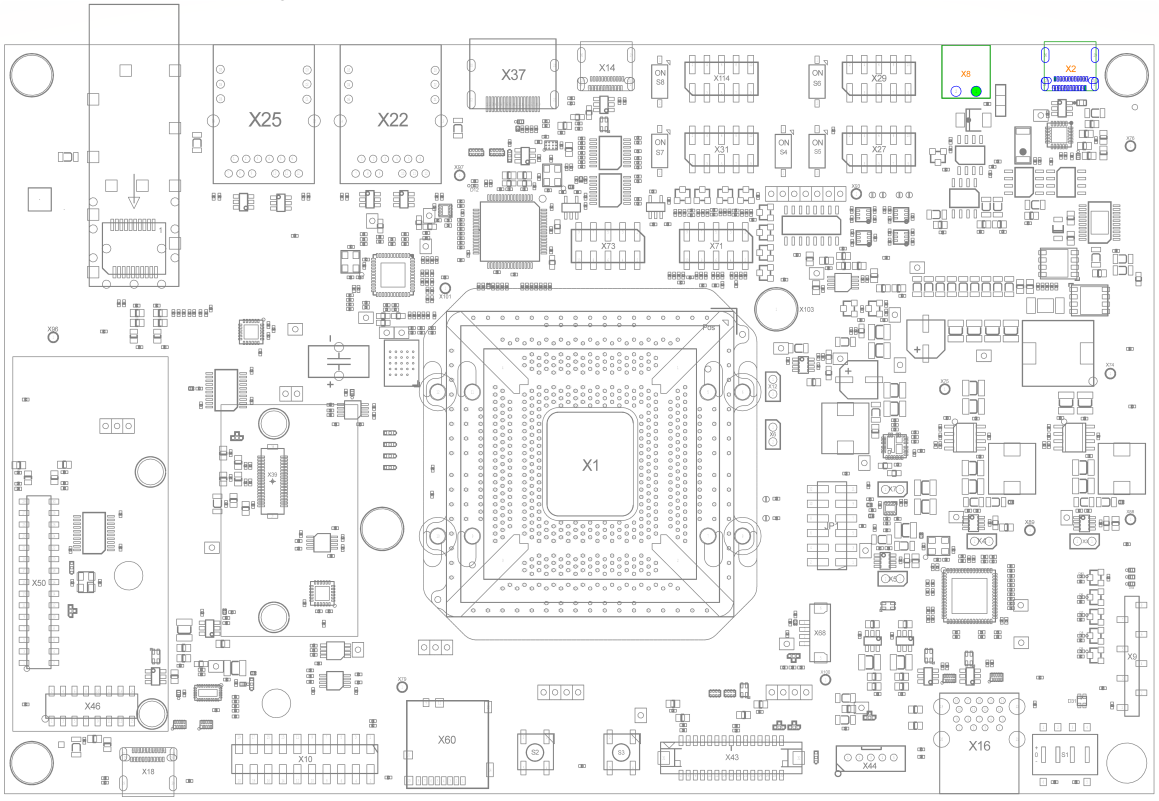


26.3.2 Power Supply (X2/X8)

Warning

Do not change modules or jumper settings while the Libra Development Board is supplied with power!

FIGURE 16: Power Supply Connectors (X2/X8)



The Libra Development Board can be powered either by a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X8) or by a USB Power Delivery Supply (X2).

Warning

Do not power the Libra Development Board via X2 and X8 at the same time!
Do not connect a USB device that is not a certified USB Power Delivery supply to X8!

The Libra Development Board is available with one power supply connector, a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X8) suitable for a single 24 V supply voltage. The required capacity for all power supply solutions depends on the specific configuration of the phyFLEX-SoM mounted on the Libra Development Board, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board.

The permissible input voltage is 24 V DC if your Development Board is equipped with a 2-pole Phoenix Contact MINI COMBICON base strip. A 24 V power supply capable of providing at least 3.5 A is recommended to power the board via the 2-pole base strip. The pin assignment for power supply connector X8:

TABLE 48: X8 Pin Assignment

Interface Pin #	Signal	Description
1	VDD_IN_PWR_CON	24 V ± 10%, 85 W
2	GND	Ground

26.3.2.1 USB Power Delivery Connector (X2)

The Libra Development Board can be powered by a USB Power Delivery Supply. The Libra Development Board provides the needed voltage and current from the connected supply and enables the on-board voltages. A 85 W USB-PD supply is recommended to power the Libra Development Board.

> **Note**
>
> Please note that connector X2 is only usable as a power supply input. It doesn't offer any USB communication interface functionality. Only use a certified USB Power Delivery supply.

26.3.2.2 RTC Backup Supply

The Libra Development Board has a double-layer capacitor equipped to back up the VDD_RTC rail of the phyFLEX FPSC SoM. The capacitor is also charged through a diode circuit from VDD_3V3. The mounted 330 mF capacitor is capable of backing up the SoM RTC for at least (TBD) at 25 °C.

26.3.3 UART

The Libra Development Board features 3 UART interfaces. This paragraph describes their default and alternative purposes.

UART1 (full flow control) is configurable to provide one of three functions via 2 integrated switches (U38/U40) and one hardware switch S5. The following table explains the necessary settings for a desired UART1 target:

TABLE 49: UART1 Target Selection

UART1 Target	S5	U38	U40
Bluetooth over M.2 Key-E	X	UART1_BT_RS_SEL = 1 Default = 0	X
RS232 at X27 through U37	0	UART1_BT_RS_SEL = 0	UART1_RS232_485_SEL = 1 S5 override GPIO

UART1 Target	S5	U38	U40
RS485 at X27 through U39	1	UART1_BT_RS_SEL = 0	UART1_RS232_485_SEL = 0 S5 override GPIO

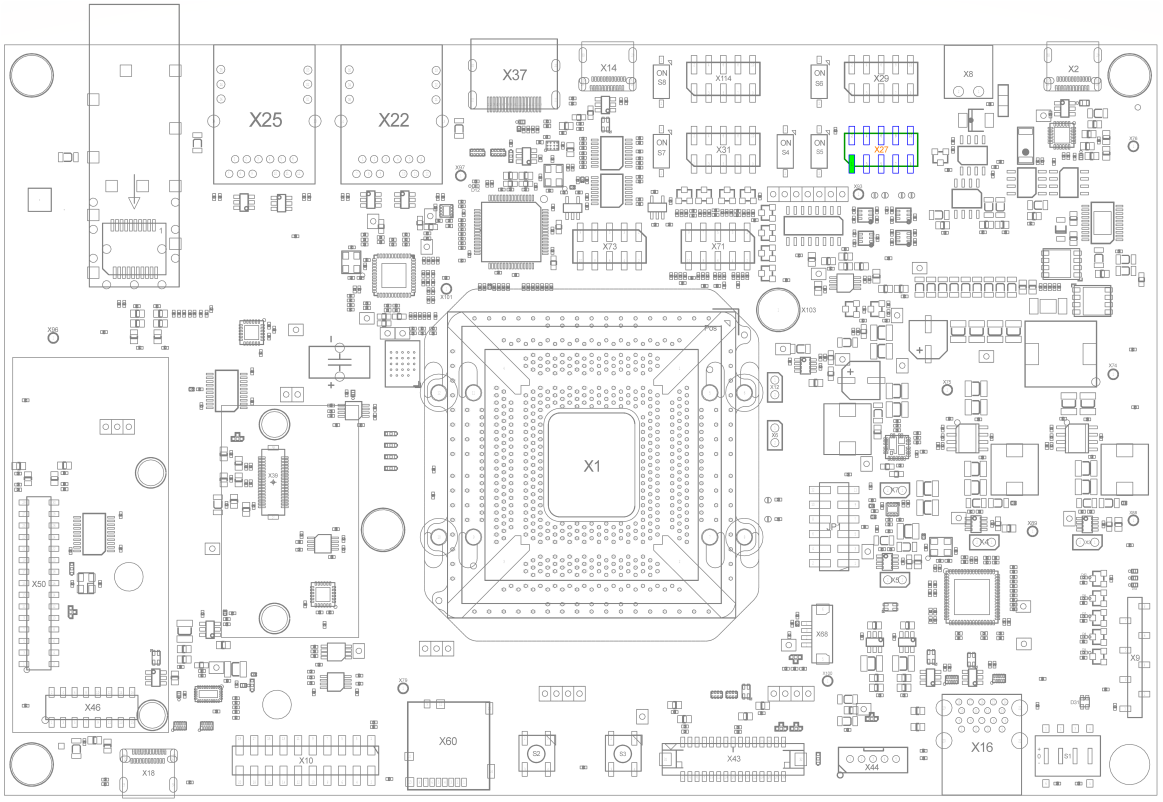
UART2 (full flow control) is connected to the USB debug channel 2 via the default setting of JP1. UART3 is connected to the USB debug channel 1 via the default setting of JP1.

26.3.3.1 UART Design Considerations

When designing a custom carrier board, remember the FPSC output TTL level is 1.8 V.

26.3.4 RS-232/RS-485 (X27)

FIGURE 17: RS-232 and RS-485 Connector (X27)



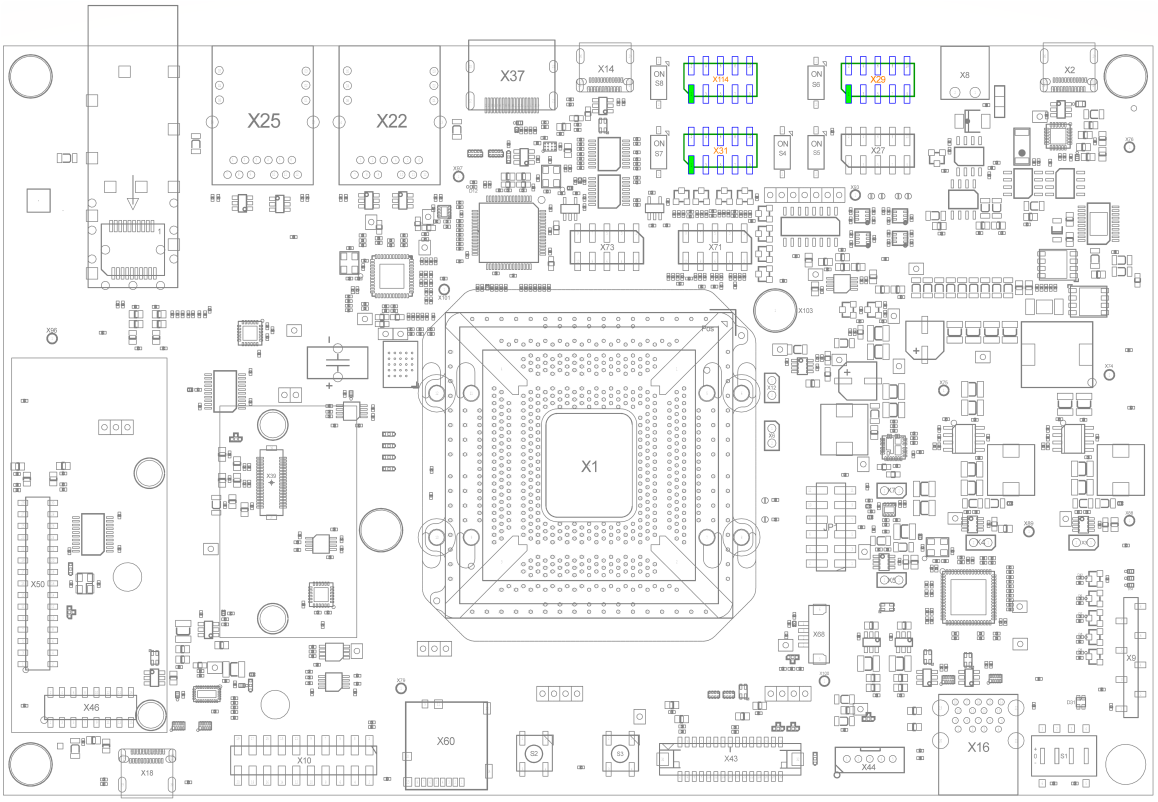
Pin header connector X27 provides the UART1 signals of the phyFLEX FPSC SoM as either RS-232 or RS-485 signal. Mode is selected by routing UART1 to the applicable converter. Please refer to the UART1 Target Selection. The RS-232 interface is intended to be used as data terminal equipment (DTE) and allows for a 5-wire connection, including the signals RTS and CTS for hardware flow control. RS-485 is available in Half-Duplex (4-wire). The table below shows the signal mapping of the RS-232 and RS-485 level signals at connector X27.

TABLE 50: RS-232/RS-485 (X27) Pin Assignment

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	NC	-	-	No connect
3	X_RS232_RXD	I	-	RS232 receive data
4	X_RS232_RTS	O	-	RS232 request to send
5	X_RS232_TXD	O	-	RS232 transmits data
6	X_RS232_CTS	I	-	RS232 clear to send
7	X_RS485_A	I/O	-	RS485 non-inverted
8	X_RS485_B	I/O	-	RS485 inverted
9	GND	-	0.0 V	Ground
10	GND	-	0.0 V	Ground

26.3.5 CAN FD (X29/X31/X114)

FIGURE 18: CAN FD (X29/X31/X114)



The phyFLEX FPSC SoM FLEXCAN1, FLEXCAN2, and FLEXCAN3 interfaces are brought out at X29, X31 and X114, each as CAN FD. The maximum permissible CAN FD data rate is 8 Mbit/s. For development purposes, a 120 Ω termination can be added by closing SW5 (CAN1), SW6 (CAN2) or SW8 (CAN3). For standard use, it is possible to mount a more suitable split termination in a customer-specific BOM.

The pinout is chosen to fit the official standard CAN pinout and is displayed in the table below.

TABLE 51: CAN FD1 (X29) Pin Assignment

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	GND	-	0.0 V	Ground
3	X_CAN1_L	CAN_I/O	-	Low-level CAN bus input/output line
4	X_CAN1_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	0.0 V	Ground
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	NC	-	-	No connect
10	NC	-	-	No connect

TABLE 52: CAN FD2 (X31) Pin Assignment

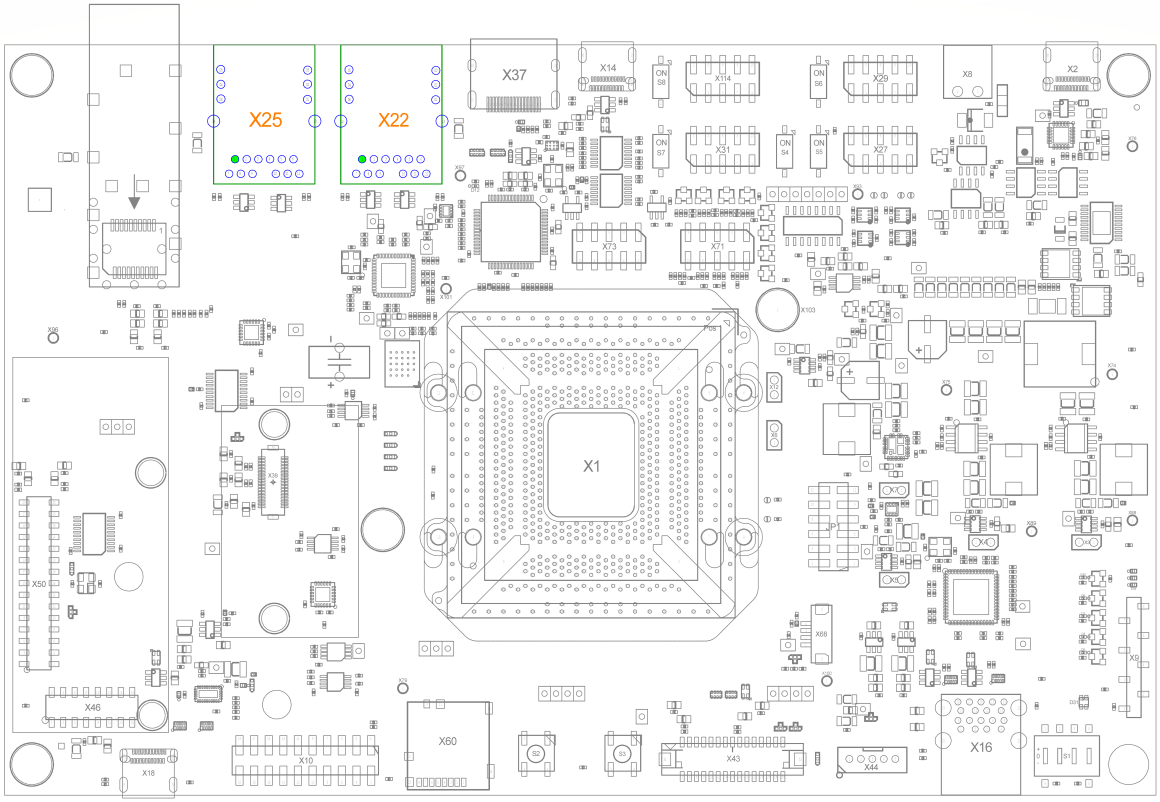
Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	GND	-	0.0 V	Ground
3	X_CAN2_L	CAN_I/O	-	Low-level CAN bus input/output line
4	X_CAN2_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	0.0 V	Ground
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	NC	-	-	No connect
10	NC	-	-	No connect

TABLE 53: CAN FD3 (X114) Pin Assignment

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	GND	-	0.0 V	Ground
3	X_CAN3_L	CAN_I/O	-	Low-level CAN bus input/output line
4	X_CAN3_H	CAN_I/O	-	High-level CAN bus input/output line
5	GND	-	0.0 V	Ground
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	NC	-	-	No connect
10	NC	-	-	No connect

26.3.6 Ethernet (X22/X25)

FIGURE 19: Ethernet Connectors (X22/X25)



The Libra Development Board is equipped with 2 RJ45 connectors. The table below describes the properties of each Ethernet interface:

TABLE 54: RJ45 Ethernet connectors X22/X25

Interface Name	Ethernet Connector	Interface Description
Ethernet2	X22	10/100/1000 Ethernet interface over a Gigabit Ethernet transceiver on a carrier board
Ethernet1	X25	10/100/1000 Ethernet interface over a Gigabit Ethernet transceiver on a mounted SoM

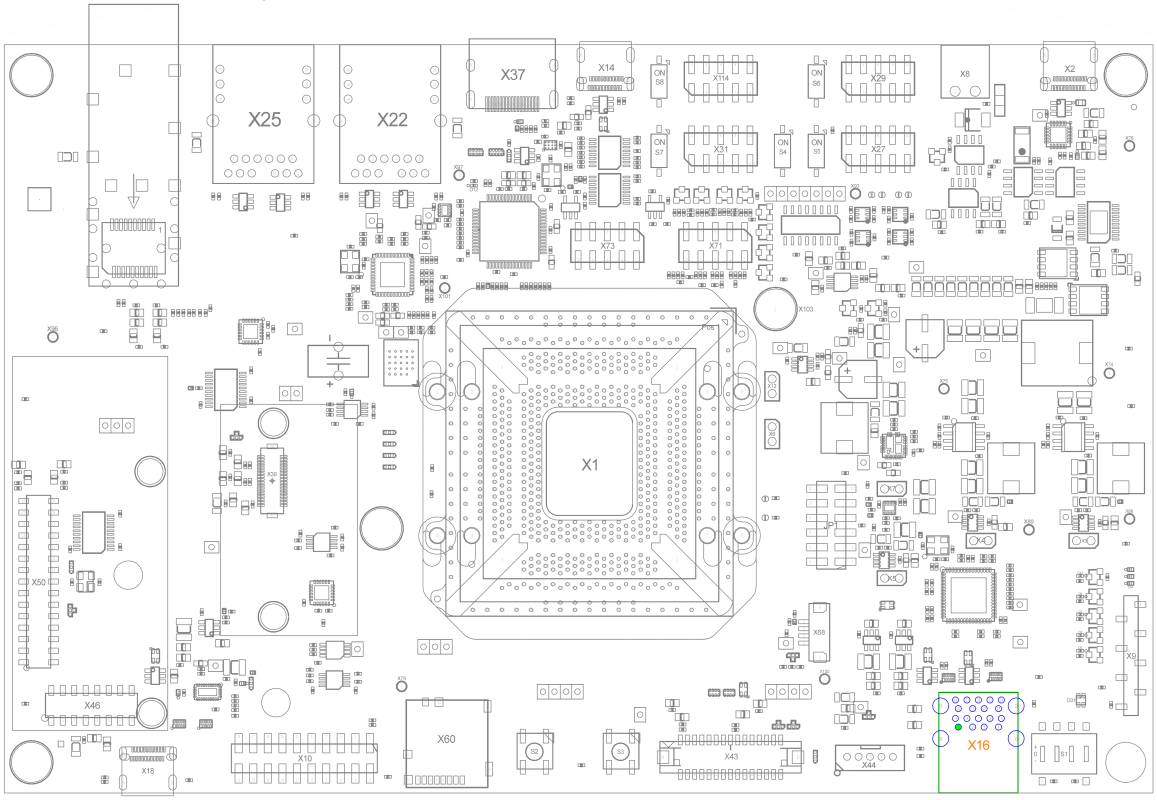
The LEDs for LINK (green) and ACTIVITY (orange) indications are integrated into the connector. The Ethernet transceivers support Auto MDI-X, eliminating the need for a direct connect LAN or cross-over path cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

26.3.6.1 Ethernet Design Considerations

The data lanes should be routed with a differential impedance of 100 Ohms. The center taps of each pair's transformer have to be connected to GND through a 100nF capacitor. The LED pins are open-drain outputs of the SoM without a resistor, so they should be connected to the cathodes of the LEDs through a resistor.

26.3.7 USB Dual Type-A 3.0 Interface (X16)

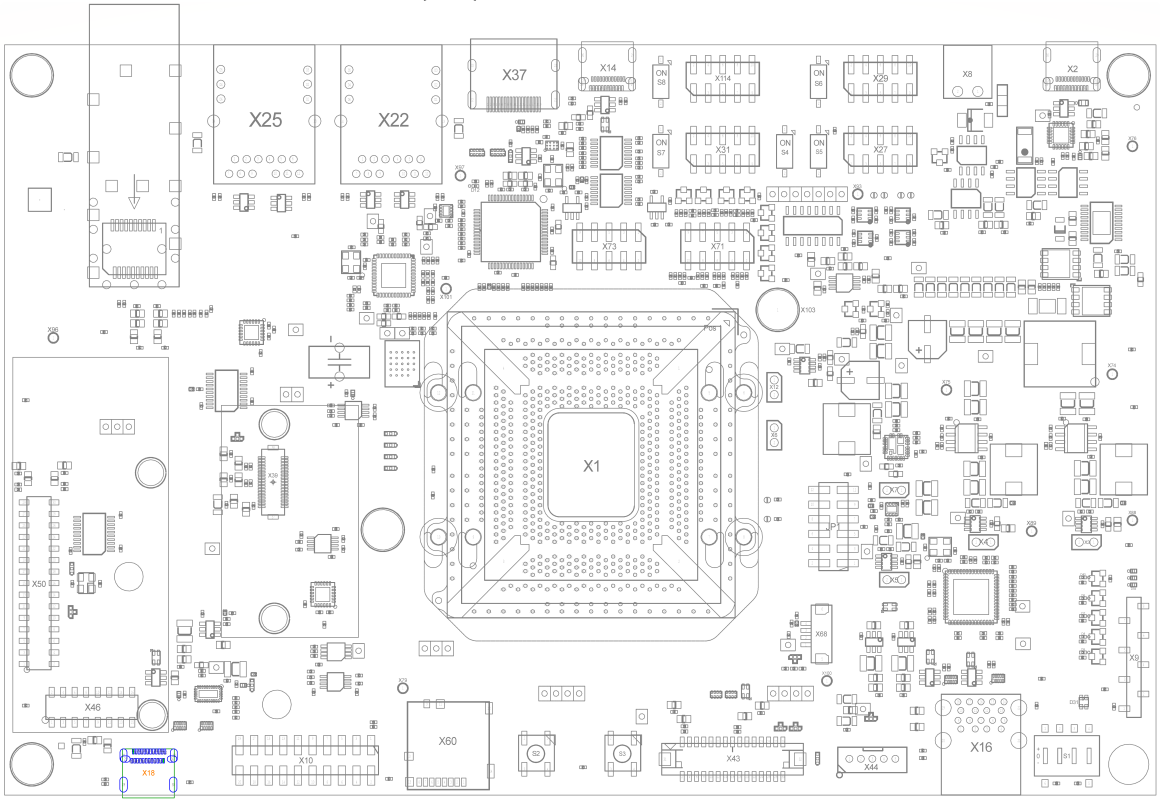
FIGURE 20: USB Dual Type-A 3.0 Connector (X16)



The Libra Development Board provides two USB 3.0 interfaces at the USB Dual Type-A connector X16. They are HOST interfaces made available through a 4-port USB HUB. USB1 will be at the connector's top and USB2 at the bottom receptacle.

26.3.8 USB-C 3.2 GEN 1 Interface (X18)

FIGURE 21: USB 3.2 Gen1 Connector (X18)



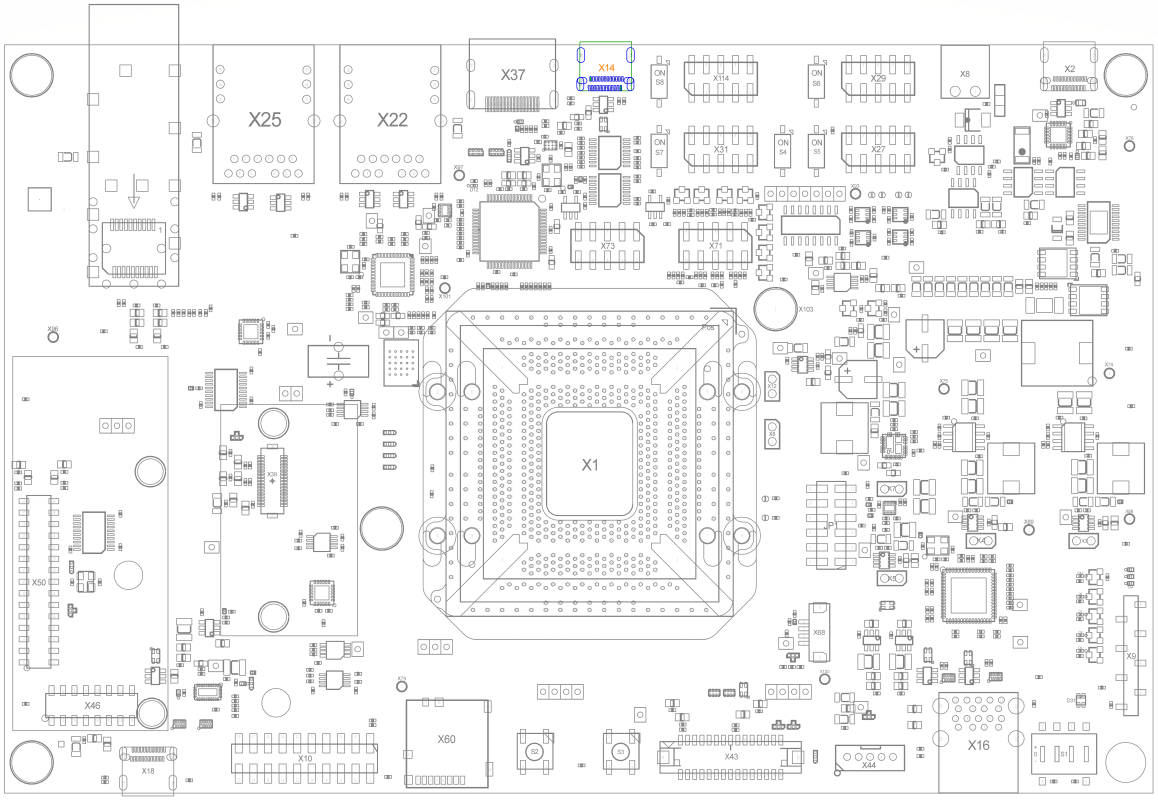
The Libra Development Board provides a USB-C 3.2 GEN 1 Dual Role interface. Muxing of super-speed differential data lanes is handled through a dedicated muxing IC (U66). The mounted SoM's USB Serial Downloader requires this interface to be able to boot from USB.

26.3.8.1 USB 3.2 Gen1 Design Considerations

Series capacitors are already present on the phyFLEX FPSC SoM. It is not necessary to provide additional series capacitors in the TX lines. Double-check the signal direction of the high-speed lines where TX is output and RX is input on the phyFLEX FPSC SoM. The TX and RX lines should be routed with an impedance of 50 Ohms to a ground plane and 100 Ohms differential impedance. Route USB 2.0 data lines with 45 Ohms to Ground and 90 Ohms differential impedance.

26.3.9 USB Debug (X14)

FIGURE 22: USB Debug Connector (X14)



The primary debug interface is UART3. UART2 is the special debug interface used to connect to an M-core or similar provided by the SoM. Both UART interfaces are connected to a UART-to-USB converter (U15 FTDI FT4232H). The USB 2.0 interface is brought out at a USB-C socket (X14). Use the following terminal settings to connect to the Libra Development Board serial interfaces:

- Speed: 115200 baud
- Data bits: 8
- Stop bits: 1
- Parity: None
- Flow control: None

The USB debug interface is also capable of manipulating the Boot Mode signals through FT4232H bank D and triggering a reset through FT4232H bank C. BOOT_MODE manipulation has to be enabled by pulling the signal DEBUG_BOOT_EN (DDBUS4 at U15) high.

The table below shows the pinout of the USB Debug connector:

TABLE 55: X14 Pin Assignment

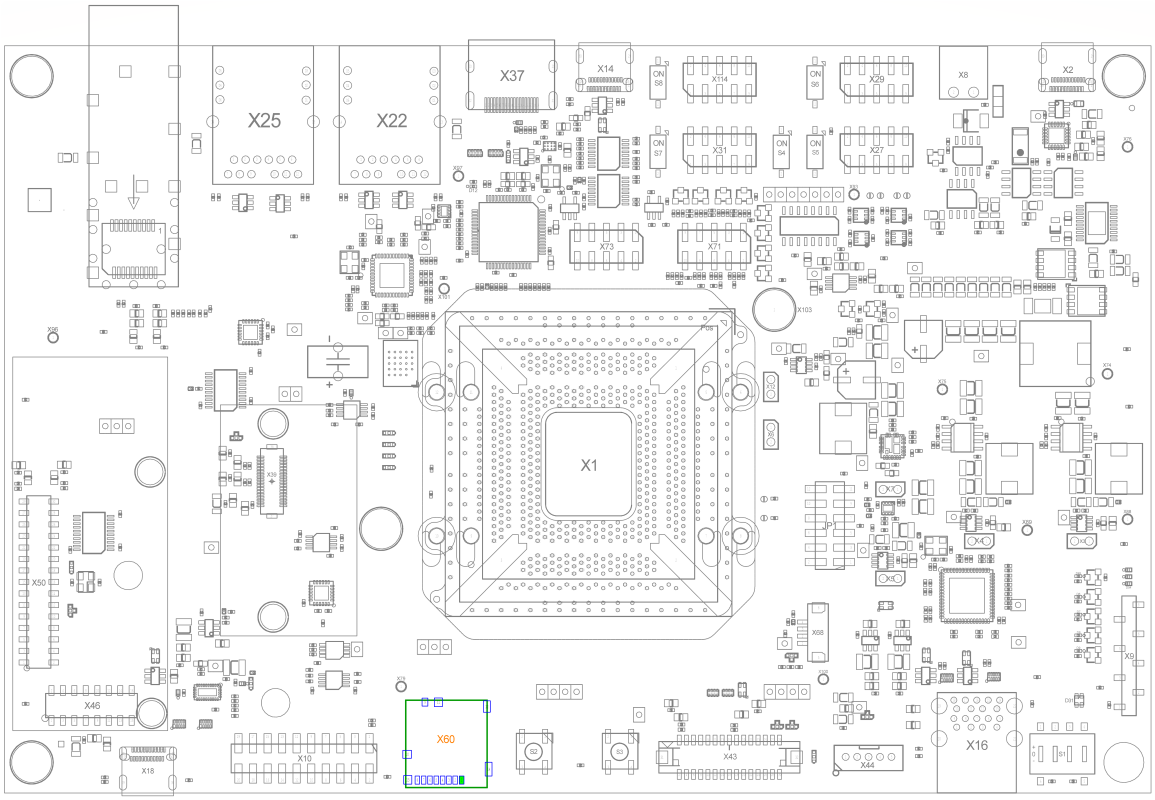
Interface Pin #	Signal name	Signal Type	Signal Level	Description
A1	GND	-	0.0 V	Ground
A2	NC	-	-	No connect
A3	NC	-	-	No connect
A4	VBUS	I	5.0 V	USB VBUS provided by Host
A5	CC1	I/O	-	Configuration channel 5k1 pull down
A6	X_DEBUG_USB_DP	USB_I/O	-	USB Debug Data+
A7	X_DEBUG_USB_DM	USB_I/O	-	USB Debug Data-
A8	NC	-	-	No connect
A9	VBUS	I	5.0 V	USB VBUS provided by Host
A10	NC	-	-	No connect
A11	NC	-	-	No connect
A12	GND	-	0.0 V	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
B1	GND	-	0.0 V	Ground
B2	NC	-	-	No connect
B3	NC	-	-	No connect
B4	VBUS	I	5.0 V	USB VBUS provided by Host
B5	CC2	I/O	-	Configuration channel 5k1 pull down
B6	X_DEBUG_USB_DP	USB_I/O	-	USB Debug Data+
B7	X_DEBUG_USB_DM	USB_I/O	-	USB Debug Data-
B8	NC	-	-	No connect
B9	VBUS	I	5.0 V	USB VBUS provided by Host
B10	NC	-	-	No connect
B11	NC	-	-	No connect
B12	GND	-	0.0 V	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	GND	-	0.0 V	Ground
26	GND	-	0.0 V	Ground
27	GND	-	0.0 V	Ground
28	GND	-	0.0 V	Ground
29	GND	-	0.0 V	Ground
30	GND	-	0.0 V	Ground

26.3.10 Secure Digital Memory Card / MultiMedia Card (X60)

FIGURE 23: SD / MM Card Connector (X60)



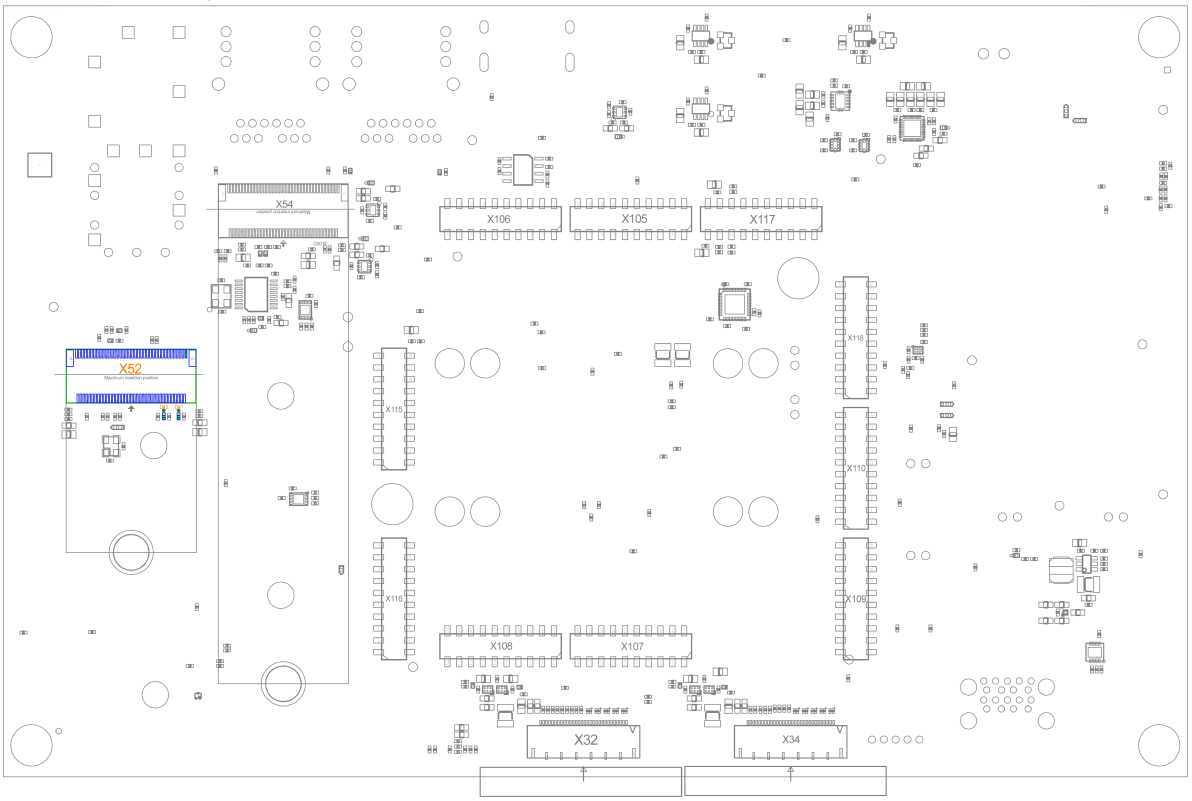
The Libra Development Board provides a standard microSDHC card slot at X60 for use with SD/MMC interface cards. It allows for a fast, easy connection to peripheral devices like microSD and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC connector. It also features card detection, a lock mechanism, and a smooth extraction function by pushing the card in and out.

26.3.10.1 SD / MM Card Design Considerations

Series resistors might be required to adapt the drive strength of the card. SD interface should be routed with an impedance of 50 Ohms to a ground plane. The trace length between CLK, CMD, and DATA lanes should be matched and kept as short as possible. Avoid Vias and take care of the signal current return path.

26.3.11 M.2 Key-E (X52)

FIGURE 24: M.2 Key-E Connector (X52)



The 1-lane PCI Express interface provides PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. Various control signals are implemented with GPIOs. The PCIE1 interface is brought out at the M.2 Key-E connector X52 shown above. The M.2 Key-E connector also features UART with flow-control, SDIO, I2C and USB 2.0.

The table below shows in-depth information, such as pin assignment and signals used to implement special features of the Mini PCIe interface.

TABLE 56: X52 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	0.0 V	Ground
2	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
3	X_USB_HUB_DN1_P	USB_I/O	-	USB 2.0 Data+
4	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
5	X_USB_HUB_DN1_N	USB_I/O	-	USB 2.0 Data-
6	LED_1	I	3,3 V	Status LED 1
7	GND	-	0.0 V	Ground
8	NC	-	-	No connect
9	X_SDIO_CLK	O	1.8 V	SDIO clock signal
10	NC	-	-	No connect
11	X_SDIO_CMD	O	1.8 V	SDIO command signal
12	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_SDIO_D0	I/O	1.8 V	SDIO data 0 signal
14	NC	-	-	No connect
15	X_SDIO_D1	I/O	1.8 V	SDIO data 1 signal
16	LED_2	I	3.3 V	Status LED 2
17	X_SDIO_D2	I/O	1.8 V	SDIO data 2 signal
18	GND	-	0.0 V	Ground
19	X_SDIO_D3	I/O	1.8 V	SDIO data 3 signal
20	X_UART1_nWAKE	O	3.3 V	UART1 sideband platform wake signal
21	X_SDIO_nWAKE	O	1.8 V	SDIO sideband wake signal
22	X_UART1_RXD_BT	I	1.8 V	UART1 receive data signal
23	X_SDIO_nRESET	PCIE_I	1.8 V	SDIO sideband enable/disable (reset) signal
24	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	NC	-	-	No connect
27	NC	-	-	No connect
28	NC	-	-	No connect
29	NC	-	-	No connect
30	NC	-	-	No connect
31	NC	-	-	No connect
32	X_UART1_TXD_BT	O	1.8 V	UART1 transmit data signal
33	GND	-	0.0 V	Ground
34	X_UART1_CTS	I	1.8 V	UART1 clear to send signal
35	X_PCIE1_TXN_P	O	-	PCI Express 1 positive transmit data signal
36	X_UART1_RTS	O	1.8 V	USB 2.0 Data-

Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	X_PCIE1_TXN_N	O	-	PCI Express 1 negative transmit data signal
38	NC	-	-	No connect
39	GND	-	0.0 V	Ground
40	NC	-	-	No connect
41	X_PCIE1_RXN_P	I	-	PCI Express 1 positive receive data signal
42	NC	-	-	No connect
43	X_PCIE1_RXN_N	I	-	PCI Express 1 negative receive data signal
44	TP84	O	1.8 V	Test point for COEX3 signal
45	GND	-	0.0 V	Ground
46	TP85	I	1.8 V	Test point for COEX_RXD signal
47	X_PCIE1_CLK_P	O	-	PCI Express 1 positive reference clock signal
48	TP86	O	1.8 V	Test point for COEX_TXD signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
49	X_PCIE1_CLK_N	O	-	PCI Express 1 negative reference clock signal
50	X_KEY-E_32k_SUSCLK	O	3.3 V	32768 Hz suspend clock signal
51	GND	-	0.0 V	Ground
52	X_PCIE1_nPERST_3V3		3.3 V	PCI Express 1 add-in card reset
53	X_PCIE1_nCLKREQ_3V3	I/O	3.3 V	PCI Express 1 clock request signal
54	X_W_nDISABLE1	O	3.3 V	Disable radio operation on add-in card 1 signal
55	X_PCIE1_nWAKE	I/O	3.3 V	PCI Express wake signal, OBFF
56	X_W_nDISABLE2	O	3.3 V	Disable radio operation on add-in card 2 signal
57	GND	-	0.0 V	Ground
58	X_I2C3_SDA	I/O	1.8 V	I2C3 serial data signal
59	NC	-	-	No connect
60	X_I2C3_SCL	O	1.8 V	I2C3 serial clock signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
61	NC	-	-	No connect
62	X_KEY-E_nALERT	I	1.8 V	Key-E interrupt signal
63	GND	-	0.0 V	Ground
64	NC	-	-	No connect
65	NC	-	-	No connect
66	NC	-	-	No connect
67	NC	-	-	No connect
68	NC	-	-	No connect
69	GND	-	0.0 V	Ground
70	NC	-	-	No connect
71	NC	-	-	No connect
72	VDD_3V3	PWR_O	3.3 V	3.3 V power rail

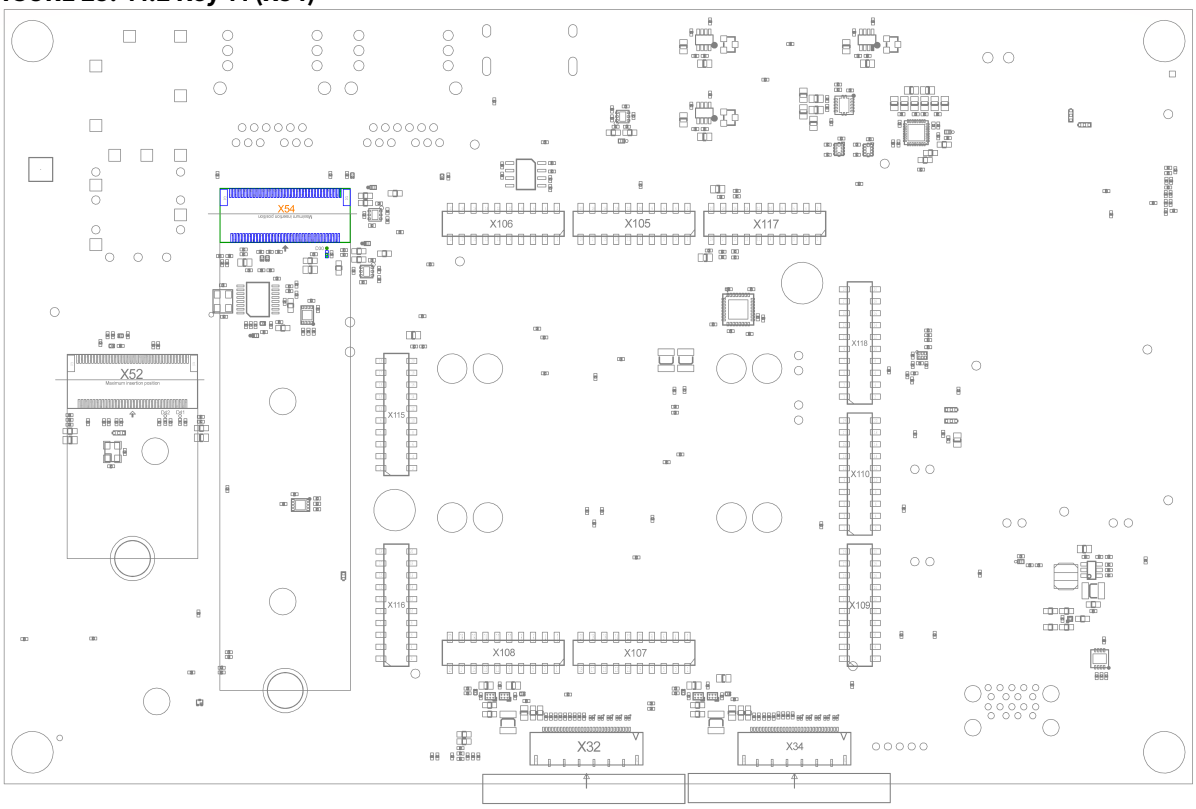
Interface Pin #	Signal name	Signal Type	Signal Level	Description
73	NC	-	-	No connect
74	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
75	GND	-	0.0 V	Ground
S1	GND	-	0.0 V	Ground
S2	GND	-	0.0 V	Ground

26.3.11.1 PCIe Design Considerations

100nF AC coupling capacitors are placed at the output of the phyFLEX FPSC SoM in series to the TX lanes. A clock generator on the carrier board generates the PCIe clock.

26.3.12 M.2 Key-M (X54)

FIGURE 25: M.2 Key-M (X54)



The second 1-lane PCI Express interface provides PCIe Gen. 3.0 functionality, which supports up to 8 GT/s operations. The mounted M.2 Key-M connector is mainly used for SSD cards. Various control signals are implemented with GPIOs. The PCIE2 interface is brought out at the M.2 Key-M connector X54 shown above. The PCIe clock is generated by the dedicated PCIe clock generator U51. This feature is not available for all mountable FPSC SoMs.

The table below shows in-depth information, such as pin assignment and signals used to implement special features of the M.2 Key-M interface.

TABLE 57: X54 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	0.0 V	Ground
2	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
3	GND	-	0.0 V	Ground
4	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
5	NC	-	-	No connect
6	NC	-	-	No connect
7	NC	-	-	No connect
8	NC	-	-	No connect
9	GND	-	0.0 V	Ground
10	LED1	I	3.3 V	M.2 Key-M activity LED signal
11	NC	-	-	No connect
12	VDD_3V3	PWR_O	3.3 V	3.3 V power rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	NC	-	-	No connect
14	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
15	GND	-	0.0 V	Ground
16	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
17	NC	-	-	No connect
18	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
19	NC	-	-	No connect
20	NC	-	-	No connect
21	GND	-	0.0 V	Ground
22	NC	-	-	No connect
23	NC	-	-	No connect
24	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	NC	-	-	No connect
27	GND	-	0.0 V	Ground
28	NC	-	-	No connect
29	NC	-	-	No connect
30	NC	-	-	No connect
31	NC	-	-	No connect
32	NC	-	-	No connect
33	GND	-	0.0 V	Ground
34	NC	-	-	No connect
35	NC	-	-	No connect
36	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	NC	-	-	No connect
38	NC	-	-	No connect
39	GND	-	0.0 V	Ground
40	X_I2C2_SCL	O	1.8 V	I2C2 serial clock
41	X_PCIE2_TXN_N	O	-	PCI Express 2 negative transmit data signal
42	X_I2C2_SDA	I/O	1.8 V	I2C2 serial data
43	X_PCIE2_TXN_P	O	-	PCI Express 2 positive transmit data signal
44	X_KEY-M_nALERT	I	1.8 V	Key-M interrupt signal
45	GND	-	0.0 V	Ground
46	NC	-	-	No connect
47	X_PCIE2_RXN_N	I	-	PCI Express 2 negative receive data signal
48	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
49	X_PCIE2_RXN_P	I	-	PCI Express 2 positive receive data signal
50	X_PCIE2_nCLKREQ_3V3	I/O	3.3 V	PCI Express 2 clock request signal
51	GND	-	0.0 V	Ground
52	X_PCIE2_nPERST_3V3		3.3 V	PCI Express 2 add-in card reset
53	X_PCIE2_CON_REFPAD_CLK_N	O	-	PCI Express 2 negative reference clock signal
54	X_PCIE2_nWAKE	I/O	3.3 V	PCI Express wake signal, OBFF
55	X_PCIE2_CON_REFPAD_CLK_P	O	-	PCI Express 2 positive reference clock signal
56	NC	-	-	No connect
57	GND	-	0.0 V	Ground
58	NC	-	-	No connect
59	NC	-	-	No connect
60	NC	-	-	No connect

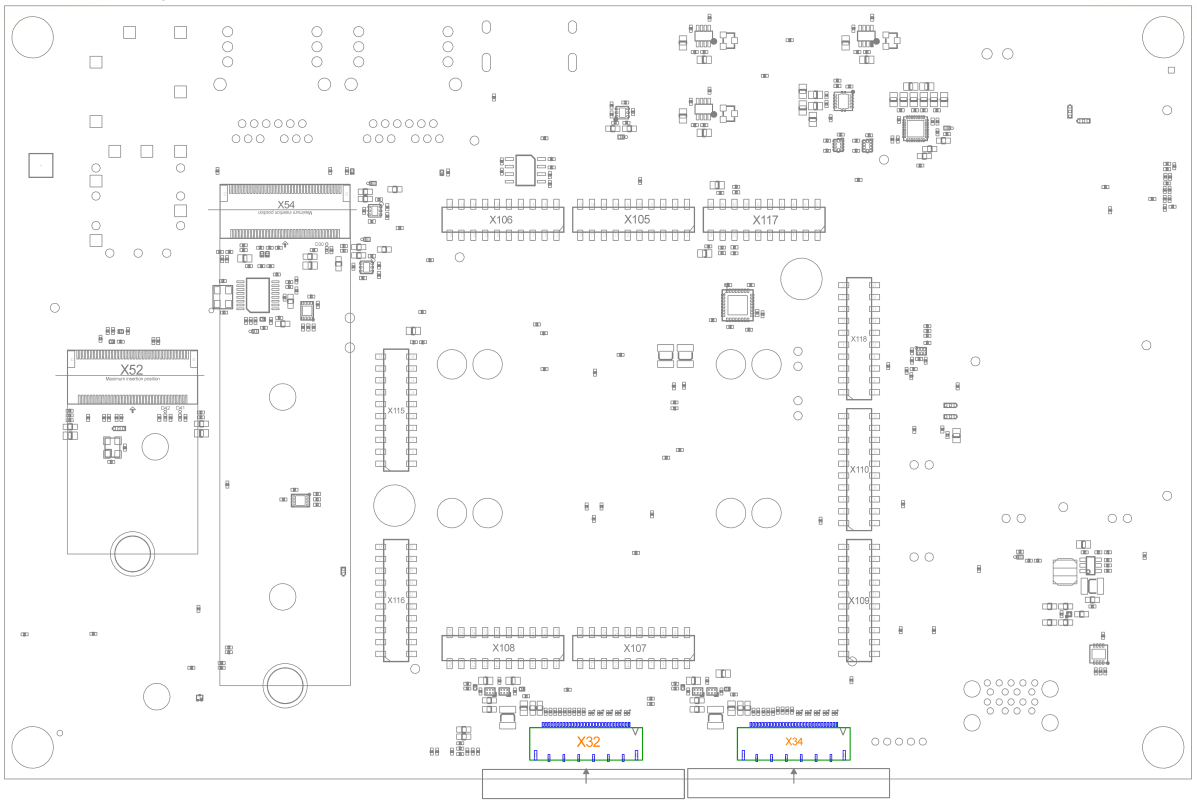
Interface Pin #	Signal name	Signal Type	Signal Level	Description
61	NC	-	-	No connect
62	NC	-	-	No connect
63	NC	-	-	No connect
64	NC	-	-	No connect
65	NC	-	-	No connect
66	NC	-	-	No connect
67	NC	-	-	No connect
68	X_KEY-M_32k_SUSCLK	O	3.3 V	32768 Hz suspend clock signal
69	NC	-	-	No connect
70	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
71	GND	-	0.0 V	Ground
72	VDD_3V3	PWR_O	3.3 V	3.3 V power rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
73	GND	-	0.0 V	Ground
74	VDD_3V3	PWR_O	3.3 V	3.3 V power rail
75	GND	-	0.0 V	Ground
S1	GND	-	0.0 V	Ground
S2	GND	-	0.0 V	Ground

26.3.13 Camera Connectivity

26.3.13.1 phyCAM-M MIPI CSI Camera Connectors (X32/34)

FIGURE 26: phyCAM-M MIPI CSI-2 Camera Connectors (X32/X34)



The phyFLEX FPSC SoM on the Libra Development Board offers 2 independent interfaces to connect digital camera boards with the MIPI CSI-2 interface. The 4-lane MIPI CSI-2 interfaces are brought out as phyCAM-M camera interfaces at connectors X32 and X34. The pin assignments of connectors X32 and X34 are shown below. The phyCAM-M camera connectors fit the phyCAM-M product family with various color and monochrome sensors. Suitable camera modules are, e.g., VM-016-COL-M (1 MPix) or VM-017-BW-M (5 Mpix), which can be delivered with a complete objective. Contact the PHYTEC Sales Team for advice on how to tailor a camera module to your application.

TABLE 58: MIPI CSI-2 Camera 1 (X32) Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_MIPI_CSI1_D0_P	MIPI CSI-2	-	MIPI CSI-2 data 0 positive signal
3	X_MIPI_CSI1_D0_N	MIPI CSI-2	-	MIPI CSI-2 data 0 negative signal
4	GND	-	-	Ground
5	X_MIPI_CSI1_D1_P	MIPI CSI-2	-	MIPI CSI-2 data 1 positive signal
6	X_MIPI_CSI1_D1_N	MIPI CSI-2	-	MIPI CSI-2 data 1 negative signal
7	GND	-	-	Ground
8	X_MIPI_CSI1_CLK_P	MIPI CSI-2	-	MIPI CSI-2 clock positive signal
9	X_MIPI_CSI1_CLK_N	MIPI CSI-2	-	MIPI CSI-2 clock negative signal
10	GND	-	-	Ground
11	X_MIPI_CSI1_D2_P	MIPI CSI-2	-	MIPI CSI-2 data 2 positive signal
12	X_MIPI_CSI1_D2_N	MIPI CSI-2	-	MIPI CSI-2 data 2 negative signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_MIPI_CSI1_D3_P	MIPI CSI-2	-	MIPI CSI-2 data 3 positive signal
15	X_MIPI_CSI1_D3_N	MIPI CSI-2	-	MIPI CSI-2 data 3 negative signal
16	GND	-	-	Ground
17	X_CSI1_CTRL4	OD-BI-PU	3.3 V	CSI1 control 4
18	X_CSI1_CTRL3	OD-BI-PU	3.3 V	CSI1 control 3
19	X_CSI1_CTRL2	OD-BI-PU	3.3 V	CSI1 control 2
20	X_CSI1_CTRL1	OD-BI-PU	3.3 V	CSI1 control 1
21	GND	-	-	Ground
22	X_I2C3_SCL_3V3	O	3.3 V	I2C3 serial clock
23	X_I2C3_SDA_3V3	I/O	3.3 V	I2C3 serial data
24	X_CSI1_ADDR	O	3.3 V	I2C camera address choice

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	X_CSI1_nRESET	O	3.3 V	Camera reset signal
26	X_CSI1_VDD_SELECT	OD-I-PU	3.3 V	Interface voltage selection: ▪ open = 3.3 V ▪ GND = 5 V
27	GND	-	-	Ground
28	VDD_CSI1_OUT	PWR_O	3.3 V / 5 V	Camera power supply
29	VDD_CSI1_OUT	PWR_O	3.3 V / 5 V	Camera power supply
30	VDD_CSI1_OUT	PWR_O	3.3 V / 5 V	Camera power supply

TABLE 59: MIPI CSI-2 Camera 2 (X34) Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_MIPI_CSI2_D0_P	MIPI CSI-2	-	MIPI CSI-2 data 0 positive signal
3	X_MIPI_CSI2_D0_N	MIPI CSI-2	-	MIPI CSI-2 data 0 negative signal
4	GND	-	-	Ground
5	X_MIPI_CSI2_D1_P	MIPI CSI-2	-	MIPI CSI-2 data 1 positive signal
6	X_MIPI_CSI2_D1_N	MIPI CSI-2	-	MIPI CSI-2 data 1 negative signal
7	GND	-	-	Ground
8	X_MIPI_CSI2_CLK_P	MIPI CSI-2	-	MIPI CSI-2 clock positive signal
9	X_MIPI_CSI2_CLK_N	MIPI CSI-2	-	MIPI CSI-2 clock negative signal
10	GND	-	-	Ground
11	X_MIPI_CSI2_D2_P	MIPI CSI-2	-	MIPI CSI-2 data 2 positive signal
12	X_MIPI_CSI2_D2_N	MIPI CSI-2	-	MIPI CSI-2 data 2 negative signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_MIPI_CSI2_D3_P	MIPI CSI-2	-	MIPI CSI-2 data 3 positive signal
15	X_MIPI_CSI2_D3_N	MIPI CSI-2	-	MIPI CSI-2 data 3 negative signal
16	GND	-	-	Ground
17	X_CSI2_CTRL4	OD-BI-PU	3.3 V	CSI2 control 4
18	X_CSI2_CTRL3	OD-BI-PU	3.3 V	CSI2 control 3
19	X_CSI1_CTRL1	OD-BI-PU	3.3 V	CSI1 control 1, Camera 2 is set up to be triggered by Camera 1 strobe output
20	X_CSI2_CTRL1	OD-BI-PU	3.3 V	CSI2 control 1
21	GND	-	-	Ground
22	X_I2C4_SCL_3V3	O	3.3 V	I2C4 serial clock
23	X_I2C4_SDA_3V3	I/O	3.3 V	I2C4 serial data
24	X_CSI2_ADDR	O	3.3 V	I2C camera address choice

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	X_CSI2_nRESET	O	3.3 V	Camera reset signal
26	X_CSI2_VDD_SELECT	OD-I-PU	3.3 V	Interface voltage selection: • open = 3.3 V • GND = 5 V
27	GND	-	-	Ground
28	VDD_CSI2_OUT	PWR_O	3.3 V / 5 V	Camera power supply
29	VDD_CSI2_OUT	PWR_O	3.3 V / 5 V	Camera power supply
30	VDD_CSI2_OUT	PWR_O	3.3 V / 5 V	Camera power supply

26.3.13.2 Camera Design Considerations

Regarding camera connections when designing a customer carrier board:

1. The differential impedance should be 100 Ohms for all lanes to a Ground Plane. The lanes should be matched.
2. phyCAM-M interfaces offer 3.3 V or 5 V supply voltages (selected by interface pin 26). Both voltages should be provided by the board to guarantee full compatibility with the phyCAM-M interface.
3. Each phyCAM interface needs a different I^2C address if connected to the same I^2C Bus. Place a Pull-up resistor at pin 24 to select the secondary address.

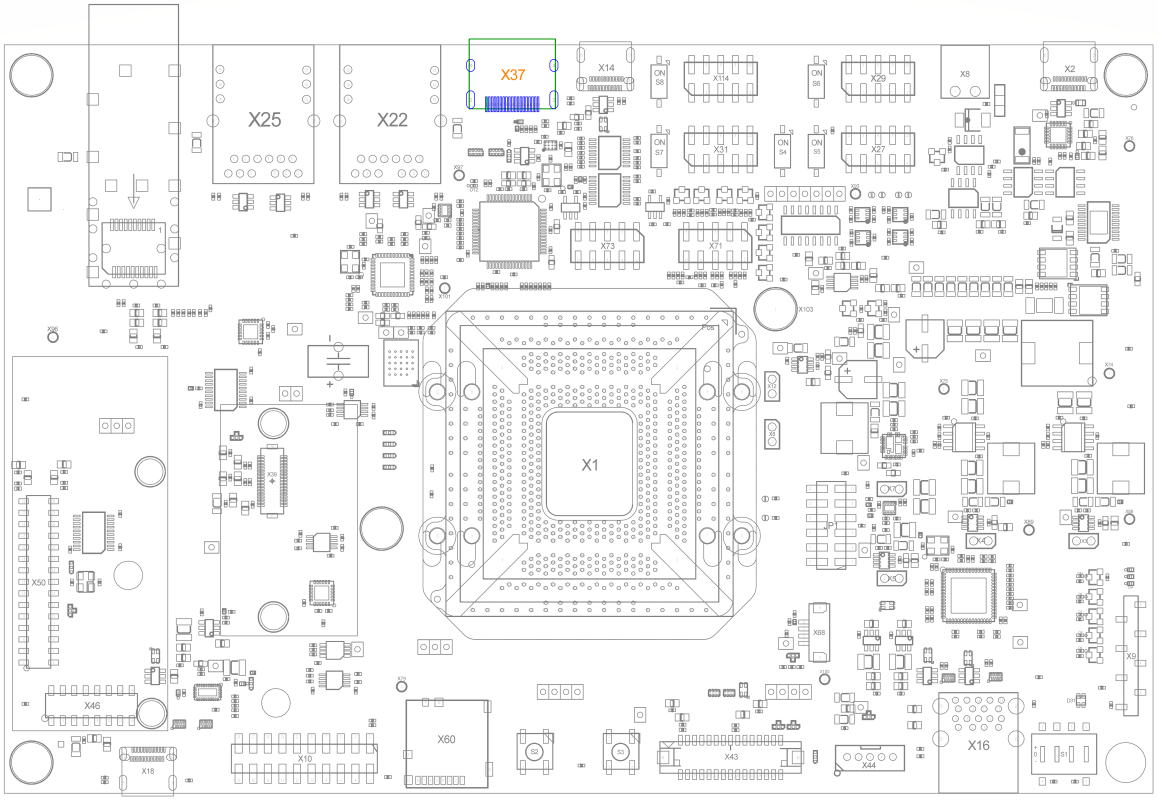
General information and design guidelines for PHYTEC camera interfaces can be found here:

- German: L-867Bd.A9 phyCAM Basis-Spezifikation und Design-In Guide
- English: L-867Be.A9 phyCAM Basis Specification and Design-In Guide

Specific information for each PHYTEC camera module can be found on that module's download page: PHYTEC Embedded Vision (Deutsch) or PHYTEC Embedded Vision (English).

26.3.14 HDMI (X37)

FIGURE 27: HDMI Connector (X37)



The Libra Development Board provides a High-Definition Multimedia Interface (HDMI), which is compliant with HDMI 2.0a. It supports a maximum resolution of 1920x1080p60, 1280x720p60, 720x480p60, and 640x480p60. Please refer to the applicable phyFLEX FPSC SoM Applications Processor Reference Manual for more information. This feature is not available for all mountable FPSC SoMs.

The HDMI interface is brought out at a standard HDMI type A connector (X37) on the Libra Development Board and comprises the following signal groups:

- Three pairs of data signals
- One pair of clock signals
- The Display Data Channel (DDC)
- The Consumer Electronics Control (CEC)
- The Hot Plug Detect (HPD) signal
- Audio Return Channel (ARC)

All signals are routed from the phyFLEX-Connector to the HDMI receptacle through ESD protection diodes and level shifting components.

TABLE 60: X32 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_HDMI_TX2_P	HDMI_O	-	HDMI data 2 positive signal
2	GND	-	0.0 V	Ground
3	X_HDMI_TX2_N	HDMI_O	-	HDMI data 2 negative signal
4	X_HDMI_TX1_P	HDMI_O	-	HDMI data 1 positive signal
5	GND	-	0.0 V	Ground
6	X_HDMI_TX1_N	HDMI_O	-	HDMI data 1 negative signal
7	X_HDMI_TX0_P	HDMI_O	-	HDMI data 0 positive signal
8	GND	-	0.0 V	Ground
9	X_HDMI_TX0_N	HDMI_O	-	HDMI data 0 negative signal
10	X_HDMI_TXC_P	HDMI_O	-	HDMI clock positive signal
11	GND	-	0.0 V	Ground
12	X_HDMI_TXC_N	HDMI_O	-	HDMI clock negative signal

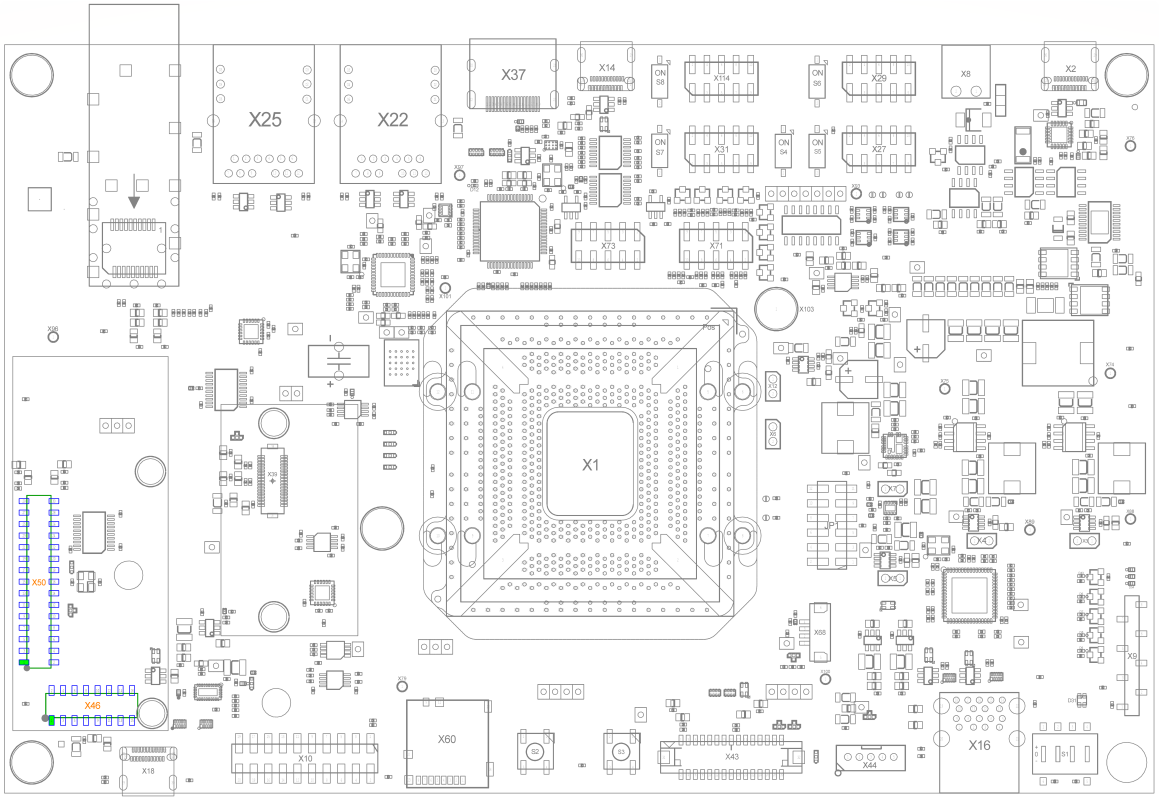
Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_HDMI_CEC	OD-BI-PU	VDD_CEC	Consumer Electronics Control
14	X_EARC_P_UTIL	-	-	Not connected by default, may be connected via resistor jumpers R518 and R519
15	X_HDMI_DDC_SCL	OD-BI-PU	5 V	I2C serial clock
16	X_HDMI_DDC_SDA	OD-BI-PU	5 V	I2C serial data
17	GND	-	0.0 V	Ground
18	VCC_5V_HDMI_OUT	PWR_O	5 V	5 V supply for an HDMI device
19	X_EARC_N_HPD	-	5 V	Audio Return Channel Negative Lane / Hot Plug detect
20	SHIELD_1	-	0.0 V	Shield connected to Ground over 100 nF and 150 pF parallel to 1 MOhm
21	SHIELD_2	-	0.0 V	
22	SHIELD_3	-	0.0 V	
23	SHIELD_4	-	0.0 V	

26.3.14.1 HDMI Design Considerations

The differential impedance should be 100 Ohms for all lanes to a Ground Plane. The lanes should be matched. The DDC lanes need pull-up resistors between 1.5k and 2k to 5V. The CEC lane needs a 27k pull-up resistor connected to 3.3 V through a diode. This prevents leaking current in a power-off state.

26.3.15 Audio/Video (SAI2/LVDS0)

FIGURE 28: Audio/Video Connectors (X46/X50)



The phyFLEX FPSC SoM offers two LVDS display interfaces. The Audio/Video (A/V) connectors X46 and X50 provide an easy way to add typical A/V functions and features to the Libra Development Board. Standard interfaces such as 4-lane LVDS, I2S, I2C, and USB, as well as different supply voltages, are available at the two A/V female pin-sockets. The A/V connector is intended to be used with phyBOARDs and PHYTEC Development Boards to add specific audio/video connectivity with custom expansion boards. A/V connector X46 makes all signals for display connectivity available and provides a supply voltage, while X50 provides signals for audio and touchscreen connectivity as well as an I2C interface, additional control signals and supply voltages. The tables below show the pin assignment of connectors X46 and X50.

TABLE 61: X46 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	-	Ground
2	X_LVDS2_D2_P	LVDS_O	-	LVDS data 2 positive signal
3	X_LVDS2_CLK_P	LVDS_O	-	LVDS clock positive signal
4	X_LVDS2_D2_N	LVDS_O	-	LVDS data 2 negative signal
5	X_LVDS2_CLK_N	LVDS_O	-	LVDS clock negative signal
6	GND	-	-	Ground
7	GND	-	-	Ground
8	X_LVDS2_D3_P	LVDS_O	-	LVDS data 3 positive signal
9	X_LVDS2_D1_P	LVDS_O	-	LVDS data 1 positive signal
10	X_LVDS2_D3_N	LVDS_O	-	LVDS data 3 negative signal
11	X_LVDS2_D1_N	LVDS_O	-	LVDS data 1 negative signal
12	GND	-	-	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	-	Ground
14	X_LVDS2_D0_P	LVDS_O	-	LVDS data 0 positive signal
15	VDD_IN_AV	PWR_O	24 V	A/V power out rail, connected to the carrier board power in
16	X_LVDS2_D0_N	LVDS_O	-	LVDS data 0 negative signal

TABLE 62: X50 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	X_USB_HUB_DN2_P	USB_I/O	-	USB 2.0 Data+
2	X_USB_HUB_DN2_N	USB_I/O	-	USB 2.0 Data-
3	X_nRESET_OUT	OD_O_PU	3.3 V	A/V reset signal
4	GND	-	-	Ground
5	NC	-	-	No connect
6	X_USB_HUB_OVERCUR2	-	3.3 V	USB over current detection
7	X_USB_HUB_nPWRCTL2	-	3.3 V	USB power control
8	X_SAI1_RXFS_3V3	O	3.3 V	A/V Backlight enable
9	X_PWM1_LVDS_DSI_3V3	O	3.3 V	A/V Backlight PWM, choice between 3.3 V, 0 V and shared PWM signal (default) via J30
10	X_nRESET_OUT	OD_O_PU	3.3 V	Global reset output
11	GND	-	-	Ground

Interface Pin #	Signal name	Signal Type	Signal Level	Description
12	NC	-	-	No connect
13	X_SAI1_TXD_3V3	O	3.3 V	SAI TXD
14	GND	-	-	Ground
15	NC	-	-	No connect
16	X_SAI1_TXC_3V3	O	3.3 V	SAI TXC
17	X_SAI1_RXC_3V3	O	3.3 V	SAI RXC
18	X_SAI1_TXFS_3V3	O	3.3 V	SAI TXFS
19	X_MCLK_AV	O	3.3 V	SAI MCLK
20	X_SAI1_RXD_3V3	I	3.3 V	SAI RXD
21	GND	-	-	Ground
22	X_I2C3_SDA_3V3	I/O	3.3 V	I2C3 serial data
23	NC	-	-	No connect

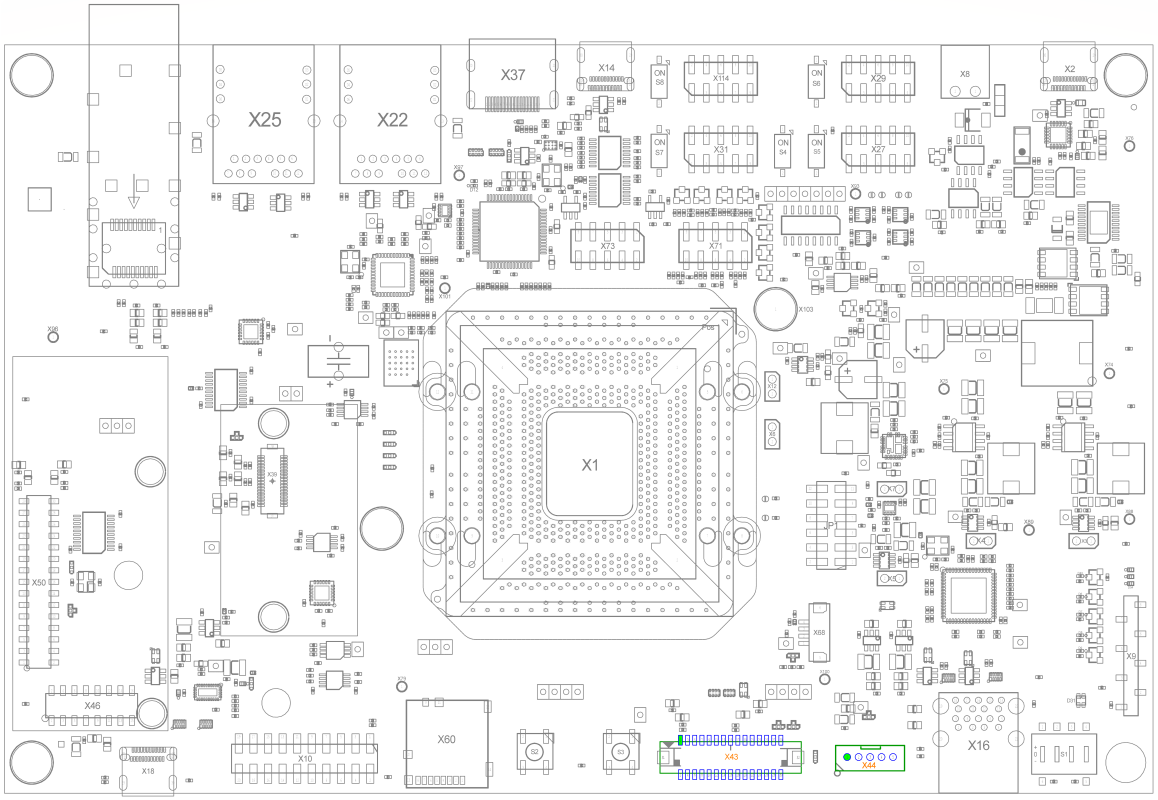
Interface Pin #	Signal name	Signal Type	Signal Level	Description
24	X_I2C3_SCL_3V3	O	3.3 V	I2C3 serial clock
25	NC	-	-	No connect
26	GND	-	-	Ground
27	VDD_5V0	PWR_O	5.0 V	A/V 5.0 V power rail
28	VDD_3V3	PWR_O	3.3 V	A/V 3.3 V power rail
29	VDD_5V0	PWR_O	5.0 V	A/V 5.0 V power rail
30	VDD_3V3	PWR_O	3.3 V	A/V 3.3 V power rail

26.3.15.1 Audio/Video Design Considerations

The differential impedance of LVDS2 lanes should be 100 Ohm and 50 Ohm to a ground plane for all lanes. Lanes should be matched. The audio signals should have a single-ended impedance of 50 Ohms to a ground plane.

26.3.16 LVDS1 (X43/X44)

FIGURE 29: LVDS1 Connectors (X43/X44)



The phyFLEX FPSC SoM offers two LVDS display interfaces. The video connectors X43 and X44 provide an easy way to connect a display to the Libra Development Board. The pinout of both connectors fits the Glyn LVDS Display Family with different display sizes and display resolutions. In addition to the Glyn LVDS signals, there is I^2C for touch brought out at X34 as well. For USB-touch functionality please use the USB Dual Type-A connector X16. The connectors are intended to be used with PHYTEC KLCD-AC163. The tables below show the pin assignment of connectors X43 and X44.

TABLE 63: X43 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	NC	-	-	No connect
2	NC	-	-	No connect
3	VDD_3V3	PWR_O	3.3 V	LVDS1 3.3 V power rail
4	GND	-	0.0 V	Ground
5	X_LVDS1_CLK_N	LVDS_O	-	LVDS clock negative signal
6	X_LVDS1_CLK_P	LVDS_O	-	LVDS clock positive signal
7	VDD_3V3	PWR_O	3.3 V	LVDS1 3.3 V power rail
8	GND	-	0.0 V	Ground
9	X_LVDS1_D0_N	LVDS_O	-	LVDS data 0 negative signal
10	X_LVDS1_D0_P	LVDS_O	-	LVDS data 0 positive signal
11	X_LVDS1_D1_N	LVDS_O	-	LVDS data 1 negative signal
12	X_LVDS1_D1_P	LVDS_O	-	LVDS data 1 positive signal

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	X_LVDS1_D2_N	LVDS_O	-	LVDS data 2 negative signal
14	X_LVDS1_D2_P	LVDS_O	-	LVDS data 2 positive signal
15	X_LVDS1_D3_N	LVDS_O	-	LVDS data 3 negative signal
16	X_LVDS1_D3_P	LVDS_O	-	LVDS data 3 positive signal
17	VDD_5V0	PWR_O	5.0 V	LVDS1 5.0 V power rail
18	GND	-	0.0 V	Ground
19	NC	-	-	No connect
20	NC	-	-	No connect
21	NC	-	-	No connect
22	GND	-	0.0 V	Ground
23	NC	-	-	No connect
24	NC	-	-	No connect

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	NC	-	-	No connect
26	NC	-	-	No connect
27	X_I2C3_SCL_3V3	O	3.3 V	I2C3 serial clock
28	GND	-	0.0 V	Ground
29	X_I2C3_SDA_3V3	I/O	3.3 V	I2C3 serial data
30	NC	-	-	No connect
31	NC	-	-	No connect
32	NC	-	-	No connect

TABLE 64: X44 Pin Assignment

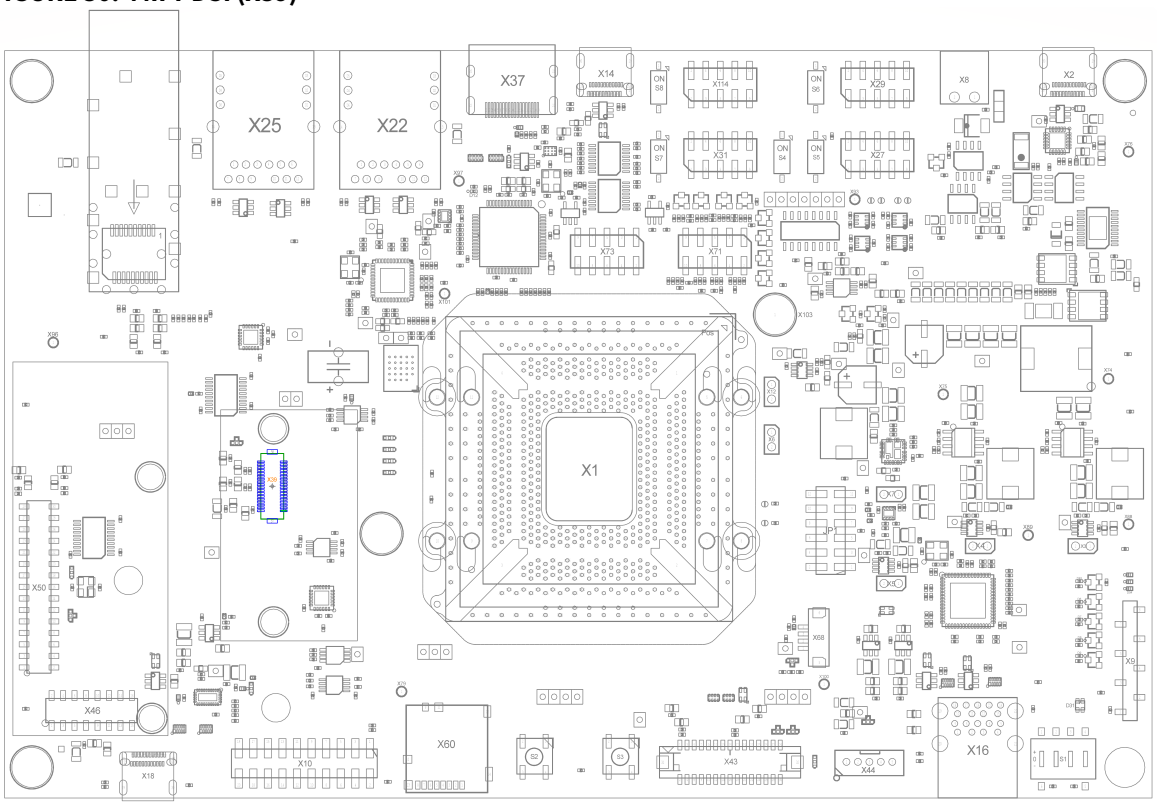
Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	VDD_12V0	PWR_O	12.0 V	LVDS1 12.0 V power rail for backlight
2	X_PWM1_LVDS_DSI_3V3	O	3.3 V	LVDS1 backlight PWM, choice between 3.3 V, 0 V and shared PWM signal (default) via J29
3	GND	-	0.0 V	Ground
4	GND	-	0.0 V	Ground
5	X_LVDS1_BL_EN	O	3.3 V	LVDS1 backlight enable

26.3.16.1 LVDS Design Considerations

The differential impedance of LVDS0 lanes should be 100 Ohm and 50 Ohm to a Ground-Plane for all lanes. The lanes should be matched.

26.3.17 MIPI-DSI (X39)

FIGURE 30: MIPI-DSI (X39)



The Libra Development Board offers one MIPI-DSI display interface. MIPI-DSI has 4 channels, supporting one display with a resolution of up to 1920 x 1080 at 60Hz. The following table shows the pin assignment of connector X39. This feature is not available for all mountable FPSC SoMs.

TABLE 65: X39 Pin Assignment

Interface Pin #	Signal name	Signal Type	Signal Level	Description
1	GND	-	0.0 V	Ground
2	GND	-	0.0 V	Ground
3	X_MIPI_DSI1_D0_P	DSI_O	-	MIPI DSI data 0 positive signal
4	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in
5	X_MIPI_DSI1_D0_N	DSI_O	-	MIPI DSI data 0 negative signal
6	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in
7	GND	-	0.0 V	Ground
8	GND	-	0.0 V	Ground
9	X_MIPI_DSI1_D1_P	DSI_O	-	MIPI DSI data 1 positive signal
10	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in
11	X_MIPI_DSI1_D1_N	DSI_O	-	MIPI DSI data 1 negative signal
12	VDD_IN_MIPI_DSI	PWR_O	24.0 V	MIPI DSI power out rail, connected to the carrier board power in

Interface Pin #	Signal name	Signal Type	Signal Level	Description
13	GND	-	0.0 V	Ground
14	GND	-	0.0 V	Ground
15	X_MIPI_DSI1_CLK_P	DSI_O	-	MIPI DSI clock positive signal
16	VDD_5V0_MIPI_DSI	PWR_O	5.0 V	MIPI DSI 5.0 V power out rail
17	X_MIPI_DSI1_CLK_N	DSI_O	-	MIPI DSI clock negative signal
18	VDD_5V0_MIPI_DSI	PWR_O	5.0 V	MIPI DSI 5.0 V power out rail
19	GND	-	0.0 V	Ground
20	GND	-	0.0 V	Ground
21	X_MIPI_DSI1_D2_P	DSI_O	-	MIPI DSI data 2 positive signal
22	VDD_3V3_MIPI_DSI	PWR_O	3.3 V	MIPI DSI 3.3 V power out rail
23	X_MIPI_DSI1_D2_N	DSI_O	-	MIPI DSI data 2 negative signal
24	VDD_3V3_MIPI_DSI	PWR_O	3.3 V	MIPI DSI 3.3 V power out rail

Interface Pin #	Signal name	Signal Type	Signal Level	Description
25	GND	-	0.0 V	Ground
26	GND	-	0.0 V	Ground
27	X_MIPI_DSI1_D3_P	DSI_O	-	MIPI DSI data 3 positive signal
28	X_I2C4_SCL_3V3	O	3.3 V	I2C4 serial clock
29	X_MIPI_DSI1_D3_N	DSI_O	-	MIPI DSI data 3 negative signal
30	X_I2C4_SDA_3V3	I/O	3.3 V	I2C4 serial data
31	GND	-	0.0 V	Ground
32	GND	-	0.0 V	Ground
33	TP42	-	-	MIPI_DSI1_GPIO0 test point
34	X_PWM1_LVDS_DSI_3V3	O	3.3 V	MIPI DSI1 PWM, choice between 3.3 V, 0 V and shared PWM signal (default) via J31
35	TP43	-	-	MIPI_DSI1_GPIO1 test point
36	X_nRESET_OUT	O	3.3 V	Global reset output

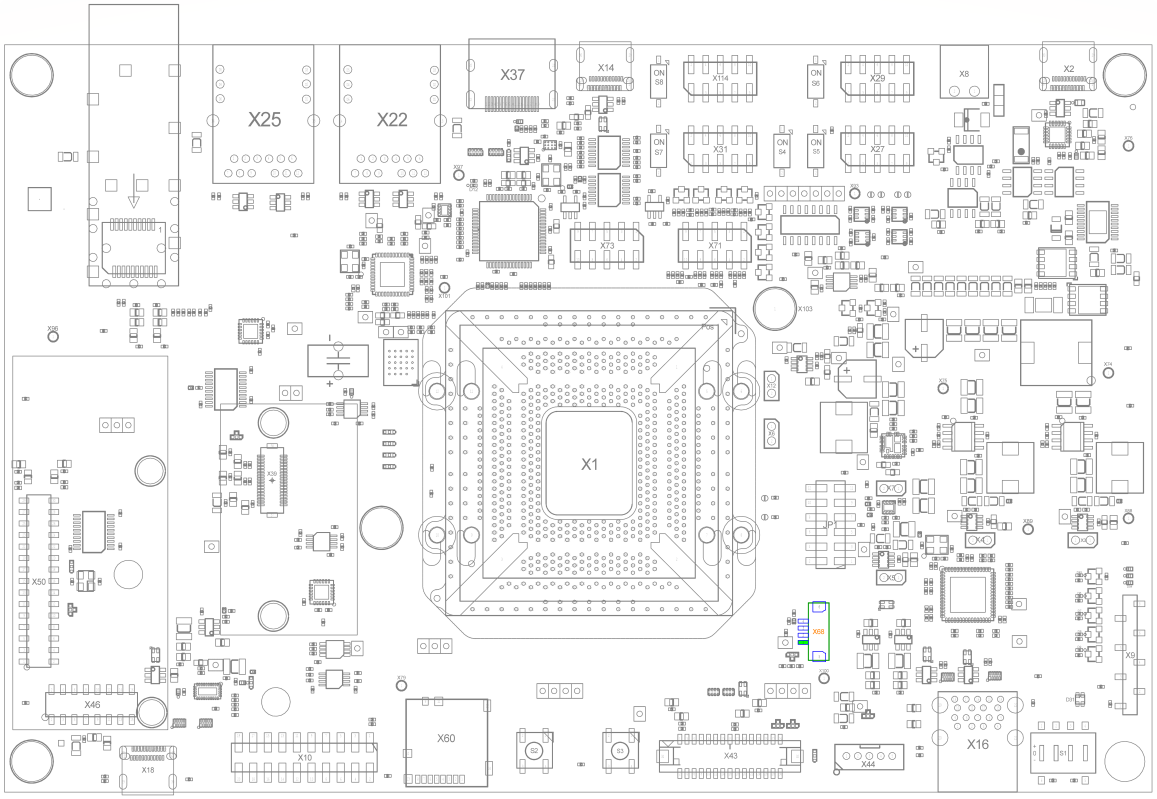
Interface Pin #	Signal name	Signal Type	Signal Level	Description
37	GND	-	0.0 V	Ground
38	GND	-	0.0 V	Ground

26.3.17.1 MIPI-DSI Design Considerations

The differential impedance of MIPI-DSI1 lanes should be 100 Ohm and 50 Ohm to a ground plane for all lanes. The lanes should be matched.

26.3.18 Fan (X68)

FIGURE 31: Fan (X68)



If heatsinking is required for the phyFLEX FPSC SoM, a PWM-controlled fan can be connected to the Libra Development Board. The fan's supply voltage is 5 V by default but can be changed to 12 V or VDD_IN (carrier board input voltage) via J19.The PWM signal is brought out as open drain pulled up to VDD_5V0 with a 4k7 resistor. The fan feedback signal, which can be used to monitor fan rotational frequency, is connected to X_FAN_FB and pulled up to VDD_1V8 via a 4k7 resistor.

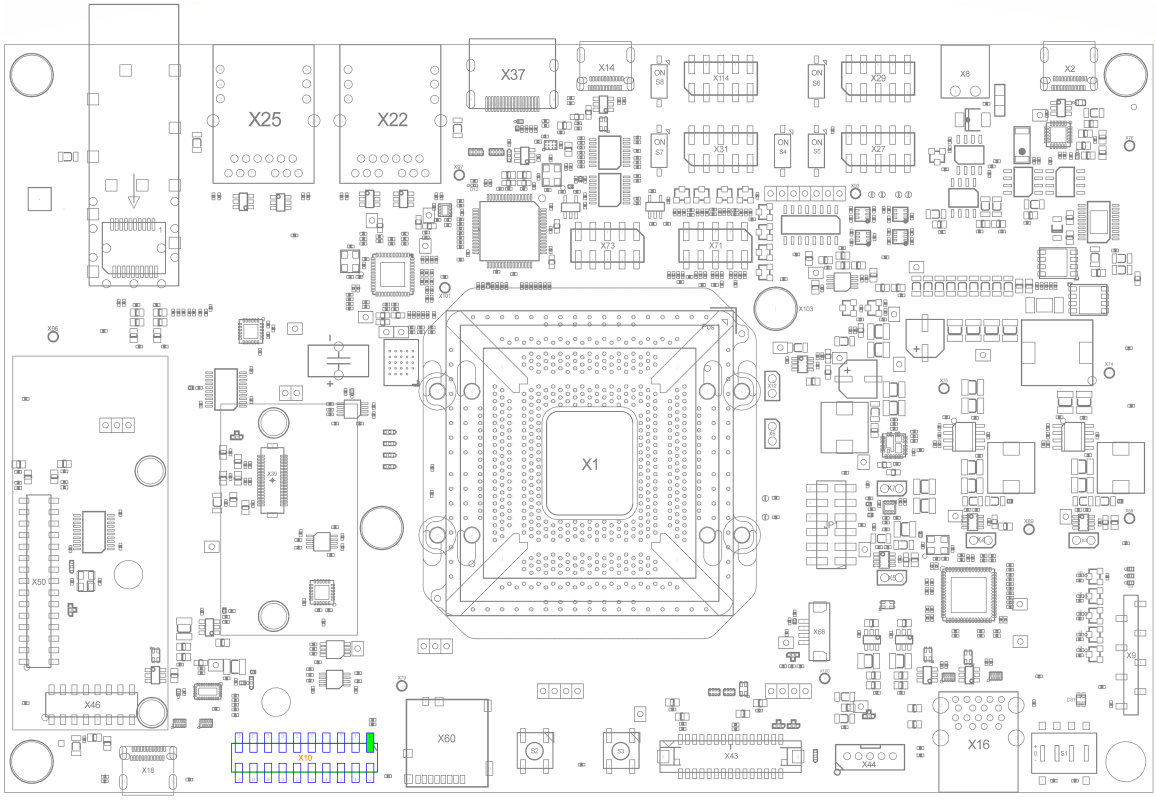
A Hirose DF13-4P-1.25V (75) socket is used as a connector with the following pinout:

TABLE 66: X68 Fan Pinout

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	X_FAN_PWR	PWR_O	5.0 V	FAN power rail, choice to use 12 V or VDD_IN via J19
2	GND	-	0.0 V	Ground
3	X_FAN_FB	I	1.8 V	FAN feedback signal (2 pulses per revolution)
4	X_PWM_FAN	OD_O_PU	5.0 V	Open drain PWM out with pull-up to VDD_5V0
5	Pad1	-	0.0 V	Connected to Ground
6	Pad2	-	0.0 V	Connected to Ground

26.3.19 JTAG (X10)

FIGURE 32: JTAG (X10)



The Libra Development Board provides a 2x10 2.54mm pin-header for JTAG connectivity. 1.8 V are available at the connector directly or with a 100R pull-up.

The JTAG connector X10 has the following pinout:

TABLE 67: X10 JTAG Connector Pinout

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	Pull-up VDD_1V8	PWR_O	1.8 V	100 Ω pull-up to 1.8 V power rail
2	VDD_1V8	PWR_O	1.8 V	1.8 V power rail
3	X_JTAG_TRST	I	1.8 V	Reset in signal
4	GND	-	0.0 V	Ground
5	X_JTAG_TDI	I	1.8 V	JTAG TDI
6	GND	-	0.0 V	Ground
7	X_JTAG_TMS	I	1.8 V	JTAG TMS
8	GND	-	0.0 V	Ground
9	X_JTAG_TCK	I	1.8 V	JTAG TCK
10	GND	-	0.0 V	Ground
11	X_JTAG_RTCK	I	1.8 V	JTAG Return Clock, no connect
12	GND	-	0.0 V	Ground

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
13	X_JTAG_TDO	O	1.8 V	JTAG TDO
14	GND	-	0.0 V	Ground
15	X_nRESET_IN	I	1.8 V	Reset in signal
16	GND	-	0.0 V	Ground
17	NC	-	-	No connect
18	GND	-	0.0 V	Ground
19	NC	-	-	No connect
20	GND	-	0.0 V	Ground

26.3.20 On-board Functionalities

26.3.20.1 Multicolor (RGB) LED (D31)

The Libra Development Board provides one multicolor (RGB) LED (D31). The LED is connected to an LED driver PCA9633TK controlled by the I2C3 bus. The location for D31 can be found in LEDs.

26.3.20.2 Factory EEPROM (U57)

The Libra Development Board provides a 2 kbit EEPROM (ST M24C02-RMC6TG) for factory data. It is connected to the I2C3 bus. The EEPROM's write protection pin is connected to TP60. Write protection can be enabled by mounting R333 (10k) pull-up resistor. In this case, the EEPROM can be written if TP60 is tied to Ground only. The EEPROM I^2C address can be fully customized by jumpers J21, 22, and 23. The default address is 0x51.

26.3.20.3 User EEPROM (U80)

The Libra Development Board provides a 2 kbit EEPROM (ST M24C02-RMC6TG) for general use. It is connected to the I2C3 bus. The EEPROM's write protection pin is connected to TP112. Write protection can be enabled by mounting R486 (10k) pull-up resistor. In this case, the EEPROM can be written if TP112 is tied to Ground only. The EEPROM I^2C address can be fully customized by jumpers J21, 22, and 23. The default address is 0x52.

26.3.20.4 Quad SPI NOR (U62)

The Libra Development Board features a 512MBit Quad SPI NOR at U62.

26.3.20.5 ADC (X73)

The Libra Development Board features 8 analog to digital channels depending on the mounted phyFLEX SOM. The inputs are used to measure carrier board voltages and currents. Maximum input voltage is 1.8 V. All input signals are available at 2.54mm pin-header X73 with the following pinout:

TABLE 68: X73 ADC

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VDD_1V8	PWR_O	1.8 V	1.8 V power rail
2	GND	-	0.0 V	Ground
3	ADC_AIN0	I	0.0 - 1.8 V	Analog input channel 0 - used for VDD_SOM current
4	ADC_AIN1	I	0.0 - 1.8 V	Analog input channel 1 - used for VDD_SOM voltage
5	ADC_AIN2	I	0.0 - 1.8 V	Analog input channel 2 - used for VDD_5V0 current
6	ADC_AIN3	I	0.0 - 1.8 V	Analog input channel 3 - used for VDD_5V0 voltage
7	ADC_AIN4	I	0.0 - 1.8 V	Analog input channel 4 - used for VDD_3V3 current
8	ADC_AIN5	I	0.0 - 1.8 V	Analog input channel 5 - used for VDD_3V3 voltage
9	ADC_AIN6	I	0.0 - 1.8 V	Analog input channel 6 - used for VDD_1V8 current
10	ADC_AIN7	I	0.0 - 1.8 V	Analog input channel 7 - used for VDD_1V8 voltage

26.3.20.6 SPI ADC (X71)

The Libra Development Board comes with an SPI-ADC U61 (MCP3208-BI/SL) with 8 channels, which are connected to carrier board current and voltage measurement devices. This SPI-ADC serves as a comparison betwenn itself and the on-board ADC, which is available depending on the mounted phyFLEX SOM. The SPI-ADCs maximum voltage is 5.0 V and the conversion method is SAR with a depth of 12 Bit. The SPI-ADC is connected to the SPI1 interface. The following table shows the pinout of pin-header X71 where all SPI-ADC input signals are available.

TABLE 69: X71 SPI-ADC

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VDD_5V0_REF	PWR_O	5.0 V	5.0 V reference voltage derived from precision voltage reference U78
2	GND	-	0.0 V	Ground
3	SPI_ADC_AIN0	I	0.0 - 5.0 V	Analog input channel 0 - used for VDD_SOM current
4	SPI_ADC_AIN1	I	0.0 - 5.0 V	Analog input channel 1 - used for VDD_SOM voltage
5	SPI_ADC_AIN2	I	0.0 - 5.0 V	Analog input channel 2 - used for VDD_5V0 current
6	SPI_ADC_AIN3	I	0.0 - 5.0 V	Analog input channel 3 - used for VDD_5V0 voltage
7	SPI_ADC_AIN4	I	0.0 - 5.0 V	Analog input channel 4 - used for VDD_3V3 current
8	SPI_ADC_AIN5	I	0.0 - 5.0 V	Analog input channel 5 - used for VDD_3V3 voltage
9	SPI_ADC_AIN6	I	0.0 - 5.0 V	Analog input channel 6 - used for VDD_1V8 current
10	SPI_ADC_AIN7	I	0.0 - 5.0 V	Analog input channel 7 - used for VDD_1V8 voltage

26.3.20.7 Temperature sensor (U56)

The Libra Development Board is equipped with a P3T1750DPZ I3C temperature sensor connected to I2C5. I2C address is 0x4F, I3C provisional ID is 0x9E.

26.3.20.8 TPM (U79)

The Libra Development Board features a Trusted Platform Module SLB9670. It is connected to SPI2 and offers TPM 2.0 functionality.

26.3.20.9 Peripheral current measurement (U5/U7/U9)

The Libra Development Board is equipped with current sensing devices which translate the momentary current load through a measurement resistor into a voltage value. This voltage value then can be interpreted by the phyFLEX SOM on-board ADC or the carrier board SPI-ADC or both at the same time. The current measurement ICs used are INA241A4QDDFRQ1 with a 0.004R 1% shunt resistor. The applicable gain factor is 100V/V. Which current measurement IC is connected to which ADC channel can be obtained from the section of the applicable ADC in this manual.

26.3.20.10 Global Board Reset (X_nRESET_OUT)

The X_nRESET_OUT signal (X_POR_B at phyFLEX FPSC SoM) is used to hold all devices with an external reset pin in the reset state. X_nRESET_OUT will be released after all board voltages are powered up and allows the phyFLEX FPSC SoM to boot. X_nRESET_OUT is brought out at several connectors.

X_nRESET_OUT Design Considerations

Note that there is a 10 kOhms pull-up resistor on the phyFLEX FPSC SoM VDD_IO voltage. It is recommended to use this signal as an open drain.

26.3.20.11 On-board Power Supplies

The Libra Development Board provides supply voltages on several connectors to power external devices. Be sure not to exceed the maximum permissible current that can be drawn from each power domain. In the table below, each source is listed with the location where a voltage connected to the source can be found:

TABLE 70: Onboard Power Supplies

Voltage Domain	Locations	Max. recommended additional current
VDD_IN	TP1, X39(VDD_IN_MIPI), X46(VDD_IN_AV), X117	Depends on used input power supply connected to the carrier board
VDD_12V0	TP3, X44(VDD_12V0_LVDS1), X117	TBD
VDD_SOM	TP4	TBD

Voltage Domain	Locations	Max. recommended additional current
VDD_5V0	TP6, X39(VDD_5V0_MIPI_DSI), X43(VDD_5V0_LVDS1), X50(VDD_5V0_AV), X117	TBD
VDD_3V3	TP7, X39(VDD_3V3_MIPI_DSI), X43(VDD_3V3_LVDS1), X50(VDD_3V3_AV), X52, X54, X114	TBD
VDD_3V3_OUT	X6	200 mA
VDD_1V8	TP8, X9, X10, X114	200 mA (derived from VDD_1V8_OUT, currents from both cannot exceed 200 mA cumulatively)
VDD_1V8_OUT	X7	200 mA

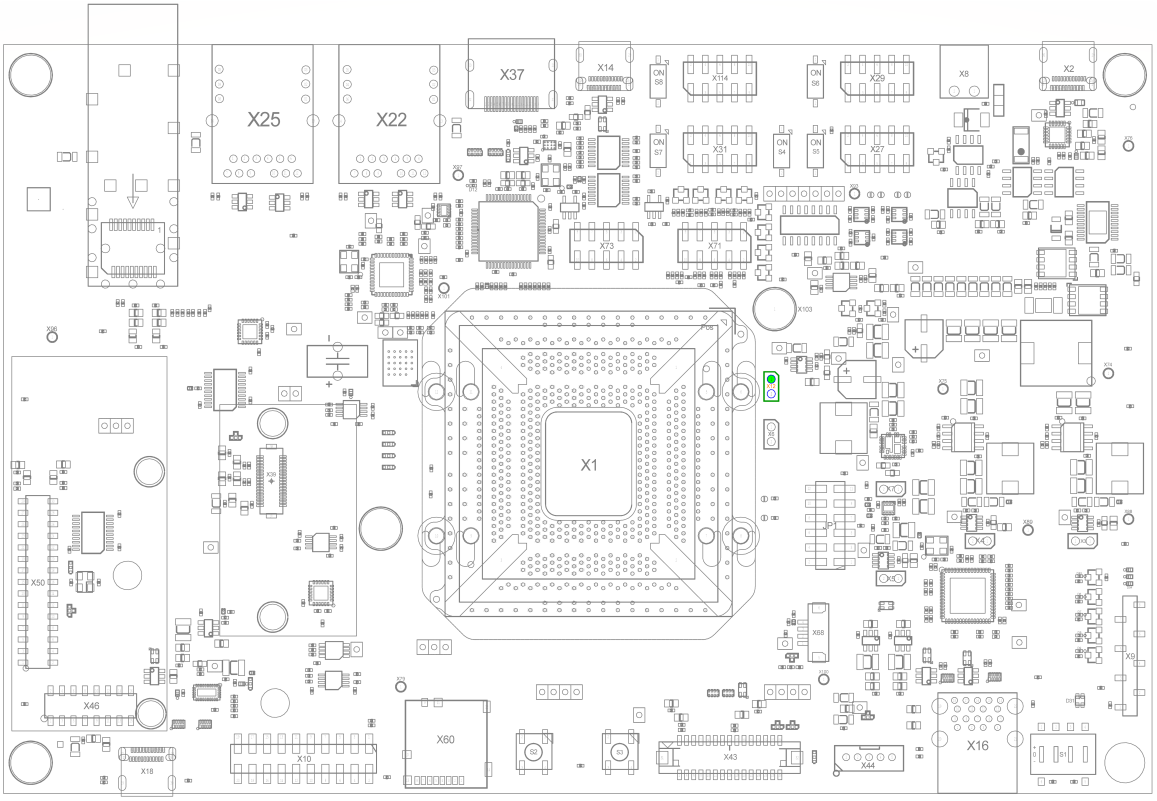
In addition to these currents, Libra Development Board delivers current for USB_VBUS of X16/X18 (3x 900 mA), phyCAM-M Interfaces (2x 1500 mA 3.3 V or 5 V depending on VCC_SELECT pin), HDMI connector (150 mA).

Warning

Drawing current may result in heating of the voltage regulator components and might require additional heat sinking.

26.3.20.12 On-board Measurement of SoM Power Consumption

FIGURE 33: SoM Input Current Amp Header (X12)



The input current of the SoM supply rail VDD_SOM can be measured on board to determine the power consumption of the SOM. A current sense amplifier translates the supply current into a proportional voltage VOUT_CC_SOM, which can be measured at X12 (on PCB top side) and X12 (on PCB bottom side). The mounted amplifier features a gain of 100V/V. The SoM input current I_{SOM_IN} in Ampere is determined by inserting VOUT_CC_SOM into the following equation.

Subsequently, the SoM input power may be derived from I_{SOM_IN} and VOUT_CC_SOM using the following formula:

For example, measuring 400 mV at X12, the input current will be 1 A. With a SoM input voltage of 5.0 V, the input P_{SOM_IN} is 5 W.

26.3.21 Switches

The Libra Development Board has several switches and buttons for various uses. The locations for all switches can be found in Switches and Buttons.

26.3.21.1 System Reset Button (S2)

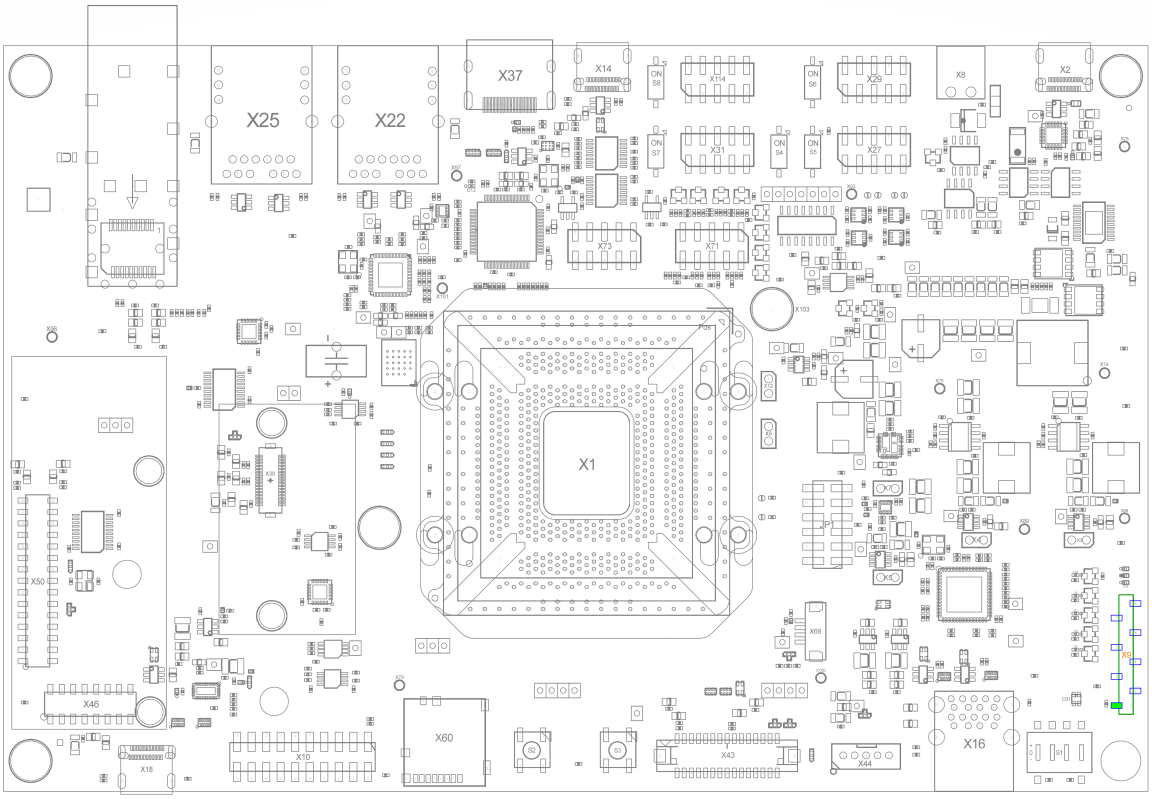
The Libra Development Board is equipped with a system reset button at S2. Pressing this button will assert reset through a voltage supervisor U11 that will pull the X_nRESET_IN pin (X1 Pin Y21) of the phyFLEX FPSC SoM low, causing the module to reset with a complete power cycle.

26.3.21.2 System ON/OFF Button (S3)

The Libra Development Board is equipped with an ON/OFF button at S3 and is connected to X_ONOFF of the phyFLEX FPSC SoM. For more information, refer to the applicable CPU's *Reference Manual*.

26.3.21.3 Boot Switch (S1)

FIGURE 34: Boot Header (X9)



The Libra Development Board features a tri-state boot switch with four individually switchable ports to select the phyFLEX FPSC SoM default bootsource. The Boot_Mode signals may also be accessed through pin header X9 or USB to UART/GPIO converter U15. Descriptions of the various boot modes can be found in Boot Mode Selection. The available boot options differ depending on the mounted phyFLEX SoM. All available options are displayed in the

table below. Default boot modes are marked red, the phyFLEX SOM will boot default when no boot mode alteration is engaged:

Boot Mode designation	
1	High
0	Low
X	Don't care
Boot Switch designation	
1	Pull-up
0	Pull-down
-	Middle setting, open

TABLE 71: Boot Configuration Options (S1)

Mounted SoM	**Boot Target**	**Memory/TargetLocation**	**BOOT_MODE**				**S1 Switch Number**			
			3	**2**	**1**	**0**	**4**	**3**	**2**	**1**
PFL-G-01 (FPSC phyFLEX-i.MX 8MP)	**eMMC (SoM default)**	SOM	0	0	1	0	-	-	-	-

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
	SD-Card	CarrierBoard	0	0	1	1	-	-	-	1
	QSPI NOR	CarrierBoard	0	1	1	0	-	1	-	-
	USB1 serial downloader	SOM	0	0	0	1	-	-	0	1
	Fuse boot	SOM	0	0	0	0	-	-	0	-
	JTAG mode	SOM	1	1	1	1	1	1	-	1

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
PFL-G-02 (FPSC phyFLEX-i.MX 95)	**eMMC (SoM default)**	SOM	1	0	1	0	-	-	-	-
	SD-Card	CarrierBoard	1	0	1	1	-	-	-	1
	QSPI NOR	CarrierBoard	1	1	0	0	-	1	0	-
	USB1 serial downloader	SOM	1	0	0	1	-	-	0	1
	Fuse boot	SOM	1	0	0	0	-	-	0	-

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
PFL-G-03 (FPSC phyFLEX-AM62L)	**MMC0 eMMC FS (SOM default)**	SOM	1	0	1	1	-	-	-	-
	USB0 Host MSC	SOM	0	1	1	1	0	1	-	-
	MMC0 eMMC FS	SOM	1	0	0	0	-	-	0	0
	FSS0 QSPI CS0	CarrierBoard	1	0	0	1	-	-	0	-
	MMC1 4b UDA FS	SOM	1	0	1	1	-	-	-	-
	DEVBOOT	SOM	0	1	1	0	0	1	-	0

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
	FSS0 Serial NAND		1	1	0	0	-	1	0	0
	FSS0 xSPI SFDP		1	1	0	1	-	1	0	-
	EXT. HOST UART0		1	1	1	0	-	1	-	0
	EXT. HOST USB0 DFU		1	1	1	1	-	1	-	-
PFL-G-04 (FPSC phyFLEX-STM32MP2)	**eMMC (SoM default)**	SOM	0	0	1	0	-	-	-	-
	UART and USB	SOM	0	0	0	0	-	-	0	-
	SD-Card	CarrierBoard	0	0	0	1	-	-	0	1

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
	Development	SOM	0	0	1	1	-	-	-	1
	QSPI NOR	CarrierBoard	0	1	0	0	-	1	0	-
PFL-G-05 (FPSC phyFLEX-i.MX 93) A55 boot	**eMMC (SoM default)**	SOM	0	0	1	0	-	-	-	-
	USB1 serial downloader	SOM	0	0	0	1	0	-	0	1
	Fuse boot	SOM	X	0	0	0	-	-	0	-

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
	SD-Card	CarrierBoard	0	0	1	1	0	-	-	1
	QSPI NOR	CarrierBoard	0	1	0	0	0	1	0	-

Mounted SoM	Boot Target	Memory/TargetLocation	BOOT_MODE				S1 Switch Number			
			3	2	1	0	4	3	2	1
PFL-G-05 (FPSC phyFLEX-i.MX 93) M33 boot	eMMC	SOM	1	0	1	0	1	-	-	-
	USB1 serial downloader	SOM	1	0	0	1	1	-	0	1
	Fuse boot	SOM	X	0	0	0	-	-	0	-
	SD-Card	CarrierBoard	1	0	1	1	1	-	-	1
	QSPI NOR	CarrierBoard	1	1	0	0	1	1	0	-

TABLE 72: Boot Mode Configuration Header Pinout (X9)

Interface Pin #	Signal Name	Signal Type	Signal Level	Description
1	VDD_1V8	PWR_O	1.8 V	1.8 V power rail
2	X_BOOT_MODE0	I	1.8 V	Boot mode 0 configuration signal
3	X_BOOT_MODE1	I	1.8 V	Boot mode 1 configuration signal
4	X_BOOT_MODE2	I	1.8 V	Boot mode 2 configuration signal
5	X_BOOT_MODE3	I	1.8 V	Boot mode 3 configuration signal
6	X_nRESET_IN	I	1.8 V	Reset in signal
7	NC	-	-	No connect
8	GND	-	0.0 V	Ground

Boot Mode Design Considerations

Bootpin voltages should be valid when X_POR_B (X_nRESET_IN at Libra Development Board) is released.

27 Additional System-Level Hardware Information

27.1 I2C Connectivity

The I2C1 interface of the phyFLEX FPSC SoM is not connected to the Libra Development Board. The table below lists the connectors and pins with I2C connectivity and on-board devices. The I²C addresses are hexadecimal in 7-bit representation of the default Linux representation.

TABLE 73: I2C2 Connectivity

I2C2 Interface	Location and/or Address
STUSB4500QTR	U1 - 0x28
M.2 Key-M	X54
Factory EEPROM	U57 - 0x51
User EEPROM	U80 - 0x52
TCAL6416RTW	U58 - 0x21
phyCAM-M CSI2 VM-016	X34 - 0x18, 0x57
phyCAM-M CSI2 VM-017	X34 - 0x37, 0x57
phyCAM-M CSI2 VM-020	X34 - 0x18, 0x57
MIPI-DSI / PEB-AV-12	X39 - 0x10, 0x24, 0x2C, 0xeE

TABLE 74: I2C3 Connectivity

I2C3 Interface	Location or Address
TUSB8042A	U21 - 0x44
phyCAM-M CSI1 VM-016	X32 - 0x10, 0x56
phyCAM-M CSI1 VM-017	X32 - 0x36, 0x56
phyCAM-M CSI1 VM-020	X32 - 0x10, 0x56
LVDS1 Connector	X43; connecting jumpers are not mounted by default
M.2 Key-E	X52

I2C3 Interface	Location or Address
PCA9533/01	U55 - 0x62
TCAL6416RTW	U72 - 0x21
HD3SS3220I	U66 - 0x47
PEB-AV-10 LVDS2	X50 - 0x18, 0x57, 0x5F
PEB-AV-13 LVDS2	X50 - 0x34

TABLE 75: I2C4 Connectivity

I2C4 Interface	Location or Address
SFP+	X113 - 0xA0, 0xA2

TABLE 76: I2C5 Connectivity

I2C5 Interface	Location or Address
P3T1750DPZ I2C	U56 - 0x4F
P3T1750DPZ I3C	U56 - 0x9E

To avoid conflicts when connecting external I2C devices to the Libra Development Board, the addresses of the onboard I2C devices must be considered. The table below lists the addresses already in use; the default address is printed in bold. The I²C addresses are hexadecimal in 7-bit representation, which is the default Linux representation.

TABLE 77: Reserved I2C Addresses

Bus	Connector	Prod. No.	Addresses
I2C3	phyCAM-M CSI1 Connector X32	VM-016-xxx-M	**0x10**, 0x18
		VM-017-xxx-M	**0x36**, 0x37
		VM-117-xxx-M	**0x36**, 0x37
		VM-017-xxx-L	**0x36**, 0x37, **0x18**
		VZ-018	**0x3D**, 0x38
I2C4	phyCAM-M CSI1 Connector X34	VM-016-xxx-M	**0x10**, 0x18
		VM-017-xxx-M	**0x36**, 0x37

Bus	Connector	Prod. No.	Addresses
		VM-117-xxx-M	**0x36**, 0x37
		VM-017-xxx-L	**0x36**, 0x37, **0x18**
		VZ-018	**0x3D**, 0x38

The Libra Development Board

28 Revision History

TABLE 78: Revision History

Date	Version #	Changes in this manual
03.02.2026	L-1089e.A0	Preliminary Manual Describes the phyFLEX-i.MX 91/93 FPSC SOM Version: 1634.0 PCB Version: 1618.2

29 Contact Information

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