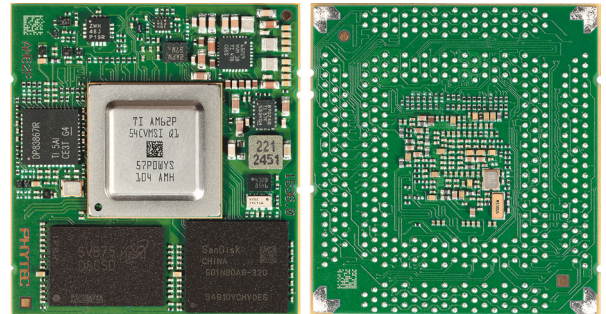


phyFLEX®-AM62Px FPSC

The phyFLEX-AM62Px module expands Phytect's phyFLEX product family with the powerful AM62P processor from the Texas Instruments Sitara series. This processor combines high computing power, efficient power management, and advanced graphics capabilities. Thanks to its standardized FPSC pinout, the module is compatible with other phyFLEX systems, ensuring long-term scalability and future-proofing for embedded applications.

Compared to the AM62L processor, the AM62P boasts significantly improved graphics and multimedia performance. While the AM62L is optimized for simple visualizations and cost-sensitive designs, the AM62P, thanks to its 2D/3D GPU, video acceleration, and multi-core architecture, offers enormous flexibility for 3D HMI, graphics-intensive user interfaces, and video streaming applications. With up to four Arm Cortex-A53 cores and versatile industrial interfaces—2 x 1 Gbit Ethernet (TSN), 3 x CAN-FD, and 2 x USB 2.0—the phyFLEX-AM62P is ideally equipped for high-performance, networked embedded systems.



AM62Px Processor

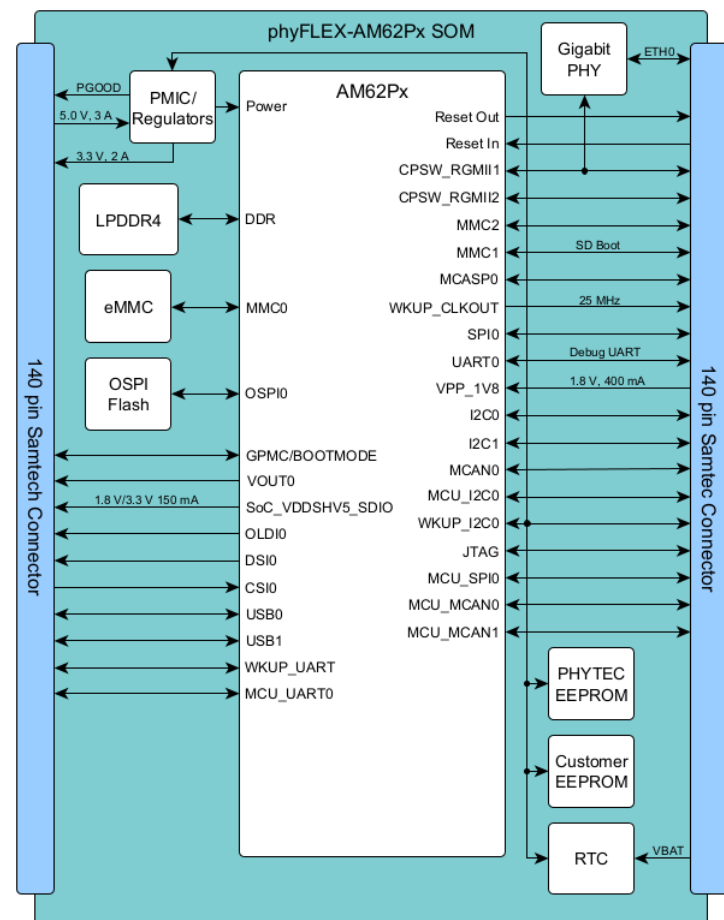
- Scalable performance with 4x Arm Cortex-A53 (1.4GHz)
- 2x Arm Cortex-R5F (800 MHz)
- 2D/3D GPU with up to 50 GFLOPS
- 3x display interfaces: MIPI, DPI, LVDS
- Security features: Secure boot, HSH Support, TEE support and Arm TrustZone®

Module Features

- Up to 256 GB TLC eMMC and up to 8 GB LPDDR4
- On-board Ethernet PHY and voltage conversion
- Low power consumption
- FPSC Gamma 1.1 footprint allowing scalable applications with other FPSC SoMs (e.g. phyFLEX-AM62Lx)
- Dimensions 35 mm x 50 mm, low profile

Your Advantages

- Ready adapted Linux® operating system
- Only one device design for different performance configurations
- Product Life-Cycle Management program
- Global Technical Support



Technical Data

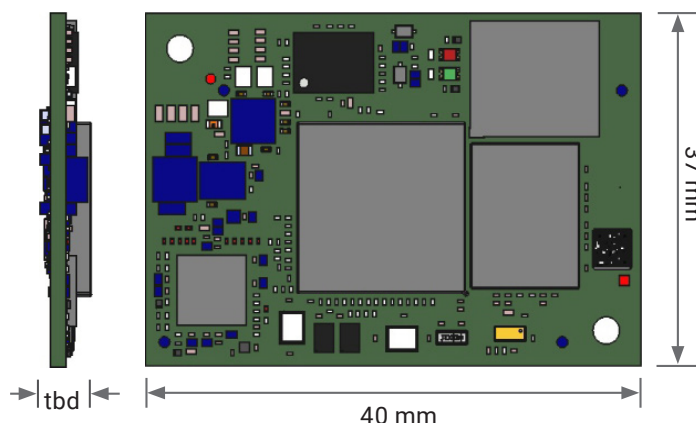
Module Configuration

SOC	
Processor	TI AM62P54, AM62P52, AM62P34, AM62P32
Core(s)	Dual- or quad-core Arm Cortex-A53
Additional core(s)	2x Arm Cortex-R5F, (1x user, 1x device mngmt.)
Clock frequency	up to 1.4 GHz (A53), up to 800 MHz (R5F)
L2 Cache	512 kB shared with ECC
GPU	3D GPU (1 shader, 50 GFLOPS, OpenGL/Vulkan)
Video processing	4K UHD H.265 decode and encode
Cryptogr. acceleration	AES, SHA-2, DRBG, PKA
HW Security	Secure boot, TrustZone
Functional Safety	up to SIL 2 targeted Systematic capability: up to SIL 3
MEMORY	
eMMC	4 GB up to 256 GB
LPDDR4	1 GB up to 8 GB
EEPROM	4 kB up to 32 kB
PHYSICAL PROPERTIES	
Dimensions	40 mm x 37 mm
Weight	tbd.
Operating temperature	-40 °C to +85 °C
Humidity	95 % rF non condensing
Operating voltage	5.0 V
Power consumption typ.	tbd.
PCB connection	Fused Tin Grid Array (FTGA) (1.27 mm pitch)
SOFTWARE	
Operating system	Linux (Yocto based)

Module Interfaces

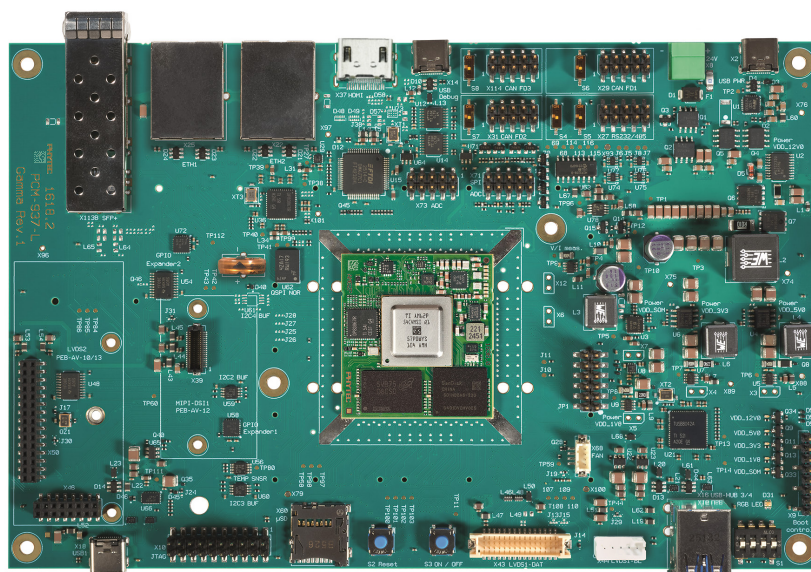
MAXIMUM INTERFACES*,**	
Ethernet	2x GbE (1x on-board PHY or RGMII/ 1x RGMII. all TSN)
USB	2x 2.0 Dual Role
UART	3x, up to 9x ¹
CAN	3x (CAN FD)
I ² C	5x, up to 6x ¹
SPI	3x (+1x QSPI), up to 4x (+1x QSPI) ¹
ePWM,	up to 4x
eCAP	up to 3x ¹
MMC/SD/SDIO	2x
Display	1/2x LVDS 8/4-lane (up to 1080p or 1920x1200 or 2x720p), 1x MIPI DSI D-PHY 1.2 (4kp30 or 3840 x 1440p60), DPI (24-bit) ¹
Audio	1x McASP, up to 3x McASP ¹
Camera	1x, up to MIPI CSI ¹
Debugging	JTAG, UART
RTC	1x on-chip, 1x on-board external on-chip, 1x on-board 1x AM62L on-chip 1 on-board

¹ Indicates the maximum number or additional interfaces when pin compatibility according to the FPSC standard is NOT required



Libra Development Board FPSC

Versatile Development Platform for FPSC Modules



INTERFACES

Ethernet	2x 1 GbE (all RJ45) (TSN support)
USB	1x USB 2.0 (Type-A), 1x USB 2.0 (Type-C)
Serial	1x RS-232 or RS-485, 2x CAN FD (3x pin header 2x5)
Display	1x LVDS
Debugging	JTAG (Expansion sockets) 1x USB 2.0 Debug (Type-C)
Various	I ² C, SPI, GPIO, ADC (Expansion connectors)

MISCELLANEOUS

MMC/SD/SDIO	microSD Card Slot
User Control	3x LED, 1x RGB LED, 2x button
Dimensions	230 mm x 140 mm
Supply Voltage	24 V or USB-C