Compatibility Guide - PCL-063 (phyCORE-i.MX 6UL/ULL) and PCL-077 (phyCORE-i.MX 91/93) (LAN-114e.A0)

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Introduction

The purpose of this guide is to show how to migrate between the phyCORE-i.MX 6UL/ULL to phyCORE-i.MX 91/93 in your applications. In this guide, we highlight the necessary parameters, signals, and power consumption to ensure a smooth migration between the two SoMs.

Overview

The two SOMs, phyCORE-i.MX 6UL/ULL and phyCORE-i.MX 91/93, are mechanically footprint-compatible. They can be substituted for each other if certain electrical parameters are met. This document is intended to guide you through a carrier board design, that will accommodate either the phyCORE-i.MX 6UL/ULL or the phyCORE-i.MX 91/93.

One of these parameters is the IO level of the externally routed GPIOs, which leads to the compatibility mode.

Compatibility mode describes the configuration of the phyCORE-i.MX 91/93 and is required to replace a phyCORE-i.MX 6UL/ULL with a phyCORE-i.MX 91/93. However, the IO-level configuration alone is not sufficient to ensure that the systems can be replaced. Further measures, which are described in this document, are required.

When designing cross-SOM hardware, several physical parameters must be taken into account. One of these parameters is the different power consumption of the two phyCORE modules, which require different measures in terms of power supply, voltage supply, and heat dissipation. Another aspect to consider is the mechanical parameters of the two footprint-compatible SOMs. This includes the contour of the SOM surface when using heat spreaders and the electrical behavior in the EMC chamber.

Warning

This document must not be used alone for the development of a carrier board or other SOM-compatible hardware, as it is only a subordinate description of the two SOM systems. In particular, the hardware manual for the respective phyCORE SOM and the datasheet for the respective processor, i.MX 6UL/ULL and i.MX 91/93, must be consulted for the development of SOM-compatible hardware.
phyCORE-i.MX 6UL/ULL: Hardware Manual - phyBOARD-i.MX 6UL/ULL (L-827e.A3)
phyCORE-i.MX 91/93: Hardware Manual - phyCORE-i.MX 91/93/phyBOARD-Segin (1607.1/1472.5) (L-1058e.A2)

Compatibility Mode

For the phyCORE-i.MX 91/93 to be interchangeable with the phyCORE-i.MX 6UL/ULL, the phyCORE-i.MX 91/93 needs to be ordered by customers in what we call "Compatibility Mode". When in "Compatibility Mode", most signals of the phyCORE-i.MX 91/93 will be compatible with the signals of the i.MX 6UL, having for example the same voltage.

To make use of phyCORE-i.MX 91/93 interfaces and features, which are not compatible with phyCORE-i.MX 6UL/ULL, the phyCORE-i.MX 91/93 can also be ordered in what we call "Full Feature Mode". This mode will bring additional features like a GBit Ethernet and High Speed SD Card Interface but it will also break most of the compatibility to phyCORE-i.MX 6UL/ULL.

The table below will show the differences between phyCORE-i.MX 6UL/ULL (PCL-063) and phyCORE-i.MX 91/93 (PCL-077) in either Compatibility or Full Feature Mode. The different voltages of the interfaces are resembled by the different font colors. The table will also show the major differences in internal processor features and interfaces of the phyCORE-i.MX 6UL/ULL (PCL-063) and phyCORE-i.MX 91/93 (PCL-077).

1 i.MX 6UL/ULL - i.MX 91/93 Overview

Signal Voltage Legend
dynamic 1,8V / 3,3V
1,8V
3,3V

i.MX 6UL/ULL Default Feature	i.MX 91 Compatibility Mode	i.MX 93 Compatibility Mode	i.MX 91 Full Feature Mode	i.MX 93 Full Feature Mode
	J13, J14 = 1+2 (3.3 V IO voltage)		**J13, J14 = 2+3 (1.8 V IO voltage)**	
			Use for 1GBit ETH operation	Use for 1GBit ETH operation
1x A7 @900Mhz	1x 64-bit A55 @1,4Ghz	2x 64-bit A55 @1,7Ghz	1x 64-bit A55 @1,4Ghz	2x 64-bit A55 @1,7Ghz
-	-	1x M33	-	1x M33
-	-	U65 NPU	-	U65 NPU
CSI	-	-	-	**MIPI CSI-2**
SD1	SD2	SD2	SD2	SD2
ETH1 (10/100MBit onboard)	ETH2 (10/100MBit onboard)	ETH2 (10/100MBit onboard)	ETH2 (10/100MBit onboard)	ETH2 (10/100MBit onboard)
ETH2 (10/100MBit RMII)	ETH1 (10/100MBit RMII)	ETH1 (10/100MBit RMII)	ETH1 **(1GBit R(G)MII +TSN)**	ETH1 **(1GBit R(G)MII +TSN)**
LCD	LCD/CSI	LCD/CSI/**LVDS**	LCD/CSI	LCD/CSI/**LVDS**
SD2	SD3	SD3	SD3 **(High Speed)**	SD3 **(High Speed)**

Dedizierte GPIO	Dedizierte GPIO	Dedizierte GPIO	Dedizierte GPIO	Dedizierte GPIO
I2C1	I2C	I2C	I2C	I2C
UART5	UART	UART	UART	UART
USB1	USB1	USB1	USB1	USB1
USB2	USB2	USB2	USB2	USB2
CCM	CCM	CCM	CCM	CCM
PWM	PWM	PWM	PWM	PWM
JTAG /Audio	JTAG	JTAG	JTAG	JTAG
VCC 3,3V	VCC 3,3V	VCC 3,3V	VCC 3,3V	VCC 3,3V
SNVS	-	-	-	-
UART1 (Debug)	UART1 (Debug)	UART1 (Debug)	UART1 (Debug)	UART1 (Debug)
UART2/SPI3	SPI1	SPI1	SPI1	SPI1

CSI/ UART3	UART2	UART2	UART2	UART2
CAN1/UART3	CAN1 **FD**	CAN1 **FD**	CAN1 **FD**	CAN1 **FD**
GPIO1.3/ADC1_IN3	ADC0	ADC0	ADC0	ADC0
Boot Pins	Boot Pins	Boot Pins	Boot Pins	Boot Pins
Tamper Pins	Tamper Pins	Tamper Pins	Tamper Pins	Tamper Pins

Special Dependencies for Display and Camera Signals

Because of the changed muxing options in i.MX 91/93 processor compared to the i.MX 6UL/ULL muxing, things like functions, display, and camera signals have special dependencies. The following table gives you a short overview. More detailed information will follow in the sections below.

When using ... Interface on phyCORE-i.MX 91/93	**This interface will not work in combination**	**This interface will work in combination**
Parallel Display	Parallel Camera, LVDS Display	MIPI CSI-2 Camera
Parallel Camera	Parallel Display	LVDS display, MIPI CSI-2 Camera
LVDS Display	Parallel Display	Parallel Camera, MIPI CSI-2 Camera

Compatibility Description

This section lists all the interfaces available on the phyCORE-i.MX 6UL/ULL and describes the impact of replacing PCL-063 with PCL-077. Solutions to make them compatible are also given.

Parallel Camera Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[1:5] X1-50 X1-[117:124]	X1-[20:22] X1-24 X1-[28:31] X1-33 X1-[36:37] X1-[39:40]
Info	Parallel Camera Interface (CSI) is available on SOM connector pins	Parallel camera interface as multiplex option available on parallel LCD interface. **Effect:** A parallel LCD interface is not available when a parallel camera interface is used. **Workaround:** The LVDS interface is also available as a multiplex option in hardware (jumper configuration on SOM) on the LCD interface. If a parallel LCD interface is required, an LVDS to RGB converter can be used. A second option is to use the MIPI CSI-2 interface instead of the parallel camera interface. Check SOM hardware options. **Note:** The location of the parallel camera interface signals is different from phyCORE-i.MX 6UL/ULL and must be adapted accordingly.

SD Card Interface

	phyCORE-i.MX 6UL/ULL	phyCORE-i.MX 91/93
SOM Pins involved	X1-[6:11] X1-108	
Additional SOM pins	X1-5	
Info	SD card interface (SD1) is available only on SOM connector pins	SD card interface (SD2) is explicitly available on the same SOM connector pins. In addition, an exclusive RESET signal for the SD2 interface is available to reset the SD card on connector pin X1-5. **Effect:** no effect on function **Note:** i.MX 91/93 supports higher speed grades at the SD2 interface, please ensure that the routing of the carrier board PCB can support higher frequencies. Respective IO levels of signals X_SD2_RESET and X_SD2_CD must be considered. It is recommended to use the phyBOARD-Segin (PBA-CD-10) as a reference for new designs. Please contact support@phytec.de for schematics.

SD2 Interface

	phyCORE-i.MX 6UL/ULL	phyCORE-i.MX 91/93
SOM Pins involved	X1-[44:49]	
Info	SD card interface (SD2) is available on SOM connector pins.	SD card interface (SD3) is available on SOM connector pins. **Effect:** SD3_CMD and SD3_CLK signals are incompatible due to the muxing option in the processor. This problem can be solved by using different J17 settings on the SOM. J17 1+4; 2+3 makes the interface compatible with the SD2 interface of the phyCORE-i.MX 6UL/ULL.

10/100Mbit Ethernet Interface on SOM

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[12:19]	
Info	10/100Mbit Ethernet PHY on SOM connected to ENET1 interface	10/100Mbit Ethernet PHY on SOM connected to ENET2 interface **Effect:** no effect on function

Parallel LCD Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[20:49]	
Info	Parallel LCD interface is explicitly available only on SOM connector pins	Parallel LCD interface is explicitly available only on SOM connector pins but affects other interfaces such as parallel camera interface. SOM configuration must be considered according to requirements. **Effect:** No parallel camera interface is available when using a parallel LCD interface, no LVDS interface is available. The availability of the SD3 interface depends on the bits used for the LCD interface. In 18-bit LCD mode SD3 is available, in 24-bit LCD mode SD3 is not available as on phyCORE-i.MX 6UL/ULL. J17 1+2; 2+4 on the SOM enable 24-bit LCD mode. **Workaround:** If a Camera interface is required, the serial camera interface MIPI CSI-2 can be used. A second way to connect a camera is to use the parallel camera interface as a multiplex option on the parallel LCD interface while using the LVDS interface to connect a display. **Note:** The above workarounds will break compatibility with phyCORE-i.MX6UL/L **Note:** When using LVDS and parallel camera interface to connect external devices, the SD3 interface is also available to connect other SDIO devices.

Second Ethernet Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[52:59]	X1-[52:59]
Additional SOM pins involved		X1-[50:51] X1-[60:61]
Info	Second Ethernet MAC interface available with RMII signal set. Supports additional Ethernet connectivity	A second Ethernet MAC interface is available with an RGMII signal set, which also supports the RMII interface function. **Effect:** In RMII mode, the interface is fully compatible with the phyCORE-i.MX 6UL/ULL. Using RGMII will break compatibility. The I.MX93/91 Processor only supports RGMII when the IO level of the processor is set to 1,8V. Since the I.MX6UL/l IO voltage is 3,3V, RGMII can not be used if compatibility with the phyCORE-I.MX6UL/L is desired, In addition, using the interface in RGMII mode also has an impact on the I2C1 interface of the phyCORE-i.MX 93, and will also break compatibility to the phyCORE-i.MX6UL/ULL. **Workaround:** Use RMII only, for compatibility. If RGMII is required IO level adjustment must be done for all IOs. In addition, a different I2C interface must be used for external I2C devices, such as X1-95(GPIO_IO02_I2C2_SDA) / X1-96 (GPIO_IO3_I2C2_SCL). **Caution:** In RGMII mode the system has 1.8V IO voltage.

I2C1 Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[60:61]	
Info	I2C1 interface is available for connecting external I2C devices. **Note:** This interface is also used by components on the SOM (EEPROM, 0x52/0x5A). More information about EEPROM can be found in the section I2C EEPROM (U10) of our Hardware Manual.	I2C Signals are available via FLEX-IO emulation. **Effect:** Since a FLEX-IO unit is used to emulate the I2C interface, differences in performance and behavior might have to be expected. **Workaround:** To ensure full I2C functionality, use another dedicated I2C interface such as I2C2 on connector pins X1-95 (I2C2_SCL) and X1-96 (I2C2_SDA).

UART5 Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[63:64] X1-[74:75]	
info	UART5 interface is available for connecting external UART devices.	UART signals are only available via the FLEX-IO signal interface (no dedicated UART IP), limited by the nature of FLEX-IO functionality **Effect:** FLEX-IO signals can be used to generate a UART interface **Workaround:** If full UART functionality is required, use another dedicated UART interface, such as UART5 on connector pins X1-79 (X_DAP_TDI/UART5_RX) and X1-82 (X_DAP_TDO/UART5_TX).

USB_OTG1 Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[65:68] X1-97	
Info	USB-OTG1 interface with Charged Detect (CHD) signal available	USB-OTG1 interface without Charge Detect signal available on SOM connector. **Effect:** No dedicated Charge Detect signal. Signal pin X1-68 is used for Charge Detect with phyCORE-i.MX 6UL/ULL is only 1.8V compatible and not usable as GPIO for phyCORE-i.MX 91/93. **Workaround:** If necessary, use a compatible and available GPIO signal to generate the charge detect signal.

USB_OTG2 Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[69:71] X1-76	
Info	USB-OTG2 interface available	USB-OTG2 is available on the same SOM connector pins. **Effect:** None

CCM CLK Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[72:73]	
Info	High-speed differential input/ output clock interface available	Single-ended output clocks available **Effect:** No differential clock interface available, only two single-ended output clocks **Workaround:** If the carrier board provides differential input signals on these pins, please use the single-ended clock interface on X1-68 (CLKIN1) and X1-118 (CLKIN2) instead. If the external differential input of the carrier board is used as the output clock, check if AC coupling is possible to convert to a single-ended clock. To achieve AC coupling the first clock signal has to be decoupled by a capacitor and the second differential clock signal has to be coupled to GND by a capacitor. Otherwise, a differential to single-ended clock conversion of the signal is required.

JTAG Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[79:84]	
Info	JTAG interface available for debug and BSCAN functions	JTAG interface is also available but without JTAG_MOD and JTAG_nTRST signals. **Effect:** Nothing **Note:** Interface can also be used as SWD interface by tying JTAG_TMS to GND.

SOM Control Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[98:102]	
Info	SOM 3.3V logic control interface available	SOM Control interface available with 1.8V logic **Effect:** For all signals intended to be pulled to GND, no effect is expected. **The following signals are affected:** • X_ONOFF (X1-99) - Pullup 1.8V on SOM • X_nRESET_IN (X1-100)- Pullup 1.8V in PMIC • X_PMIC_ON_REQ (X1- 101)- Pullup 1.8V on SOM • X_PMIC_STBY_REQ (X1-102) - 1.8V output from uP • X_nRESET_OUT (X1-98) - VDD_IO dependent

POWER Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
Main Power Supply		
SOM pins involved	X1-[90:93]	
Info	3.3V power directly to SOM and peripherals	3.3V SOM power must be supplied first, peripheral power must follow the SOM power-up sequence **Effect:** Power up of peripherals connected to SOM must be sequenced by signal X_nPWR_READY of SOM, pin X1-103 **Workaround:** Use a load switch to sequence the power of external devices connected to the SOM via signal lines.
SNVS Power Supply		
SOM pins involved	X-94	
Info	Backup power supply via pin X1-94 to power the SNVS domain	Pin X1-94 unconnected, SNVS power domain is sourced from the PMIC on the SOM. **Effect:** In standby mode, a supply of Pin X1-94 is not required. Instead, the main power supply of the SOM must be kept available for the PMIC and can not be turned off during stand-by mode. The processor will use the SNVS domain provided by the PMIC to enter standby mode.

BOOT Mode Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[25:49] X1-[103:104]	X1-107 X1-109 X1-111 X1-116
Info	Boot configuration: BOOTCFG[1:2,4] X1-[25:49] Boot mode interface: X_BOOT_MODE[1:0] X1-[103:104]	The Boot configuration is reduced to four IO signals which are latched during RESET. The boot mode interface (X_BOOT_MODE[3:0]) is available in a different location compared to the phyCORE-i.MX6UL/L. **Effect:** A default boot mode is defined by the SOM which can be altered, Therefore X_BOOT_MODE[3:0] must be configured to support the desired boot modes. BOOTCFG[1:2,4] must be cleared for phyCORE-i.MX 6UL/ULL. **Workaround:** Use the default boot mode setup on the SOM while external signals are not connected. **Note:** Please ensure that external components connected to X_BOOT_MODE[3:0] do not affect latching during boot-up.

UART1 Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[105,107]	
Info	UART1 interface available without handshake signals on SOM connector	UART1 interface available on same pins of SOM connector without handshake signals **Effect:** None
Note: This is the system's standard serial debug interface.		

ECSPI3 / UART2 Interface

	phyCORE-i.MX 6UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[109:112]	
Info	ECSPI3 / UART2 interface available on SOM connector	The SPI interface function is given as a dedicated IP core with compatibility with the SOM connector pins, but there is no dedicated UART interface available on the same pins of the SOM connector. **Effect:** The UART interface function is not available on these SOM pins. **Workaround:** UART - Check for other IO pins with UART functionality to solve the problem.

CAN / UART3 Interface

	phyCORE-i.MX6 UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[113:116]	
Info	CAN1 / UART3 interface available on SOM connector, UART 3 integrates handshake signals	CAN1 interface is available on the same pins as the SOM connector. UART2 with RX/TX signals available on the same pins as UART (i.MX 6UL/ULL) but without handshake signals. **Effect:** Using the CAN1 interface has no impact on functionality; for UART2 no handshake signals are available on the same pins of the UART2 interface of the SOM. **Workaround:** UART2 - Check the availability of UART2 handshake signals on other SOM pins.

GPIO Interface

	phyCORE-i.MX6 UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-51 X1-78 X1-[85:88] X1-[95:96] X1-106	
Info	Multiple GPIO pins are available for use	Several GPIO pins are available via the processor GPIO controller, additionally FLEXIO controller is available for support of additional functions. **Effect:** None

ADC Interface

	phyCORE-i.MX6 UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[74:78] X1-96 X1-97	X1-[3-4] X1-81
Info	Multiple GPIO1 pins available for analog input from processor ADC	Dedicated ADC pin function on phyCORE-i.MX 91/93. ADC function is very different from phyCORE-i.MX 6UL/ULL. **Effect:** Analogue input pins are on different pins of the SOM. Maximum ADC voltage is 1.8V versus 3.3V on phyCORE-i.MX 6UL/ULL. **Workaround:** The analog input circuit must be modified for phyCORE-i.MX 91/93. Set an external resistor divider on the analog inputs to select the maximum input voltage.

TAMPER Interface

	phyCORE-i.MX6 UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-51 X1-[85:88] X1-95	X1-2 X1-104
Info	Multiple GPIO5 pins available for the TAMPER function	Two dedicated TAMPER pins are available on i.MX 91/93 **Effect**: TAMPER pins are located on different pins of the SOM. TAMPER interface IO voltage level is 1.8V versus 3.3V of i.MX 6UL/ULL **Workaround:** Select other TAMPER pins, and set the external resistor divider to select max. input voltage.

MISC Interfaces

	phyCORE-i.MX6 UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-68 X1-118	
Info	Affected signals: • Charge Detect of USB_OTG1 • Data signal D3 from CSI	Function changed to dedicated CLKIN interface available on phyCORE-i.MX 91/93 with signals CLKIN1 and CLKIN2. **Effect:** Charge detection function X_USB_OTG1_CHD_B and CSI data signal X_CSI_D3 are no longer available on corresponding SOM pins. **Workaround:** If a Charge Detect Function is required, check for other GPIO pins to set up the function. If Data 3 of parallel camera interface is needed, use multiplexed pCAM interface on LCD signals. **Caution:** If CLKIN1/2 is not used, an external 10K pull-down per pin is recommended.

RTC_XTAL Interface

	phyCORE-i.MX6 UL/ULL	**phyCORE-i.MX 91/93**
SOM Pins involved	X1-[140:141]	
Info	The SOM's RTC_XTAL interface is connected directly to the processor's RTC_XTAL interface.	The RTC_XTAL interface of the SOM connector is directly connected to the RTC Crystal interface of the PMIC. **Effect:** None

Revision History

Date	Version #	Changes to this Manual
05.03.2024	LAN-114e.A0	Preliminary Version