phyCORE®-TC399

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the KSP-0200 System on Module, henceforth referred to as phyCORE®-TC399. The manual specifies the phyCORE®-TC399's design and function. Precise specifications for the Infineon® Semiconductor TC399 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Note: We refrain from providing detailed, part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products. Please read the section**"Product Change Management and information in this manual on parts populated on the SOM"** within the *Preface.*

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: RD) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connector on the undersides of the phyCORE-i.MX°8M System on Module.

Types of Signals

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of a signal.

Signal Type	Description	Abbr.
Power	Supply voltage input	PWR_I
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
OC-Bidir PU	Open collector input/output with pull up	OC-BI
OC-Output	Open collector output without pull up, requires an external pull up	OC
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O

Table 1: Signal Types used in this Manual

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
CB	Carrier Board; used in reference to the phyCORE Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
GPI	General purpose input.
GPIO	General purpose input and output.
GPO	General purpose output.
IRAM	Internal RAM; the internal static RAM on the Infineon® Semiconductor TC399 microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
PEB	PHYTEC Extension Board
POR	Power-on reset
RTC	Real-time clock.
SMT	Surface mount technology.
SOM	System on Module; used in reference to the phyCORE-TC399 module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board.

Table 2: Abbreviations and Acronyms used in this Manual

Preface

As a member of PHYTEC's phyCORE® product family, the phyCORE-TC399 is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, thereforeoffers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE® module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce development time and risk and allows for increased focus on the product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

For more information go to:

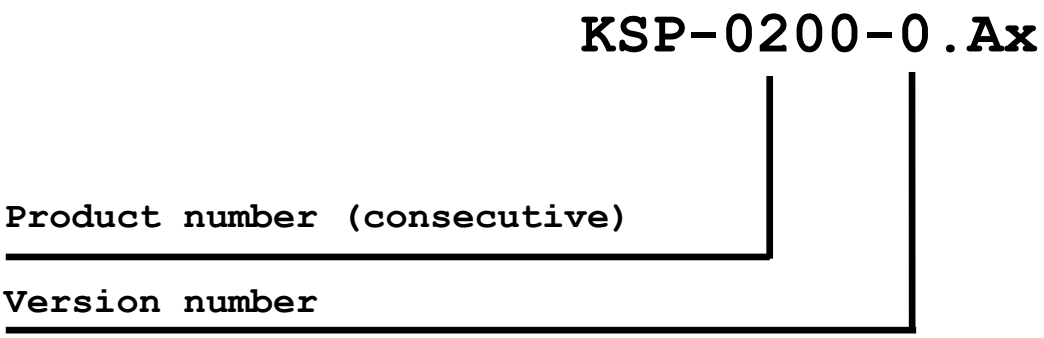
http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html

or

http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyCORE-TC399 has the following structure:



Product Specific Information and Technical Support

In order to receive product specific information on all future changes and updates, we recommend registering at:

http://www.phytec.de/de/support/registrierung.html

or

http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/support/knowledge-database/

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE®-TC399

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
PHYTEC products lacking protective enclosures are subject to damage by ESD and, therefore, must be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union’s Directive for Electro Magnetic Conformity only in accordance with the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM / SBC

With the purchace of a PHYTEC SOM / SBC, you will, in addition to our HW and SW offerings, receive free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are constantly being evaluated in order to take the right measures in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating longevity of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in the rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Change management in cases of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.

- Provide early change notifications concerning functional relevant changes of our products.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

1 Introduction

The phyCORE-TC399 belongs to PHYTEC's phyCORE System on Module family. phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini, micro, and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

Independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments. phyCORE board design features an increased pin package which allows for the dedication of approximately 20 % of all connector pins on the phyCORE boards to ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMT components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-TC399 is a subminiature (57 mm x 71.5 mm) insert-ready System on Module populated with the Infineon® Semiconductor TC399 microcontroller. Its universal design enables its insertion into a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.5 mm) connectors aligning two sides of the board, allowing it to be plugged, like a "big chip", into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller reference manual or datasheet. The descriptions in this manual are based on the Infineon ® Semiconductor TC399. No description of compatible microcontroller derivative functions is

included, as such functions are not relevant for the basic functioning of the phyCORE-TC399.

1.1 Features of the phyCORE-TC399

The phyCORE-TC399 offers the following features:

1.1.1 Internal Features of the TC399

- Processor: Infineon TC39x (LFGBA516)
- Architecture: Aurix 2nd Gen. Controller
- Clock Frequency: up to 6x 300 MHz
- Flash (on chip): up to 16 MB

1.1.2 Memory Configuration of the phyCORE-TC399

- SRAM: up to 8MByte (10ns) (standard: 5MB)
- EEPROM: up to 32kB (SPI) (standard: 8kB)

1.1.3 Other Board-Level Features of the phyCORE-TC399

- Single 3.3V supply for phyCORE-TC399 module
- All controller-required supplies are generated on-board
- Voltage Supervisor IC
- Two RS-232 transceivers for channel UART0 and UART7 (RxD/TxD), also usable as TTL
- 10/100/100 Mbit/s DP83867IRRGZ , RGMII access from MCU
- 10/100 Mbit/s W5300, 16-bit EBU access from MCU
- Bootconfig pins for boot source selection (DIP-Switch)
- Support of 16-pin OCDS1 JTAG or 10-pin DAP debug interface through dedicated connectors
- I2C-RTC battery-buffered
- SD-Card interface (SPI-Mode)
- Four CAN-Transceivers , also usable as TTL
- Industrial temperature range (-40 °C to +85 °C)
- Free I/Os from MCU available on phyCORE-Connector

1.2 Block Diagram

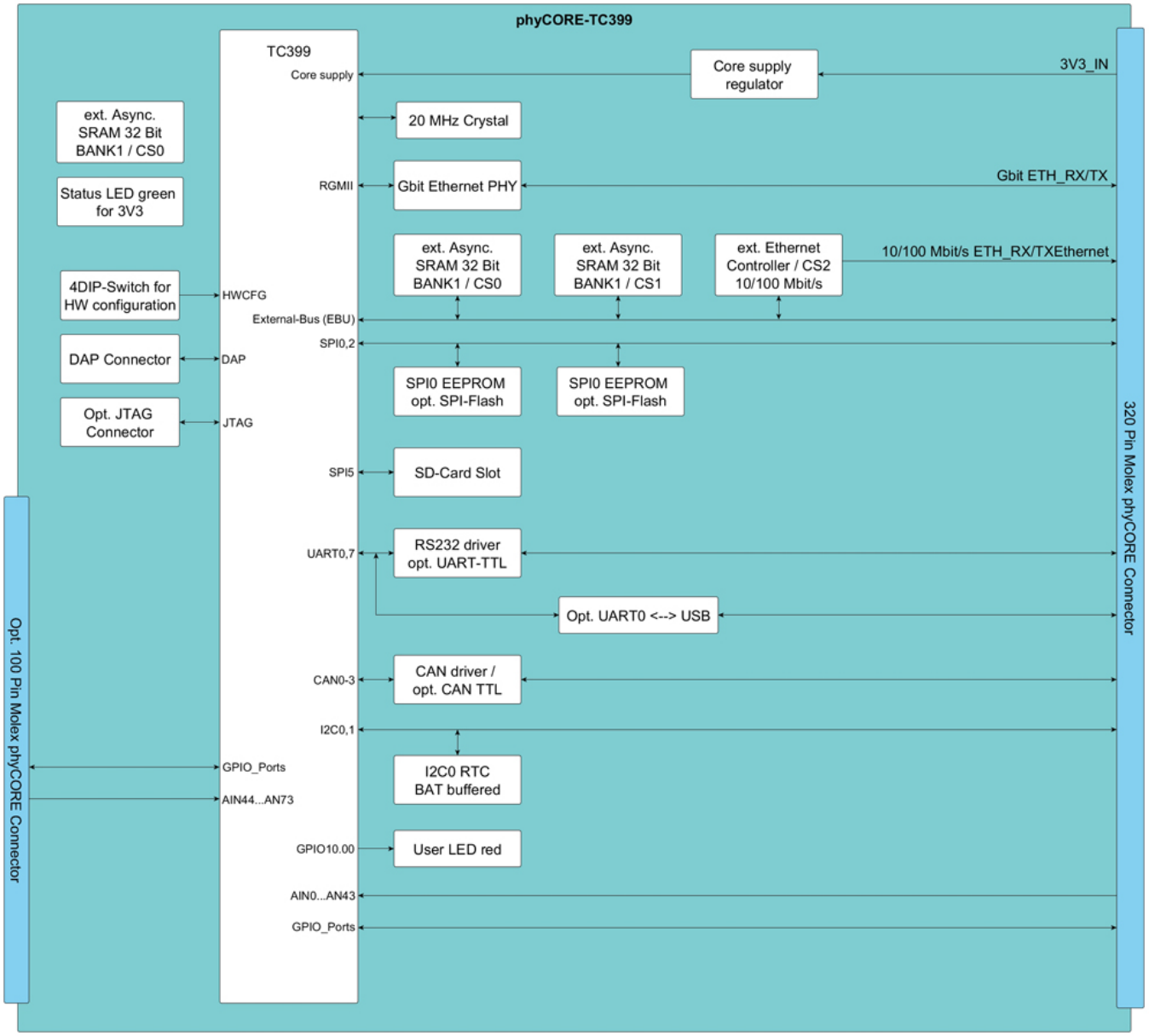


Figure 1: Block Diagram of the phyCORE-TC399

1.3 Component Placement Diagram

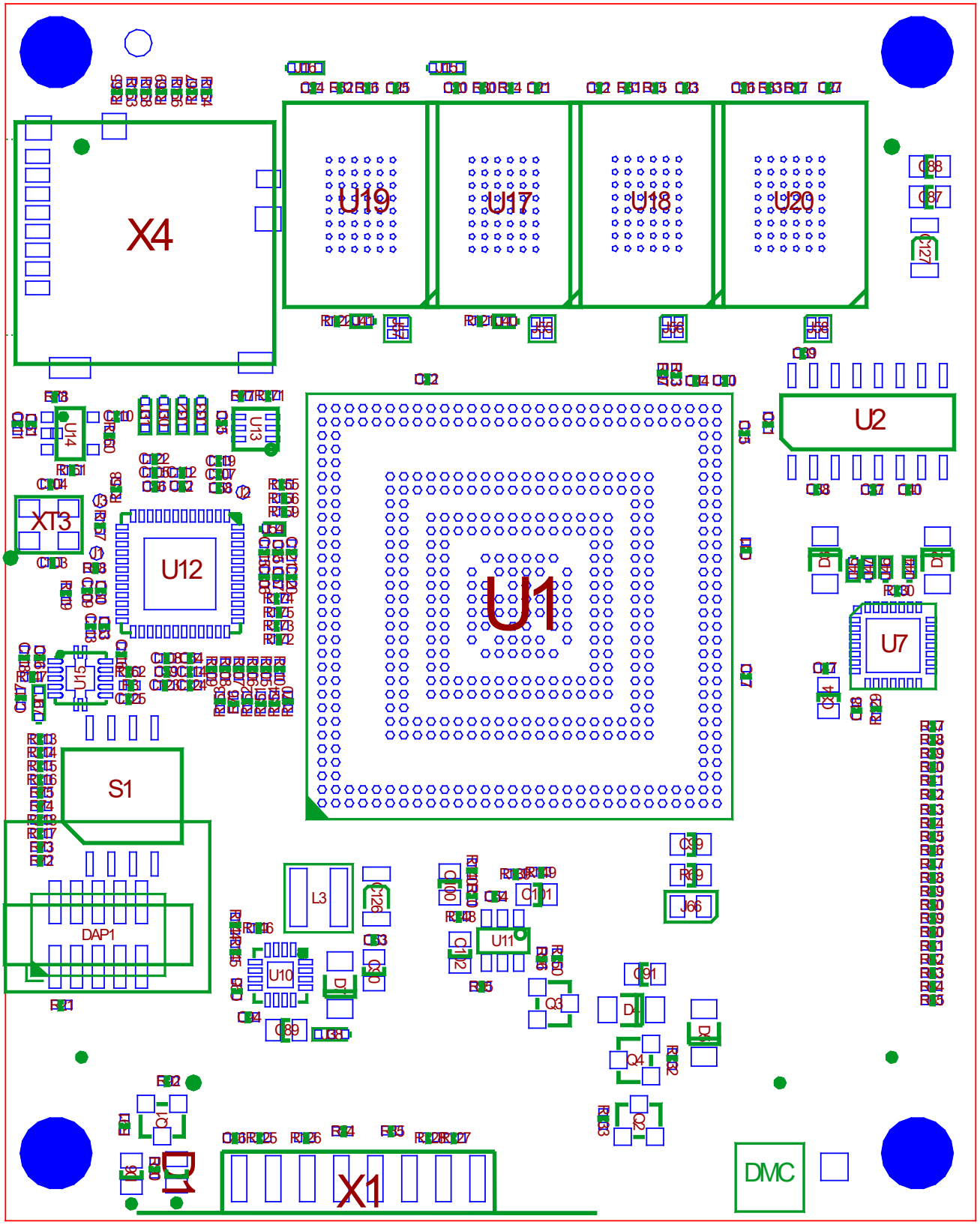


Figure 2: phyCORE-TC399 Component Placement (top view)

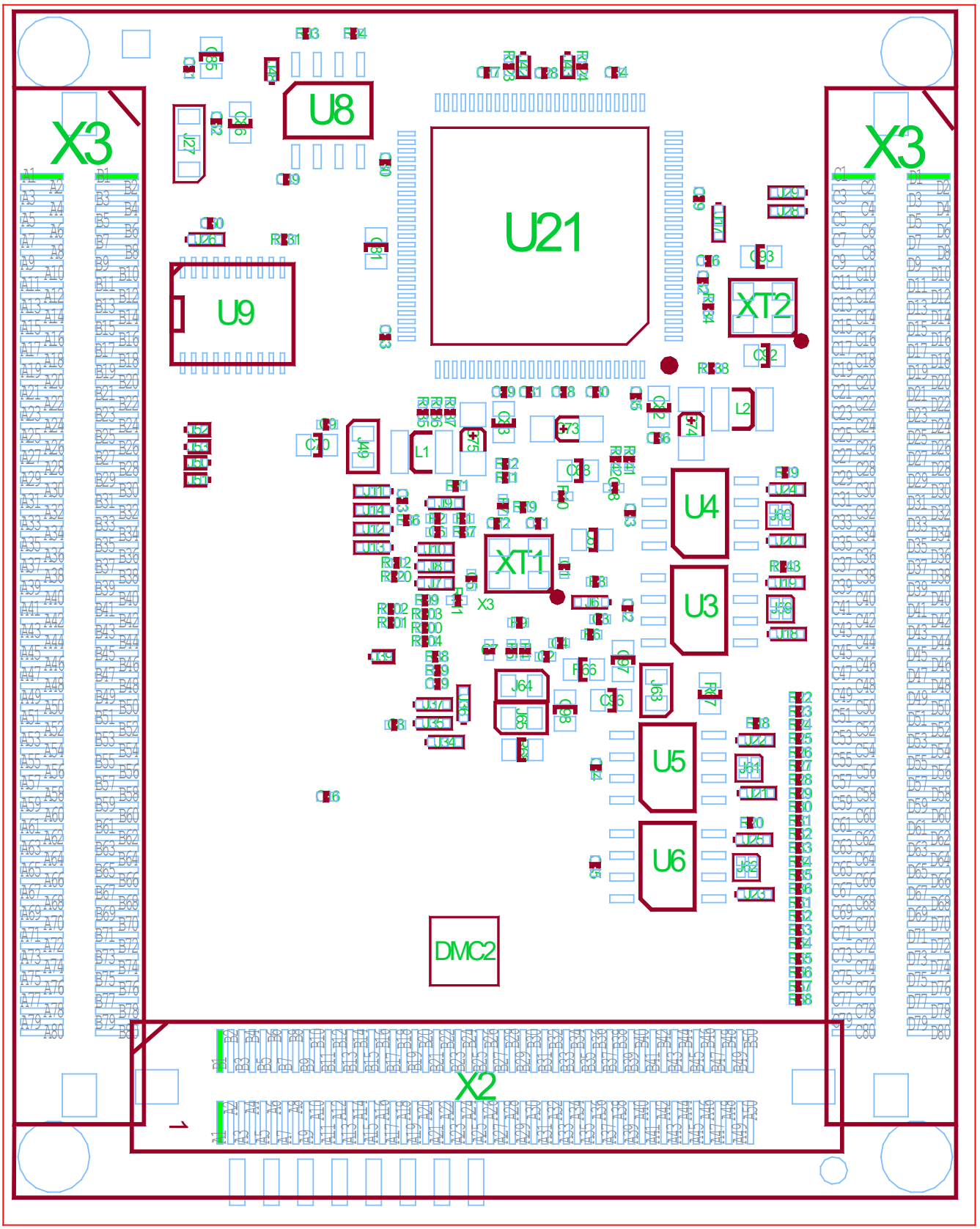


Figure 3: phyCORE-TC399 Component Placement (bottom view)

1.4 Minimum Requirements to operate the phyCORE-TC399

Basic operation of the phyCORE-TC399 requires a single supply of +3.3 V input voltage with 2.5 A load and the corresponding GND connection.

The following supply pins are located at the phyCORE-Connector X3:

3V3 -> X3 -> 1C, 2C, 1D,2D

Connect all +3.3 V VCC input pins to your power supply and, at minimum, the matching number of GND pins.

Corresponding GND -> X3 -> 3C, 3D, 7C, 7D

Please refer to *Section 2* for information on additional GND Pins located at the phyCORE-Connector X3.

Caution!
PHYTEC recommends connecting all available +3.3 V input pins to the power supply system on a custom carrier board housing the phyCORE-TC399 and, at the very least, the matching number of GND pins neighboring the +3.3 V pins.

In addition, proper implementation of the phyCORE-TC399 module into a target application also requires connecting all GND pins.

Please refer to *Section 4* for more information.

2 Pin Description

Please ensure that all module connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals selected extend to surface mount technology (SMT) connectors (0.635 mm) lining three sides of the module (referred to as phyCORE-Connector). This allows the phyCORE-TC399 to be plugged into any target application like a "big chip".

The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. The pin numbering values increase moving down the board (*Figure 4*).

The numbered matrix can be aligned with the phyCORE-TC399 (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin X3A1) is, therefore, covered with the corner of the phyCORE-TC399. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

This allows the numbering scheme to be consistent for both the module’s phyCORE-Connector as well as the mating connector on the phyCORE Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-Connector is usually assigned a single designator for its position (X3 for example). In this manner, the phyCORE-Connector comprises a single, logical unit regardless of the fact that it could consist of more than one physically-socketed connector.

Figure 4 illustrates the numbered matrix system. It shows a phyCORE-TC399 with both SMT phyCORE-Connectors on its underside (defined as dotted lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-TC399 module showing the phyCORE-Connector mounted on the underside of the module's PCB.

Table 3 to *Table 8* provide an overview of the pinout of the phyCORE-Connector X3 and the optional connector X2 with signal names and descriptions specific to the phyCORE-TC399. It also provides the appropriate voltage domain, signal type (ST), and a functional grouping of the signals. The signal type also includes information about the signal direction [1]. A description of the signal types can be found in *Table 1*.

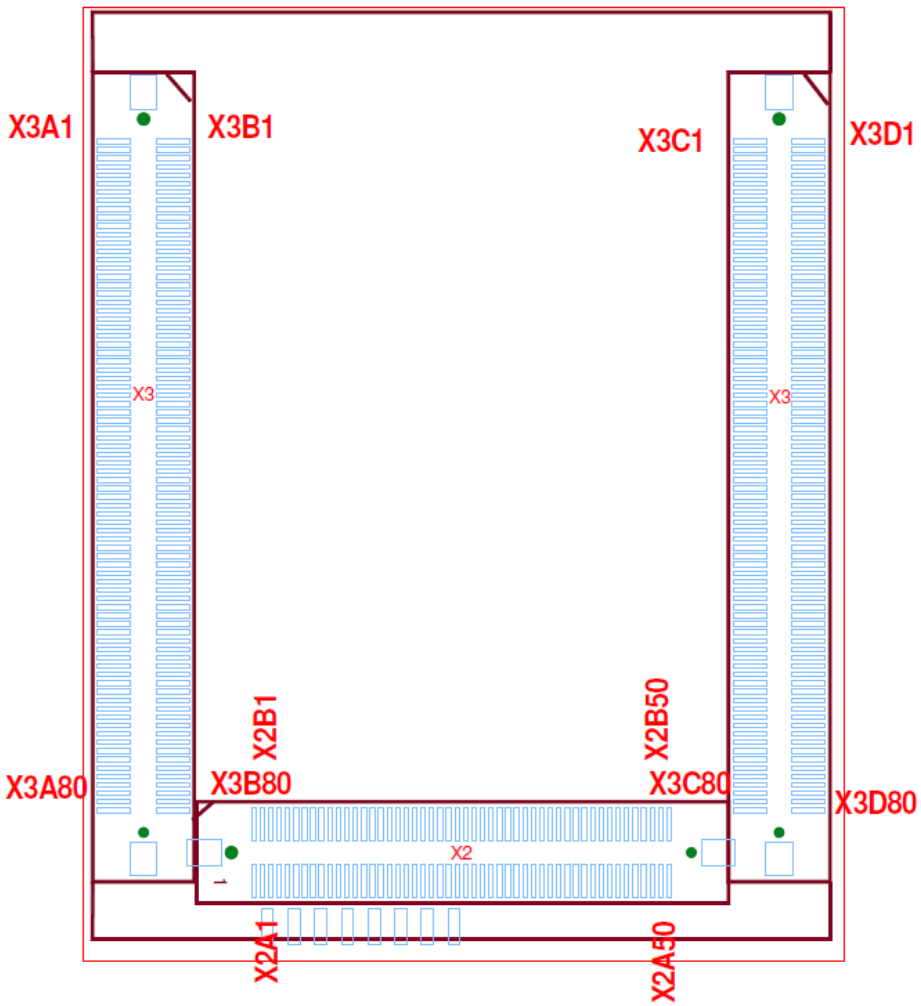


Figure 4: Pinout of the phyCORE-Connector (top view)

1: The specified direction indicated refers to the standard phyCORE use of the pin.

Caution!

- The Infineon® Semiconductor phyCORE-TC399 is a multi-voltage-operated microcontroller and, as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Infineon® Semiconductor TC399 Reference Manual* for details on the functions and features of controller signals and port pins.
- As some of the signals which are brought out on the phyCORE-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset. The signals which may affect the boot configuration are shown in *Table 12*. It is necessary to avoid voltages at the IO pins of the phyCORE-TC399 which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up or power-down. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the TC399 are supposed to be powered while the phyCORE-TC399 is in suspend mode or turned off.

Note:

- Most of the controller pins have multiple multiplexed functions. As most of these pins are connected directly to the phyCORE-Connector, the alternative functions are available by using the phyCORE-TC399's pin muxing options. Signal names and descriptions in *Table 3* to *Table 8*, however, are in regard to the specification of the phyCORE-TC399 and the functions defined therein. Please refer to the *TC399 Reference Manual* or the schematic to understand the alternative functions. In order to utilize a specific pin's alternative function, the corresponding registers must be configured within the appropriate register in the software.
- The following tables describe the full set of signals available at the phyCORE-Connector according to the phyCORE-TC399 specification. However, the availability of some interfaces is order-specific (e.g. Camera_0). This means some signals might not be available on your module.

Pin#	Signal	Signal Type	Signal Level	Description
X3A1	NC / 1V25EXT	- /PWR_I	- / 1.25V	Not connected or MCU core Supply input (refer to jumper J49)
X3A2	GND	-	-	Ground 0 V
X3A3	P1508 /REQ5	I/O	3.3 V	GPIO P15.08 used as IRQ input for the the Gbit RGMII PHY U12. Free to use if the U12 is NOT populated or jumper J54 is open (refer to jumper J54)
X3A4	/ESR1	I	3.3V	ESR1 Port Pin input, can be used to trigger a reset or an NMI
X3A5	/CS2	I/O	3.3V	EBU Chip Select output. Used for onboard Ethernet Controller U21 Free to use if the U21 is NOT populated or jumper J42 is open (refer to jumper J42)
X3A6	/ADV	I/O	3.3V	GPIO P25.07, can be used as Address Valid Control Signal
X3A7	GND	-	-	Ground 0 V
X3A8	/BC0	O	3.3V	EBU Byte Control Signa0
X3A9	A1	O	3.3V	EBU address line A1
X3A10	A2	O	3.3V	EBU address line A2
X3A11	A4	O	3.3V	EBU address line A4
X3A12	GND	-	-	Ground 0 V
X3A13	A7	O	3.3V	EBU address line A7
X3A14	A9	O	3.3V	EBU address line A9
X3A15	A10	O	3.3V	EBU address line A10
X3A16	A12	O	3.3V	EBU address line A12
X3A17	GND	-	-	Ground 0 V
X3A18	A15	O	3.3V	EBU address line A15
X3A19	D1	I/O	3.3V	EBU data line D1
X3A20	D2	I/O	3.3V	EBU data line D2
X3A21	D4	I/O	3.3V	EBU data line D4
X3A22	GND	-	-	Ground 0 V
X3A23	D7	I/O	3.3V	EBU data line D7
X3A24	A17/ X_ETH0_DN	O/ETH_I/O	*3.3V / ETH*	Gbit Ethernet X_ETH0_DN or EBU address line A10 (refer to jumper J31)

Table 3: Pinout of the phyCORE-Connector X3, Row A

Pin#	Signal	Signal Type	Signal Level	Description
X3A25	A18 / X_ETH0_DP	O/ETH_I/O	*3.3V / ETH*	Gbit Ethernet X_ETH0_DP or EBU address line A18 (refer to jumper J30)
X3A26	NC / X_ETH0_CN	O/ETH_I/O	*- / ETH*	Gbit Ethernet X_ETH0_CN or Not Connected (refer to jumper J50)
X3A2	GND	-	-	Ground 0 V

7				
X3A28	NC / X_ETH0_CP	- /ETH_I/O	*- / ETH*	Gbit Ethernet X_ETH0_CP or Not Connected (refer to jumper J51)
X3A29	D9	I/O	3.3V	EBU data line D9
X3A30	D10	I/O	3.3V	EBU data line D10
X3A31	D12	I/O	3.3V	EBU data line D12
X3A32	GND	-	-	Ground 0 V
X3A33	D15	I/O	3.3V	EBU data line D15
X3A34	/WAIT	O	3.3V	GPIO P25.06, can be used as EBU_WAIT input Signal
X3A35	NC	-	-	Not connected
X3A36	NC	-	-	Not connected
X3A37	GND	-	-	Ground 0 V
X3A38	D17	I/O	3.3V	EBU data line D17
X3A39	D19	I/O	3.3V	EBU data line D19
X3A40	D20	I/O	3.3V	EBU data line D20
X3A41	D22	I/O	3.3V	EBU data line D22
X3A42	GND	-	-	Ground 0 V
X3A43	D25	I/O	3.3V	EBU data line D25
X3A44	D27	I/O	3.3V	EBU data line D27
X3A45	D28	I/O	3.3V	EBU data line D28
X3A46	D30	I/O	3.3V	EBU data line D30
X3A47	GND	-	-	Ground 0 V
X3A48	LAN_/CS	I	3.3V	Chip Select input of the onboard Ethernet Controller (U21). Can be used if jumper J42 is open (refer to jumper J42)
X3A49	/WR	O	3.3V	EBU write Control
X3A50	BFCLKI	I	3.3V	EBU Burst Flash Clock Feedback, onboard connected to BFCLKO via R97/R13
X3A51	BFCLKO	O	3.3V	EBU Burst Flash Clock Output, onboard connected to BFCLKI via R97/R13

X3A52	GND	-	-	Ground 0 V
X3A53	/CSRAM2	I	3.3V	Chip Select input of the second RAM BANK, can be used if jumper J41 is open (refer to jumper J41).
X3A54	P0011	I/O	3.3V	GPIO P00.11
X3A55	P0010	I/O	3.3V	GPIO P00.10
X3A56	P0008	I/O	3.3V	GPIO P00.08
X3A57	GND	-	-	Ground 0 V
X3A58	P0005	I/O	3.3V	GPIO P00.05
X3A59	P0004	I/O	3.3V	GPIO P00.04
X3A60	P0003	I/O	3.3V	GPIO P00.03
X3A61	P0001	I/O	3.3V	GPIO P00.01
X3A62	GND	-	-	Ground 0 V
X3A63	P0202	I/O	3.3V	GPIO P02.02
X3A64	P0214	I/O	3.3V	GPIO P02.14
X3A65	P2007	I/O	3.3V	GPIO P20.07

Table 3: Pinout of the phyCORE-Connector X3, Row A (cont.)

Pin#	Signal	Signal Type	Signal Level	Description
X3A66	P2307	I/O		GPIO P23.07
X3A67	GND	-		Ground 0 V
X3A68	P2304	I/O		GPIO P23.04
X3A69	P2302	I/O		GPIO P23.02
X3A70	P2301	I/O		GPIO P23.01
X3A71	P0204 / P0208	I/O		GPIO P02.04 / P02.08 (refer to jumper J34)
X3A72	GND	-		Ground 0 V
X3A73	P0106	I/O		GPIO P01.06
X3A74	P0104	I/O		GPIO P01.04
X3A75	P0103	I/O		GPIO P01.03
X3A76	P0207 / P0210	I/O	3.3V	GPIO P02.07 / P02.10 (refer to jumper J36)
X3A77	GND	-	-	Ground 0 V
X3A78	P3305 / SLSO07	I/O	3.3V	GPIO P33.05
X3A79	P3403 / SLSO210	I/O	3.3V	GPIO P34.03
X3A80	P2006 / SLSO28	I/O	3.3V	GPIO P20.06

Table 3: Pinout of the phyCORE-Connector X3, Row A (cont.)

Pin#	Signal	Signal Type	Signal Level	Description
X3 B1	RTC_CLKOUT /1V25EXT	O/PWR_I	3.3V / 1.25V	Real Time Clock Clockout or MCU core Supply input (refer to jumper J26)
X3 B2	P3307 / REQ4	I/O	3.3V	GPIO P33.07 used as IRQ input for the onboard 100Mbit Ethernet Controller U21. Free to use if the U21 is NOT populated or jumper J43 is open (refer to jumper J43)
X3 B3	P1403 /HWCFG3/SLSO23	I/O	3.3V	GPIO P14.03 - HWCFG3 (bootmode pin) (refer to DIP-switch S1)
X3 B4	GND	-	-	Ground 0 V
X3 B5	/CS1	O	3.3V	EBU Chip Select output. Used for the second RAM BANK U19/U20. Free to use if the U19/U20 is NOT populated or jumper J41 is open (refer to jumper J41)
X3 B6	/CS0	O	3.3V	EBU Chip Select output. Used for the first RAM BANK U17/U18. Free to use if the U17/U18 is NOT populated or jumper J40 is open (refer to jumper J40)
X3 B7	/RD	O	3.3V	EBU read Control
X3 B8	A0	O	3.3V	EBU address line A0
X3 B9	GND	-	-	Ground 0 V
X3 B10	A3	O	3.3V	EBU address line A3
X3 B11	A5	O	3.3V	EBU address line A5
X3 B12	A6	O	3.3V	EBU address line A6
X3 B13	A8	O	3.3V	EBU address line A8
X3 B14	GND	-	-	Ground 0 V
X3	A11	O	3.3V	EBU address line A11

Pin#	Signal	Signal Type	Signal Level	Description
B15				
X3B16	A13	O	3.3V	EBU address line A13
X3B17	A14	O	3.3V	EBU address line A14
X3B18	D0	I/O	3.3V	EBU data line D0
X3B19	GND	-	-	Ground 0 V
X3B20	D3	I/O	3.3V	EBU data line D3
X3B21	D5	I/O	3.3V	EBU data line D5

Table 4: Pinout of the phyCORE-Connector X3, Row B

Pin#	Signal	Signal Type	Signal Level	Description
X3B22	D6	I/O	3.3V	EBU data line D6
X3B23	A16 / X_ETH0_BN	O /ETH_I/O	*3.3V / ETH*	Gbit Ethernet X_ETH0_BN or EBU address line A16 (refer to jumper J32)
X3B24	GND	-	-	Ground 0 V
X3B25	A19 / X_ETH0_BP	O /ETH_I/O	*3.3V / ETH*	Gbit Ethernet X_ETH0_BP or EBU address line A19 (refer to jumper J33)
X3B26	NC / X_ETH0_AN	O /ETH_I/O	*3.3V / ETH*	Gbit Ethernet X_ETH0_AN Optional: NC (refer to jumper J52)
X3B27	NC / X_ETH0_AP	O /ETH_I/O	*3.3V / ETH*	Gbit Ethernet X_ETH0_AP Or Not Connected (refer to jumper J53)
X3B28	D8	I/O	3.3V	EBU data line D28
X3B29	GND	-	-	Ground 0 V
X3B30	D11	I/O	3.3V	EBU data line D11
X3B31	D13	I/O	3.3V	EBU data line D13
X3B32	D14	I/O	3.3V	EBU data line D14
X3B33	/BC1	O	3.3V	EBU Byte Control Signa1
X3B34	GND	-	-	Ground 0 V
X3B35	NC	-	-	Not Connected
X3B36	NC	-	-	Not Connected
X3B37	D16	I/O	3.3V	EBU data line D16

X3B38	D18	I/O	3.3V	EBU data line D18
X3B39	GND	-	-	Ground 0 V
X3B40	D21	I/O	3.3V	EBU data line D21
X3B41	D23	I/O	3.3V	EBU data line D23
X3B42	D24	I/O	3.3V	EBU data line D24
X3B43	D26	I/O	3.3V	EBU data line D26
X3B44	GND	-	-	Ground 0 V
X3B45	D29	I/O	3.3V	EBU data line D29
X3B46	D31	I/O	3.3V	EBU data line D31
X3B47	NC	-	-	Not Connected
X3B48	NC	-	-	Not Connected
X3B49	GND	-	-	Ground 0 V
X3B50	/ADV	O	3.3V	EBU address valid output
X3B51	NC	-	-	Not Connected
X3B52	/BC2	O	3.3V	EBU Byte Control Signa2
X3B53	/BC3	O	3.3V	EBU Byte Control Signa3
X3B54	GND	-	-	Ground 0 V
X3B55	P0012	I/O	3.3V	GPIO P00.12
X3B56	P0009	I/O	3.3V	GPIO P00.09
X3B57	P0007	I/O	3.3V	GPIO P00.07
X3B58	P0006	I/O	3.3V	GPIO P00.06
X3B59	GND	-	-	Ground 0 V
X3B60	P0002	I/O	3.3V	GPIO P00.02
X3B61	P0000	I/O	3.3V	GPIO P00.00
X3B62	P0205	I/O	3.3V	GPIO P02.05
X3B63	P2013 / SLSO02	I/O	3.3V	GPIO P20.13
X3B64	GND	-	-	Ground 0 V
X3B65	P0206	I/O	3.3V	GPIO P02.06
X3B66	P2306	I/O	3.3V	GPIO P23.06

Table 4: Pinout of the phyCORE-Connector X3, Row B (cont.)

Pin #	Signal	Signal Type	Signal Level	Description
X3B 67	P2305	I/O	3.3V	GPIO P23.05
X3B 68	P2303	I/O	3.3V	GPIO P23.03
X3B 69	GND	-	-	Ground 0 V
X3B 70	P2300	I/O	3.3V	GPIO P23.00
X3B 71	P0201 / P0211	I/O	3.3V	GPIO P02.01 / P02.11 (refer to jumper J35)
X3B 72	P0107	I/O	3.3V	GPIO P01.07
X3B 73	P0105	I/O	3.3V	GPIO P01.05
X3B 74	GND	-	-	Ground 0 V
X3B 75	P0203	I/O	3.3V	GPIO P02.03
X3B 76	P0200 / P0209	I/O	3.3V	GPIO P02.00 / P02.09 (refer to jumper J35)

X3B 77	P2010 / SLSO06	I/O	3.3V	GPIO P20.10
X3B 78	P3315 / SLSO211	I/O	3.3V	GPIO P33.15
X3B 79	GND	-	-	Ground 0 V
X3B 80	P2003/SLSO29	I/O	3.3V	GPIO P20.03

Table 4: Pinout of the phyCORE-Connector X3, Row B (cont.)

Pin#	Signal	Signal Type	Signal Level	Description
X3C1	3V3	PWR_I	3.3V	Supply voltage +3.3 VDC
X3C2	3V3	PWR_I	3.3V	Supply voltage +3.3 VDC
X3C3	GND	-	-	Ground 0 V
X3C4	P2100 / X_ETH0_LED1	I/O	3.3V / ETH	Gbit Ethernet PHY LED1 (ACT) or GPIO P21.00 (refer to jumper J28)
X3C5	P2102	I/O	3.3V	GPIO P21.02
X3C6	VBAT_IN	I		Supply voltage for the RTC and Low Power SRAM data retention (refer to jumper J15, J16)
X3C7	GND	-	-	Ground 0 V
X3C8	RESOUT	O	3.3V	High active Reset-output, generated by inverting the /Reset output of the voltage supervisor U11 with FET Q3 **Caution: do not short the RESOUT Signal. It cause damage to the MOSFET Q3**
X3C9	/BOOT	I	3.3V	Following a power-on reset (/PORST), the Boot configuration of the processor is read over the inputs HWCFG[6..3]. /BOOT signal enables the possible to alter the default (start from internal Flash) HWCFG[4:5]= 11 /BOOT = float/High) to Generic Bootstrap (P14.0/1)) HWCFG[4:5]= 00 /BOOT = Low
X3C10	/HDRST	OC	3.3V	ESR0 Port Pin (default) Or /PORST (refer to jumper J9)
X3C11	/PORST	I	3.3V	Power-On Reset Input the boot configuration is fetched following a power-on reset
X3C12	GND	-	-	Ground 0 V

Pin#	Signal	Signal Type	Signal Level	Description
X3C13	P2200	I/O	3.3V	GPIO P22.00
X3C14	P3311	I/O	3.3V	GPIO P33.11
X3C15	P3312	I/O	3.3V	GPIO P02.03
X3C16	P2203	I/O	3.3V	GPIO P02.03
X3C17	GND	-	-	Ground 0 V
X3C18	CAN_H1 (P3401)	I/O	CAN_BUS	CANH output of the CAN transceiver for the CAN00 node **Alternative:** GPIO P34.01 (refer to jumper J60 and jumper J20)

Table 5: Pinout of the phyCORE-Connector X3, Row C

Pin#	Signal	Signal Type	Signal Level	Description
X3C19	P2204 / RxD7	I	3.3V	Receive line of the TC399 UART7 **Alternative:** GPIO P22.04. If the alternative function is used, Transceiver U2 should not be populated
X3C20	P2201 / TxD7	O	3.3V	Transmit line of the TC399 UART7. **Alternative:** GPIO P22.01 If the alternative function is used, Transceiver U2 should not be populated
X3C21	RXD7_RS232	O	RS232	RxD input of the RS-232 transceiver for the UART7 interface
X3C22	GND	-	-	Ground 0 V
X3C23	TXD7_RS232	O	RS232	TxD output of the RS-232 transceiver for the UART7 interface
X3C24	P1113 / SDA1	I/O	3.3V	GPIO P11.13
X3C25	P1114 / SCL1	I/O	3.3V	GPIO P11.14
X3C26	P1507 / MRST2	I/O	3.3V	GPIO P15.07
X3C27	GND	-	-	Ground 0 V
X3C28	P1506 / MTSR2	I/O	3.3V	GPIO P15.06
X3C29	P3314 / SCLK2	I/O	3.3V	GPIO P33.14
X3C30	5V_VBUS	PWR_I	5V	USB-VBUS (5V) input for opt. bus-powered USB to ASC0 Bridge (U7)
X3C31	P1504 / SCL0	O	3.3V	SCL I2C0 connected to onboard I2C-RTC U9
X3C32	GND	-	-	Ground 0 V
X3C33	E_/LINK	O	3.3V	Link Good signal from the on-board Ethernet Controller U21
X3C34	E_/SPEED	O	3.3V	Speed indication from the on-board Ethernet Controller U21
X3C35	E_RX-	ETH_I	ETH	RxD- input line of the on-board Ethernet Controller U21
X3C36	E_TX-	ETH_O	ETH	TxD- output line of the on-board Ethernet Controller U21
X3C37	GND	-	-	Ground 0 V
X3C38	NC	-	-	Not Connected
X3C39	P2001 / BRKIN	I	3.3V	OCDS Break Input
X3C40	P2000 / BRKOUT	I/O	3.3V	OCDS Break Out
X3C41	/TRST	I	3.3V	JTAG Reset Input
X3C42	GND	-	-	Ground 0 V
X3C43	CAN_L2 (P1501)	I/O	CAN_BUS	CANL output of the CAN transceiver for the CAN02 node. **Alternative:** GPIO P15.01 (refer to

				jumper J61 and jumper J22)
X3C44	CAN_H2 (P1500)	I/O	CAN_BUS	CANH output of the CAN transceiver for the CAN02 node. **Alternative:** GPIO P15.00 (refer to jumper J61 and jumper J21)
X3C45	CAN_L3(P3203)	I/O	CAN_BUS	CANL output of the CAN transceiver for the CAN03 node. **Alternative:** GPIO P32.03(refer to jumper J62 and jumper J25)
X3C46	P3308	I/O	3.3V	GPIO P33.08
X3C47	GND	-	-	Ground 0 V
X3C48	P3301	I/O	3.3V	GPIO P33.01
X3C49	P3302	I/O	3.3V	GPIO P33.02
X3C50	P1002/REQ2	I/O	3.3V	GPIO P10.02
X3C51	P3306	I/O	3.3V	GPIO P33.06
X3C52	GND	-	-	Ground 0 V
X3C53	AN21 /P1300/CAN10TX	I/O	3V3	Analog Input AN21 and GPIO P13.00 via R22
X3C54	AN23 /P1301/CAN10RX	I/O	3V3	Analog Input AN23 and GPIO P13.01 via R23
X3C55	AN28 / P1302	I/O	3V3	Analog Input AN28 and GPIO P13.02 via R24
X3C56	AN19 / P1303	I/O	3V3	Analog Input AN19 and GPIO P13.03 via R25
X3C57	GND	-	-	Ground 0 V
X3C58	AN18 / P2008/SLSO00	I/O	3V3	Analog Input AN18 and GPIO P20.08 via R26 GPIO P20.08 used as SLSO00 for onboard EEPROM U8 refer jumper J48
X3C59	AN17 / P2011	I/O	3V3	Analog Input AN17 and GPIO P20.11 via R27
X3C60	AN27 / P2012	I/O	3V3	Analog Input AN27 and GPIO P20.12 via R28

Table 5: Pinout of the phyCORE-Connector X3, Row C

Pin#	Signal	Signal Type	Signal Level	Description
X3C61	AN16 / P2014	I/O	3V3	Analog Input AN16 and GPIO P20.14 via R29
X3C62	AGND	-	-	Analog Ground 0 V
X3C63	AN15 / P3204	I/O	3V3	Analog Input AN15 and GPIO P32.04 via R30
X3C64	AN14 / P3205	I/O	3V3	Analog Input AN14 and GPIO P32.05 via R31
X3C65	AN13/ P3206/SLSO212	I/O	3V3	Analog Input AN13 and GPIO P32.06 via R32
X3C66	AN39 / P3207	I/O	3V3	Analog Input AN39 and GPIO P32.07 via R33

X3C67	AGND	-	-	Analog Ground 0 V
X3C68	AN10/ P1402/HWCFG2/SLSO21	I/O	3V3	Analog Input AN10 and GPIO P14.02 via R34 HWCFG3 (bootmode pin)
X3C69	AN25 / P0013	I/O	3V3	Analog Input AN39 and GPIO P00.13 via R35
X3C70	AN9 / P1404/HWCFG6	I/O	3V3	Analog Input AN10 and GPIO P14.02 via R36 HWCFG3 (bootmode pin)(refer to DIP-Switch S1)
X3C71	AN35 / P1410/TXDA	I/O	3V3	Analog Input AN35 and GPIO P14.10 via R51
X3C72	AGND	-	-	Analog Ground 0 V
X3C73	AN42 / P1406/TXENB	I/O	3V3	Analog Input AN42 and GPIO P14.06 via R52
X3C74	AN43 / P1408/RXDA0	I/O	3V3	Analog Input AN43 and GPIO P14.08 via R53
X3C75	AN7 / P0208	I/O	3V3	Analog Input AN7 and GPIO P02.08 via R54
X3C76	AN20 / P0209	I/O	3V3	Analog Input AN20 and GPIO P20.09 via R55
X3C77	AGND	-	-	Analog Ground 0 V
X3C78	AN2 / P0210	I/O	3V3	Analog Input AN2 and GPIO P02.10 via R56
X3C79	AN26 / P0211	I/O	3V3	Analog Input AN26 and GPIO P02.11 via R57
X3C80	AN1 / P0212	I/O	3V3	Analog Input AN1 and GPIO P02.08 via R58

Table 5: Pinout of the phyCORE-Connector X3, Row C (cont.)

Pin#	Signal	Signal Type	Signal Level	Description
X3D1	3V3	PWR_I	3V3	Supply voltage +3.3 VDC
X3D2	3V3	PWR_I	3V3	Supply voltage +3.3 VDC
X3D3	GND	-	-	Ground 0 V
X3D4	P2101 / X_ETH0_LED0	I/O	3.3V	Gbit Ethernet PHY LED0 (LINK) or GPIO P21.01 (refer to jumper J29)
X3D5	P2103	I/O	3.3V	GPIO P21.03
X3D6	P2104	I/O	3.3V	GPIO P21.04
X3D7	P2105	I/O	3.3V	GPIO P21.05
X3D8	P2202	I/O	3.3V	GPIO P22.02
X3D9	GND	-	-	Ground 0 V
X3D10	/RESIN	I	3.3V	Reset input, controls the system reset /PORST
X3D11	P1007/REQ0	I/O	3.3V	GPIO P10.07
X3D12	P1008/REQ1	I/O	3.3V	GPIO P10.08
X3D13	P2000/REQ6	I/O	3.3V	GPIO P20.00
X3D14	GND	-	-	Ground 0 V

Pin#	Signal	Signal Type	Signal Level	Description
X3D15	P2009/SLSI0/REQ7	I/O	3.3V	GPIO P20.09
X3D16	RxD0	I	3.3V	Receive line of the TC399 UART0. **Alternative:** GPIO P14.01 If the alternative function is used, Transceiver U2 should not be populated (refer to jumper J3)
X3D17	TxD0	O	3.3V	Transmit line of the TC399 UART0. **Alternative:** GPIO P14.00. If the alternative function is used, Transceiver U2 should not be populated (refer to jumper J3)
X3D18	CAN_L1 (P3402)	I/O	CAN_BUS	CANL output of the CAN transceiver for the CAN00 node. **Alternative:** GPIO P34.02. (refer to jumper J60 and jumper J24)

Table 6: Pinout of the phyCORE-Connector X3, Row D

Pin#	Signal	Signal Type	Signal Level	Description
X3D19	GND	-	-	Ground 0 V
X3D20	CAN_L0 (P1401)	I/O	CAN_BUS	CANL output of the CAN transceiver for the CAN01 node. **Alternative:** GPIO P14.01 (refer to jumper J59 and jumper J19)
X3D21	CAN_H0 (P1400)	I/O	CAN_BUS	CANR output of the CAN transceiver for the CAN01 node. **Alternative:** GPIO P14.00 (refer to jumper J59 and jumper J18)
X3D22	RXD0_RS232	I	RS232	RxD input of the RS-232 transceiver for the UART0 interface
X3D23	TXD0_RS232	O	RS232	TxD output of the RS-232 transceiver for the UART0 interface
X3D24	GND	-	-	Ground 0 V
X3D25	P3310	I/O	3.3V	GPIO P33.10
X3D26	P3313/SLSO213	I/O	3.3V	GPIO P33.13
X3D27	P2206/MRST0	I	3.3V	MISO SPI0 TC399 connected to onboard SPI-EEPROM U8

X3D28	P2205/MTSR0	O	3.3V	MOSI SPI0 TC399 connected to onboard SPI-EEPROM U8
X3D29	GND	-	-	Ground 0 V
X3D30	P2207/SCLK0	O	3.3V	SCLK SPI0 TC399 connected to onboard SPI-EEPROM U8
X3D31	P2211/SLSO010	I/O	3.3V	GPIO P33.10
X3D32	P1505/SDA0	I/O	3.3V	SDA I2C0 connected to onboard I2C-RTC U9
X3D33	/IRQRTC	OC	3.3V	RTC interrupt output
X3D34	GND	-	-	Ground 0 V
X3D35	E_RX+	ETH_I	ETH	RxD+ input of the Ethernet Controller U21
X3D36	E_TX+	ETH_O	ETH	TxD+ output of the Ethernet Controller U21
X3D37	USB_D+	USB_I/O	USB	USB D+ data line from opt bus-powered USB <-> ASC0 converter (U7)
X3D38	USB_D-	USB_I/O	USB	USB D- data line from opt bus-powered USB <-> ASC0 converter (U7)
X3D39	GND	-	-	Ground 0 V
X3D40	P2106/TDI	I	3.3V	JTAG Data Input
X3D41	TDO/DAP2	O	3.3V	JTAG Data Output
X3D42	TMS/DAP1	I	3.3V	JTAG State Machine Control / DAP: DAP1 Data I/O
X3D43	TCK/DAP0	I	3.3V	JTAG Module Clock Input / DAP: DAP0 Clock Input
X3D44	GND	-	-	Ground 0 V
X3D45	CAN_H3 (P3202)	I/O	CAN_BUS	CANL output of the CAN transceiver for the CAN03 node. **Alternative:** GPIO P32.02 (refer to jumper J62 and jumper J23)
X3D46	P3309	I/O	3.3V	GPIO P33.09
X3D47	P3300	I/O	3.3V	GPIO P33.00
X3D48	P3303	I/O	3.3V	GPIO P33.03
X3D49	GND	-	-	Ground 0 V
X3D50	P1003/REQ3	I/O	3.3V	GPIO P10.03
X3D51	P3304	I/O	3.3V	GPIO P33.03
X3D52	AN24 / P3404	I/O	3.3V	Analog Input AN24 and GPIO P34.04 via R37
X3D53	AN30 / P3405	I/O	3.3V	Analog Input AN30 and GPIO P34.05 via R38
X3D54	GND	-	-	Ground 0 V
X3D55	AN8 / P2208/CAN22TX	I/O	3.3V	Analog Input AN8 and GPIO P22.08 via R39
X3D56	AN12 / P2209/CAN22RX	I/O	3.3V	Analog Input AN12 and GPIO P22.09 via R40
X3D57	AN36 / P2210	I/O	3.3V	Analog Input AN63 and GPIO P22.10 via R41
X3D58	AN37 /	I/O	3.3V	Analog Input AN37 and

	P1115			GPIO P11.15 via R42
X3D59	AGND	-	3.3V	Analog Ground 0 V
X3D60	VAREF2	REF_I	3.3V	ADC Analog Reference Voltage VAREF2 connected onboard to 3.3V (Refer to jumper J63)
X3D61	AN29 / P1000	I/O	3.3V	Analog Input AN29 and GPIO P10.00 via R43 P10.00 used for onboard red LED D1 refer to jumper J39

Table 6: Pinout of the phyCORE-Connector X3, Row D

Pin#	Signal	Signal Type	Signal Level	Description
X3D62	AN22 / P1001	I/O	3.3V	Analog Input AN22 and GPIO P10.01 via R44
X3D63	AN0 / P1004	I/O	3.3V	Analog Input AN0 and GPIO P10.04 via R45
X3D64	AGND	-	-	Analog Ground 0 V
X3D65	AN5 / P1005/HWCFG4	I/O	3.3V	Analog Input AN5 and GPIO P10.05 via R46
X3D66	AN38 / P1006/HWCFG5	I/O	3.3V	Analog Input AN38 and GPIO P10.06 via R47
X3D67	AN11 / P3200	I/O	3.3V	Analog Input AN11 and GPIO P32.00 via R48
X3D68	AN33 / P3201	I/O	3.3V	Analog Input AN33 and GPIO P32.01 via R49
X3D69	AGND	-	3.3V	Analog Ground 0 V
X3D70	AN31 / P0014	I/O	3.3V	Analog Input AN31 and GPIO P00.14 via R50
X3D71	AN32 / P1407/RXDB0	I/O	3.3V	Analog Input AN32 and GPIO P14.07 via R59
X3D72	AN40 / P1405/HWCFG1/TXDB	I/O	3.3V	Analog Input AN40 and GPIO P14.05 via R60
X3D73	AN41 / P1409/TXENA	I/O	3.3V	Analog Input AN41 and GPIO P14.09 via R61
X3D74	AGND	-	-	Analog Ground 0 V
X3D75	AN6 / P0015	I/O	3.3V	Analog Input AN6 and GPIO P00.15 via R62
X3D76	AN4 / P0213	I/O	3.3V	Analog Input AN4 and GPIO P02.13 via R63
X3D77	AN3 / P0214	I/O	3.3V	Analog Input AN3 and GPIO P02.14 via R64
X3D78	AN34 / P0215	I/O	3.3V	Analog Input AN34 and GPIO P02.15 via R65
X3D79	AGND	-	-	Analog Ground 0 V
X3D80	VAREF1	REF_I	3.3V	ADC Analog Reference Voltage VAREF1 connected onboard to 3.3V(Refer to jumper J63)

Table 6: Pinout of the phyCORE-Connector X3, Row D (cont.)

Pin#	Signal	Signal	Signal Level	Description

		Type		
X2A1	P1510/MRST5	I/O	*3.3V*	GPIO P15.10
X2A2	P1512/CD	I/O	*3.3V*	GPIO P15.12
X2A3	GND	-	-	Ground 0 V
X2A4	P1515/SCLK5	I/O	*3.3V*	GPIO P1515
X2A5	P1411	I/O	*3.3V*	GPIO P14.11
X2A6	P1413	I/O	*3.3V*	GPIO P14.13
X2A7	GND	-	-	Ground 0 V
X2A8	P1304/CAN23_TX	I/O	*3.3V*	GPIO P13.04
X2A9	P1306	I/O	*3.3V*	GPIO P13.06
X2A10	P1307	I/O	*3.3V*	GPIO P13.07
X2A11	P1310	I/O	*3.3V*	GPIO P13.10
X2A12	GND	-	-	Ground 0 V
X2A13	P1313	I/O	*3.3V*	GPIO P13.13
X2A14	P1315	I/O	*3.3V*	GPIO P13.15
X2A15	P1009	I/O	*3.3V*	GPIO P10.09
X2A16	P1011	I/O	*3.3V*	GPIO P10.11
X2A17	GND	-	-	Ground 0 V
X2A18	P1015	I/O	*3.3V*	GPIO P10.15
X2A19	P0101	I/O	*3.3V*	GPIO P01.01
X2A20	P0102	I/O	*3.3V*	GPIO P01.02
X2A21	P0109	I/O	*3.3V*	GPIO P01.09
X2A22	GND	-	-	Ground 0 V
X2A23	P0112	I/O	*3.3V*	GPIO P01.12
X2A24	P0114	I/O	*3.3V*	GPIO P01.14
X2A25	P0115	I/O	*3.3V*	GPIO P0.115
X2A26	NC		-	

Table 7: Pinout of the optional phyCORE-Connection X2, Row A

Pin#	Signal	Signal Type	Signal Level	Description
X2A27	AGBT_CLKP (GND)	I (-)	-	Ground 0 V Emulation Device:AGBT
X2A28	AGBT_CLKN (GND)	I (-)	-	Ground 0 V Emulation Device:AGBT
X2A29	DAPE0_EMU (NC)	I (-)	-	Not Connected Emu. Emulation Device:AGBT
X2A30	DAPE2_EMU (NC)	I/O (-)	-	Not connected Emulation Device:AGBT
X2A31	NC	-	-	NOT CONNECTED
X2A32	AGND	-	-	Analog Ground 0 V
X2A33	AN46	I	*3.3V*	Analog Input AN46
X2A34	AN48	I	*3.3V*	Analog Input AN48
X2A35	AN72	I	*3.3V*	Analog Input AN72
X2A36	AN70	I	*3.3V*	Analog Input AN70
X2A37	AGND	-	-	Analog Ground 0 V
X2A38	AN68	I	*3.3V*	Analog Input AN68
X2A39	AN66	I	*3.3V*	Analog Input AN66
X2A40	AN64	I	*3.3V*	Analog Input AN64
X2A41	AN62	I	*3.3V*	Analog Input AN62
X2A42	AGND	-	-	Analog Ground 0 V
X2A43	AN60	I	*3.3V*	Analog Input AN60
X2A44	AN58	I	*3.3V*	Analog Input AN58
X2A45	AN56	I	*3.3V*	Analog Input AN56
X2A46	AN54	I	*3.3V*	Analog Input AN54

X2A47	AGND	-	-	Analog Ground 0 V
X2A48	AN52	I	*3.3V*	Analog Input AN52
X2A49	AN50	I	*3.3V*	Analog Input AN50
X2A50	AN49	I	*3.3V*	Analog Input AN49

Table 7: Pinout of the optional phyCORE-Connection X2, Row A (cont.)

Pin#	Signal	Signal Type	Signal Level	Description
X2B1	P1511/SLSO52	I/O	*3.3V*	GPIO P15.11
X2B2	P1513	I/O	*3.3V*	GPIO P15.13
X2B3	P1514/MTSR5	I/O	*3.3V*	GPIO P15.14
X2B4	GND	-	-	Ground 0 V
X2B5	P1412	I/O	*3.3V*	GPIO P14.12
X2B6	P1414	I/O	*3.3V*	GPIO P14.14
X2B7	P1415	I/O	*3.3V*	GPIO P14.15
X2B8	P1305/CAN23_RX	I/O	*3.3V*	GPIO P13.05
X2B9	GND	-	-	Ground 0 V
X2B10	P1309/CAN21_TX	I/O	*3.3V*	GPIO P13.09
X2B11	P1311	I/O	*3.3V*	GPIO P13.11
X2B12	P1312/CAN21_RX	I/O	*3.3V*	GPIO P13.12
X2B13	P1314	I/O	*3.3V*	GPIO P13.14
X2B14	GND	-	-	Ground 0 V
X2B15	P1010	I/O	*3.3V*	GPIO P10.10
X2B16	P1013	I/O	*3.3V*	GPIO P10.13
X2B17	P1014	I/O	*3.3V*	GPIO P10.14
X2B18	P0100	I/O	*3.3V*	GPIO P01.00
X2B19	GND	-	-	Ground 0 V
X2B20	P0108	I/O	*3.3V*	GPIO P10.10
X2B21	P0110	I/O	*3.3V*	GPIO P10.13
X2B22	P0111	I/O	*3.3V*	GPIO P10.14
X2B23	P0113	I/O	*3.3V*	GPIO P01.00
X2B24	GND	-	-	Ground 0 V
X2B25	NC	-	-	NOT CONNECTED

Table 8: Pinout of the optional phyCORE-Connection X2, Row B

Pin#	Signal	Signal Type	Signal Level	Description
X2B26	NC	-	-	NOT CONNECTED
X2B27	AGBT_TX0N (GND)	O (-)	-	Ground 0 V Emu. Device:AGBT
X2B28	AGBT_TX0P (GND)	O (-)	-	Ground 0 V Emu. Device:AGBT
X2B29	AGBT_ERR (GND)	I (-)	-	Ground 0 V Emu. Device:AGBT
X2B30	DAPE1_EMU (NC)	I/O (-)	-	Ground 0 V Emu. Device:AGBT
X2B31	AN44	I	*3.3V*	Analog Input AN49
X2B32	AN45	I	*3.3V*	Analog Input AN49
X2B33	AN47	I	*3.3V*	Analog Input AN49
X2B34	AGND	-	-	Analog Ground 0 V
X2B35	AN73	I	*3.3V*	Analog Input AN49
X2B36	AN71	I	*3.3V*	Analog Input AN49
X2B37	AN69	I	*3.3V*	Analog Input AN49
X2B38	AN67	I	*3.3V*	Analog Input AN49

X2B39	AGND	-	-	Analog Ground 0 V
X2B40	AN65	I	*3.3V*	Analog Input AN49
X2B41	AN63	I	*3.3V*	Analog Input AN49
X2B42	AN61	I	*3.3V*	Analog Input AN49
X2B43	AN59	I	*3.3V*	Analog Input AN49
X2B44	AGND	-	-	Analog Ground 0 V
X2B45	AN57	I	*3.3V*	Analog Input AN49
X2B46	AN55	I	*3.3V*	Analog Input AN49
X2B47	AN53	I	*3.3V*	Analog Input AN49
X2B48	AN51	I	*3.3V*	Analog Input AN49
X2B49	AGND	-	-	Analog Ground 0 V
X2B50	VAREF3	REF_I	3.3V	ADC Analog Reference Voltage VAREF3 connected onboard to 3.3V (Refer to jumper 63)

Table 8: Pinout of the optional phyCORE-Connection X2, Row B (cont.)

3 Jumpers

For configuration purposes, the phyCORE-TC399 has several solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while Figure 6 and *Figure 7* indicate the location and the default configuration of the solder jumpers on the board.

Table 9 provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-TC399 to specific design needs. It shows their default positions and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCORE-TC399.

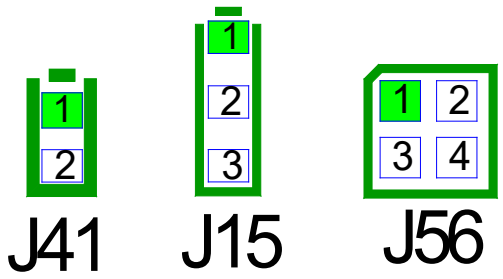


Figure 5: Typical Jumper Pad Numbering Scheme

Note:
Pin 1 on each jumper is identified by a light green box.

If manual jumper modification is required, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered jumpers need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, hot air rework station or other desoldering method is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

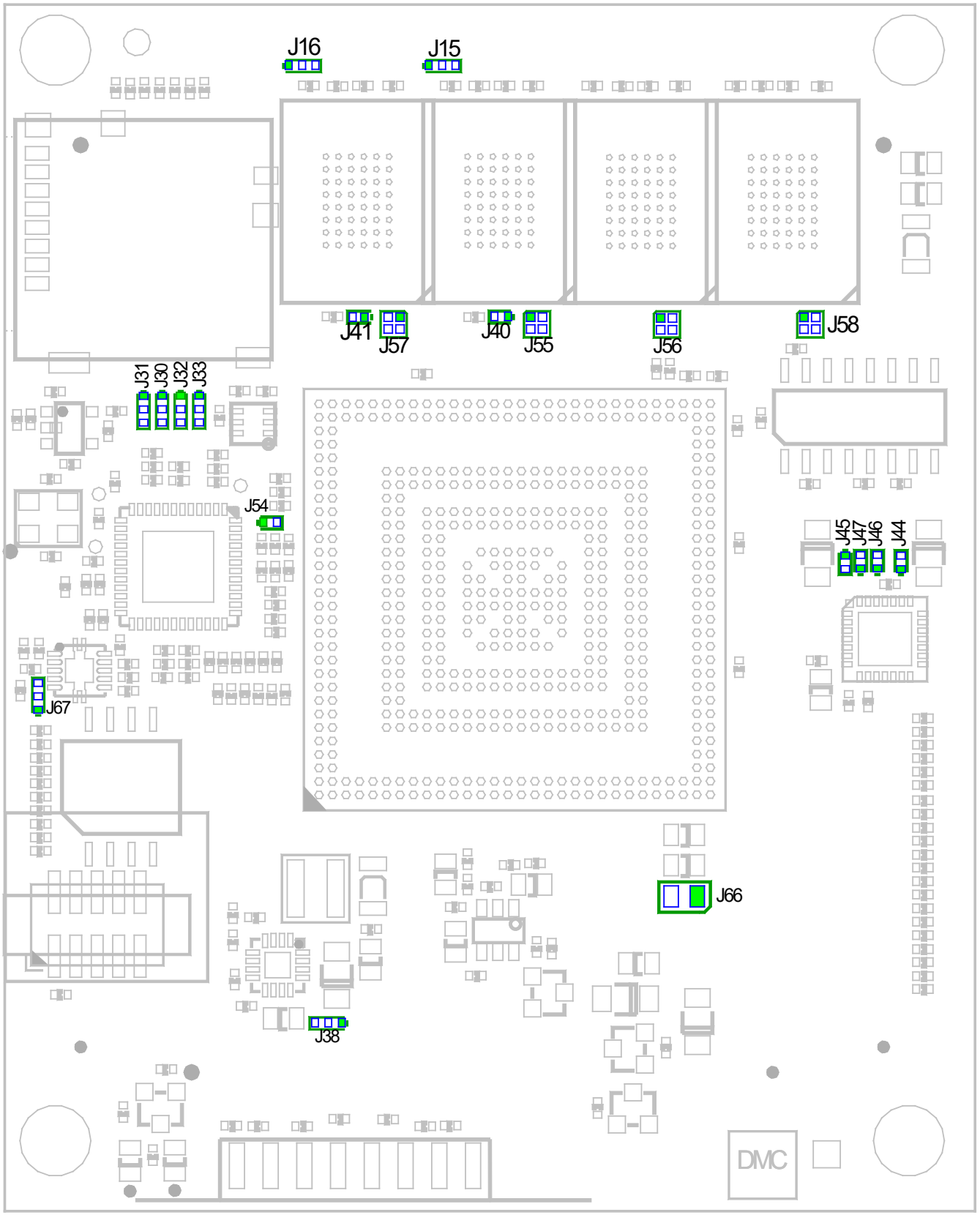


Figure 6: Jumper Locations (top view)

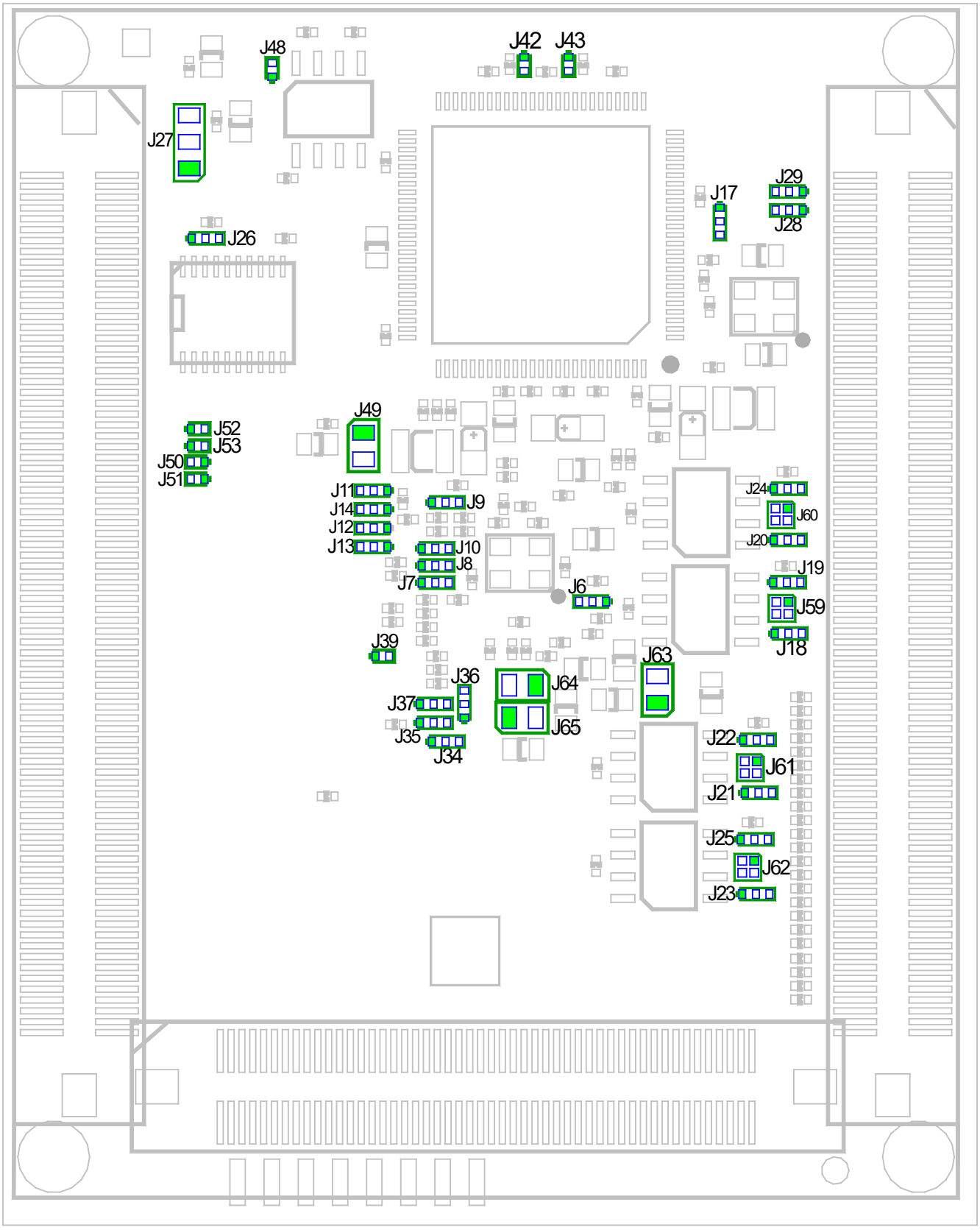


Figure 7: Jumper Locations (bottom view)

Please pay special attention to the "TYPE" column to ensure the correct type of jumper (0 Ohms, 10k Ohms, etc…) are

used. The jumpers are 0402 package with a 1/8 W or better power rating.

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	See Section
J6	Standby Power Supply VEVRSB for TC399 Standby SRAM	0 Ω (0402)	
1+2	**VEVRSB = 3V3**		
2+3	VEVRSB = 3,3V or VBAT_IN		
J7	TC399 ball M15 routing	0 Ω (0402)	
1+2	**TC399 ball M15 is connected to GND**		
2+3	TC399 ball M15 is exposed to X2pin30A (Emulation Device only)		
J8	TC399 ball M16 routing	0 Ω (0402)	
1+2	**TC399 ball M16 is connected to GND**		
2+3	TC399 ball M16 is exposed to X2pin30A (Emulation Device only)		
J9	Periphial ResetOut /HDRST **Reserved, Do not change !**	0 Ω (0402)	
1+2	**/HDRST = /ESR0**		
2+3	/PORST		
J10	TC399 ball R19 routing	0 Ω (0402)	
1+2	TC399 ball R19 is exposed to X2pin30A (emulation Device only)		
2+3	**Reserved, Do not change**		
open	**TC399 ball R19 is not connected**		
J11	P1502 routing	0 Ω (0402)	
1+2	**P1502 used as CAN01_TX**		
2+3	P1502 used as TxD0		
J12	P1503 routing	0 Ω (0402)	
1+2	**P1503 used as CAN01_RX**		
2+3	P1503 used as RxD0		
J13	P1401 routing Generic ASC/CAN_Bootloader Mode	0 Ω (0402)	
1+2	P1401 used as CAN01_RX		
2+3	**P1401 used as RxD0**		
J14	P1400 routing Generic ASC/CAN_Bootloader Mode	0 Ω (0402)	
1+2	P1400 used as CAN01_TX		

2+3	**P1400 used as TxD0**		

Table 9: Jumper Settings

Jumper	Description	Type	See Section
J15	Supply for the SRAM BANK1 (U17/U18)	0 Ω (0402)	
1+2	**SRAM- BANK1 supply is only 3,3V (for HS-SRAM)**		
2+3	SRAM- BANK1 supply is 3,3V or VBAT_IN for LP- SRAM		
J16	supply for the SRAM BANK2 (U19/U20)	0 Ω (0402)	
1+2	**SRAM- BANK2 supply is only 3,3V (for HS-SRAM)**		
2+3	SRAM- BANK2 supply is 3,3V or VBAT_IN for LP- SRAM		
J17	Connects speed or transmit Ethernet indication to X3-34C	0 Ω (0402)	
1+2	**Connect SPD_LED (U21) signal to phyCORE-molex connector X3-34C**		
2+3	Connect TX_LED (U21) signal to phyCORE-molex connector X3-34C		
J18	CAN_TX selection for U3	0 Ω (0402)	
1+2	**CAN01_TX (refer J11/J14) is connected to CAN transceiver U3 and J59**		
2+3	P1300 is connected to CAN transceiver U3 and J59		
J19	CAN_RX selection for U3	0 Ω (0402)	
1+2	**CAN01_RX (refer J12/J13) is connected to CAN transceiver U3 and J59**		
2+3	P1301 is connected to CAN transceiver U3 and J59		
J20	CAN_TX selection for U4	0 Ω (0402)	
1+2	**CAN00_TX is connected to CAN transceiver U4 and J60**		
2+3	P1309 is connected to CAN transceiver U4 and J60		
J21	CAN_TX selection for U5	0 Ω (0402)	
1+2	**CAN02_RX is connected to CAN transceiver U5 and J61**		

2+3	P1304 is connected to CAN transceiver U5 and J61		

Table 9: Jumper Settings (cont.)

Jumper	Description	Type	See Section
J22	CAN_RX selection for U4	0 Ω (0402)	
1+2	**CAN02_RX is connected to CAN transceiver U5 and J61**		
2+3	P1305 is connected to CAN transceiver U5 and J61		
J23	CAN_TX selection for U6	0 Ω (0402)	
1+2	**CAN03_TX is connected to CAN transceiver U6 and J62**		
2+3	P2208 is connected to CAN transceiver U6 and J62		
J24	CAN_RX selection for U4	0 Ω (0402)	
1+2	**CAN00_RX is connected to CAN transceiver U4 and J60**		
2+3	P1312 is connected to CAN transceiver U4 and J60		
J25	CAN_RX selection for U6	0 Ω (0402)	
1+2	**CAN03_RX is connected to CAN transceiver U6 and J62**		
2+3	P2209 is connected to CAN transceiver U6 and J62		
J26	clockout function of the RTC at U9	0 Ω (0402)	
1+2	**RTC-Clockout disabled**		
2+3	RTC-Clockout enabled		
J27	Pin X3-B1 signal connection	0 Ω (0805)	
1+2	**RTC U9 CLKOUT is connected to X3-B1**		
2+3	1.25V MCU core Supply input pin J27=2+3 only if on-board Regulator U10 for 1V25V not populated		
J28	Pin X3-C4 signal connection	0 Ω (0402)	
1+2	P2100 is connected to X3-C4		

2+3	**X_ETH0_LED1 (ACT) is connected to X3-C4**		

Table 9: Jumper Settings (cont.)

Jumper	Description	Type	See Section
J29	Pin X3-D4 signal connection	0 Ω (0402)	
1+2	P2101 is connected to X3-D4		
2+3	**X_ETH0_LED0 (LINK) is connected to X3-D4**		
J30	Pin X3-A25 signal connection	0 Ω (0402)	
1+2	EBU address line A18 connected to X3-25A		
2+3	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_DP connected to X3-25A**		
J31	Pin X3-A24 signal connection	0 Ω (0402)	
1+2	EBU address line A17 connected to X3-24A		
2+3	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_DN connected to X3-24A**		
J32	Pin X3-B23 signal connection	0 Ω (0402)	
1+2	EBU address line A16 connected to X3-23B		
2+3	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_BN connected to X3-23B**		
J33	Pin X3-B25 signal connection	0 Ω (0402)	
1+2	EBU address line A19 connected to X3-25B		
2+3	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_BP connected to X3-25B**		
J34	Pin X3-A71 signal connection	0 Ω (0402)	
1+2	**P0204 is connected to X3-71A**		
2+3	P0208 is connected to X3-71A		
J35	Pin X3-B71 signal connection	0 Ω (0402)	
1+2	**P0201 is connected to X3-71B**		
2+3	P0211 is connected to X3-71B		

J36	Pin X3-A76 signal connection	0 Ω (0402)	
1+2	**P0207 is connected to X3-76A**		
2+3	P0210 is connected to X3-76A		
J37	Pin X3-B76 signal connection	0 Ω (0402)	
1+2	**P0200 is connected to X3-76B**		
2+3	P0209 is connected to X3-76B		
J38	Enable/disable regulator U10	0 Ω (0402)	
1+2	**Enable Voltage regulator U10 for 1.25V CPU Core supply**		
2+3	disable Voltage regulator U10 for 1.25V MCU Core supply		

Table 9: Jumper Settings (cont.)

Jumper	Description	Type	See Section
J39	P10.00 connection to red LED D1	0 Ω (0402)	
closed	**P1000 is connected to on-board red LED D1**		
open	P1000 is NOT connected to on-board red LED D1		
J40	/CS0 connection to SRAM U17/18	0 Ω (0402)	
closed	**/CS0 connected to onboard SRAM BANK1 memory U17/U18**		
open	/CS1 is freely usable on X3		
J41	/CS1 connection to SRAM U19/20	0 Ω (0402)	
closed	**/CS1 connected to onboard SRAM BANK2 memory U19/U20**		
open	/CS1 is freely usable on X3		
J42	/CS2 connection to ETH Contr.U21	0 Ω (0402)	
closed	**/CS2 connected to onboard 10/100Mbit Ethernet Controller U21**		
open	/CS2 is freely usable on X3		
J43	P3307 as IRQ for ETH Contr.U21	0 Ω (0402)	
closed	**P3307/REQ4 connected to IRQ-output Ethernet controller U21**		
open	P3307 is freely usable on X3		
J44	/Boot Signal connection to U7	0 Ω (0402)	
closed	/BOOT Signal is connected to onboard USB-UART Bridge-RTS-output		
open	**/BOOT Signal is NOT connected to onboard USB-UART Bridge-RTS-output**		
J45	/PORST Signal connection to U7	0 Ω	

closed	/PORST Signal is connected to onboard U7 USB-UART Bridge-DTR-output	(0402)	
open	**/PORST Signal is NOT connected to onboard U7 USB-UART Bridge-RTS- output**		
J46	TXD Signal connection to U7	0 Ω (0402)	
closed	*TxD0 Signal is connected to onboard U7 USB-UART Bridge-Rxd-input*		
open	**TxD0 Signal is NOT connected to onboard U7 USB-UART Bridge-Rxd-input**		
J47	RXD Signal connection to U7	0 Ω (0402)	
closed	RxD0 Signal is connected to onboard U7 USB-UART Bridge-Txd-output		
open	**RxD0 Signal is NOT connected to onboard U7 USB-UART Bridge-Txd-output**		

Table 9: Jumper Setting (cont.)

Jumper	Description	Type	See Section
J48	P2008/SLSO00 connection to U8	0 Ω (0402)	
closed	**P2008/SLSO00 is connected to /CS input of SPI-EEPROM U8**		
open	P2008/SLSO00 is freely usable on X3		
J49	Pin X3-A1 connection	0 Ω (0805)	
closed	X3A1 Pin is connected to MCU Core supply 1V25. J49=1+2 only if onBoard Regulator U10 for 1V25V not populated		
open	**X3A1 Pin is not connected Pin**		
J50	Pin X3-A26 signal connection	0 Ω (0402)	
closed	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_CN connected to X3-26A**		
open	X3-26A Pin is not connected		
J51	Pin X3-A28 signal connection	0 Ω (0402)	
closed	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_CP connected to X3-28A**		

open	X3-28A Pin is not connected		
J52	Pin X3-B26 signal connection	0 Ω (0402)	
closed	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_AN connected to X3-26B**		
open	X3-26B Pin is not connected		
J53	Pin X3-B27 signal connection	0 Ω (0402)	
closed	**Gbit Ethernet Differential Transmit and Receive Signal X_ETH0_AP connected to X3-27B**		
open	X3-27B Pin is not connected		
J54	P1508 as IRQ for GbETH Contr.U12	0 Ω (0402)	
closed	**P1508/REQ5 connected to IRQ-output Ethernet controller U12**		
open	P1508/REQ5 is freely usable on X3		
J55 J56	These jumpers configure the correct byte control signals being used on the MCU depending on the SRAM devices. SRAM BANK1 (U17/U18) populating the module.	0 Ω (0402)	
1+2	**Reserved, Do not change !**		
3+4	**Reserved, Do not change !**		

Table 9: Jumper Setting (cont.)

Jumper	Description	Type	See Section
J57 J58	These jumpers configure the correct byte control signals being used on the MCU depending on the SRAM devices. SRAM BANK1 (U19/U20) populating the module.	0 Ω (0402)	
1+2	**Reserved, Do not change !**		
3+4	**Reserved, Do not change !**		

J59 **J60** **J61** **J62**	These jumpers connect the TTL_CAN signals with the phyCORE connector pins, for connection to external CAN transceivers, or if CAN outputs are used as standard port pins U3 => CAN Node 0; U4 => CAN Node 1 U5 => CAN Node 2; U6 => CAN Node 3	0 Ω (0402)	
1+2 3+4	The on-board CAN transceivers U3, U4, U5, U6 are used.		
open	**On-board CAN Transceiver is used**		
J63	TC399 ADC supply VDDM connection	0 Ω (0805)	
closed	**ADC analog supply voltage VDDM connected to 3.3V**		
open	ADC analog supply voltage VDDM must be supplied VAREF1 or VAREF2 or VAREF3 dependig on jumper settings J64 / J65 / 66 closed		
J64	onboard TC399 VAREF1 connection	0 Ω (0805)	
closed	**VAREF1 connected to ADC analog supply voltage VDDM. VAREF1 can supply VDDM with 3.3V/5V if J63 is open**		
open	VAREF1 = reference input only		
J65	onboard TC399 VAREF2 connection	0 Ω (0805)	
closed	**VAREF2 connected to ADC analog supply voltage VDDM. VAREF3 can supply VDDM with 3.3V/5V if J63 is open**		
open	VAREF2 = reference input only		
J66	onboard TC399 VAREF3 connection	0 Ω (0805)	
closed	**VAREF3 connected to ADC analog supply voltage VDDM. VAREF3 can supply VDDM with 3.3V/5V if J63 is open**		
open	VAREF2 = reference input only		
J67		0 Ω (0402)	
1+2	**Enable Voltage regulator U15 1.0V Gbit PHY supply**		
2+3	Disable voltage regulator U15		

Table 9: Jumper Setting (cont.)

4 Power

The phyCORE-TC399 operates off of a primary voltage supply with a nominal value of +3.3 V. On-board switching regulators generate the 2.5 V, 1.25 V, and 1 V voltage supplies required by the TC399 MCU and on-board components from the primary 3.3 V supplied to the SOM.

For proper operation, the phyCORE-TC399 must be supplied with a voltage source of 3.3 V (±5%) with 2.5 A load at the VCC pins on the phyCORE-Connector X3.

3V3: -> X3 -> C1, C2, D1, D2

Connect all +3.3 V VCC input pins to your power supply and, at minimum, the matching number of GND pins.

Corresponding GND: -> X3 -> C3, D3, C7, D9

Please refer to *Section 2* for information on additional GND Pins located at the phyCORE-Connector X3.

Caution!
As a general design rule, PHYTEC recommends connecting all GND pins which are next to signals that are being used in the application circuitry. For maximum EMI performance, all GND pins should be connected to a solid ground plane.

4.1 Standby Power Supply

In some applications, it is desirable to disconnect all supply voltages from the module, but still maintain certain data in the volatile memory.

For such cases, the phyCORE-TC399 offers the input pin VBAT_IN (X3C6). If a voltage of 3.1 V is supplied over VBAT_IN, the data is maintained in the RTC and, depending on the hardware configuration, in the SRAM memory device mounted at BANK1 U17/U18 or BANK2 U19 /U20 (refer to jumpers J15 and J16). The data will remain even if all other supply voltages have been turned off.

Connecting a battery via the VBAT_IN input is not mandatory for normal operation of the module, since all devices listed above are supplied with power by the module's operating voltage 3V3.

5 Reset

The input voltages, 3V3, and the on-board generated operation voltage, VCC_1V25, are monitored by a voltage supervisor device at U11.

Once all voltages have reached their target level, the voltage supervisory circuit keeps the /PORST reset signal at low level (low is the active level) for an additional 140ms. Then the /PORST signal switches to high level (inactive) and the MCU boot sequence starts.

6 System Configuration and Booting

Although most features of the phyCORE-TC399 microprocessor are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The phyCORE-TC399 supports the start-up modes detailed in the following sections.

6.1 Internal start

In this basic startup mode, the first user instruction is fetched from the Internal Program Flash of the device. The user code start address, defined as STADD, is configurable in the Boot Mode Header (BMHDx.STAD) data structure.

6.2 Bootloader Modes

1) ASC Bootloader
2) CAN Bootloader

6.2.1 Alternate Boot Modes (ABM)

Boot only if all defined conditions are satisfied.

If mode selection by HWCFG pins is enabled(BMHDx.PINDIS=0), the DIP Switch S1 (see *Figure 2*) on the phyCORE-TC399 can be used to select the desired boot source

S1.0	HWCFG3	0 - Boot from pins HWCFG [5:4] 1 - Flash BMI boot
S1.2/3	HWCFG4/5	Refer to *Table 11*
S1.4	HWCFG6	Default Pad state: • 0 - Pins in tristate • 1 - Pins with pull-up

Table 10: DIP Switch S1 Modes

S1[4:0] (on=0; off=1)	HWCFG [4]	HWCFG [5]	Boot Source
on,on,on,on	0	0	Generic Bootstrap (P14.0/1)
	0	1	ABM, Generic Bootstrap on fail (P14.0/1
	1	0	ABM, ASC Bootstrap on fail (P15.2/3)
on,off,off,on	**1**	**1**	Internal start from Flash

Table 11: Boot Modes of the phyCORE-TC399

Caution!
Please make sure that the signals shown in are not driven by any device on the baseboard during reset. This is to avoid accidental change of the boot configuration.

Configuration Pin	Pin #	Signal Default	Description
P1405/HWCFG1/TXDB	72D	1k5 PD	if R60 is populated
P1402/HWCFG2/SLSO21	68C	1k5 PD	if R34 is populated
P1403/HWCFG3/SLSO23	3B	10k PU or 1k5 PD	
P1005/HWCFG4	65D	10k PU or 1k5 PD	if R46 is populated
P1006/HWCFG5	66D	10k PU or 1k5 PD	if R47 is populated
P1404/HWCFG6	70C	10k PU or 1k5 PD	if R36 is populated

Table 12: Boot Configuration Pins at the phyCORE-Connector

7 System Memory

The phyCORE-TC399 system memory consist of internal TC399 Flash memory, external standard asynchronous SRAM, and SPI-Flash/EEPROM:

- up to 16 Mbyte internal TC399 Flash
- up to 4 Mbyte external asynchronous high Speed SRAM_BANK1
- up to 4 Mbyte external asynchronous high Speed SRAM_BANK2
- SPI-EEPROM/Flash - up to 32kB EEPROM or max. 2Mbyte Flash

The following sections detail each memory type used on the phyCORE-TC399.

7.1 External Asynchronous SRAM_BANK 1 and 2 (U17-U20))

The RAM memory of the phyCORE-TC399 is comprised of two SRAM BANKS with a capacity of up to 4MByte for each BANK. The chips are connected to the External Bus Interface (EBU) of the TC399 microcontroller.

The SRAM initialization is performed by software using the internal registers of the TC399.
When writing custom code, the RAM must be initialized by accessing the appropriate EBU configuration registers on the TC399 controller. Refer to the *TC399 Reference Manual* for accessing and configuring these registers.

The SRAM BANK1 (U17/U18) is controlled by /CS0 with 32-bit bus width. The SRAM BANK2 (U19/U20) is controlled by /CS1 with 32-bit bus width.

7.2 SPI EEPROM Flash Memory (U8)

The phyCORE-TC399 features a non-volatile memory with an SPI interface. This memory can be used to store configuration data or operating parameters that must not be lost in the event of a power interruption. Depending on the module's configuration, this memory can be in the form of an EEPROM (per default) or FLASH. The memory is connected to the Microcontroller’s SPI0 interface.

Use SLSO00 (SSC Slave Select Output 0) to enable the memory (see *Figure 8*).

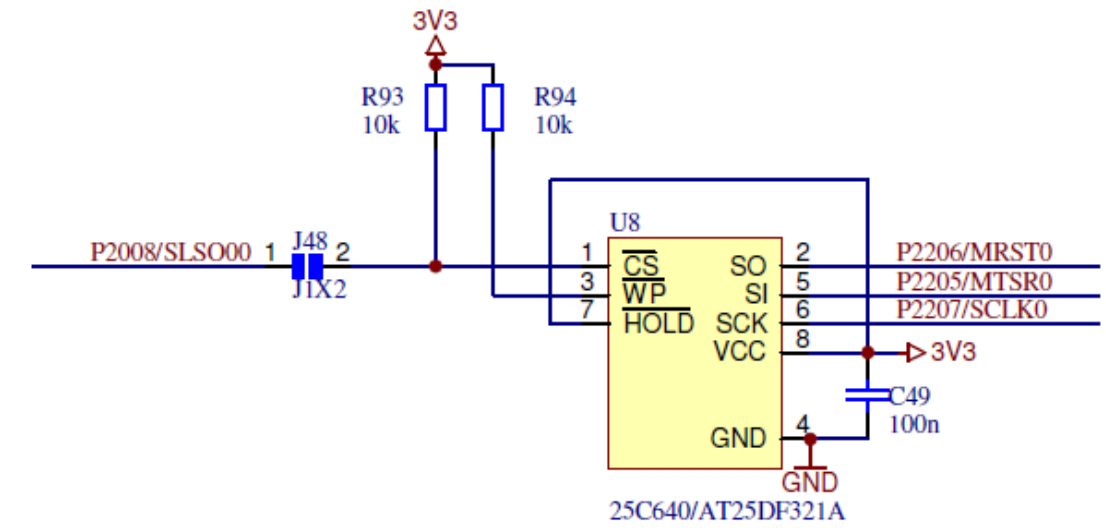
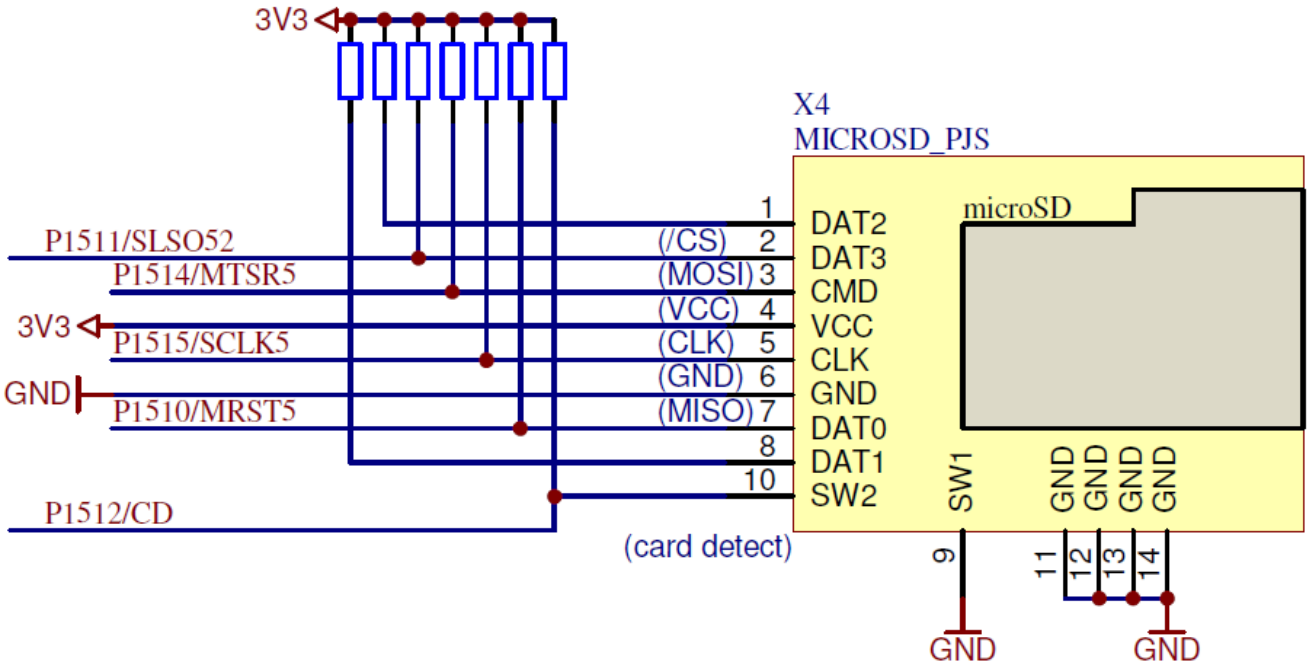


Figure 8: OnBoard SPI EEPROM/Flash connection

Caution!
The phyCORE-TC399 uses the SPI EEPROM U8 to store the modules MAC-addresses. 0x00 to 0x20 should be reserved!

8 uSD Card Interface (SPI Mode) X4

The phyCORE-TC399 is equipped with a micro SD Card Slot. The SD Card Slot is connected (in SPI-Mode) to the TC399



microcontroller SPI5 Interface.

Figure 9: On-board uSD Card Interface (in SPI-Mode) connection

9 Serial Interfaces

The phyCORE-TC399 provides several dedicated serial interfaces, some of which are equipped with a transceiver to allow direct connection to external devices:

1. One high-speed Universal Asynchronous transceiver/receiver (UART)
2. One USB to UART Bridge
3. One 10/100/1000 Mbit/s on-board GbE PHY Ethernet interface
4. One on-board 10/100 Mbit hardwired TCP/IP Ethernet Controller
5. Two Serial Peripheral Interface (SPI) interfaces
6. Two Inter-Integrated Circuit (I^2C) interfaces
7. Up to four Controller Area Network (CAN) interfaces

9.1 Universal Asynchronous Interface

One dual-channel RS-232 transceiver is located on the phyCORE-TC399 at U2 (see *Figure 2*). This device converts the signal levels for the RXD0_TTL and TXD0_TTL lines as well as those of the serial interface, RXD7_TTL and TXD7_TTL, from TTL level to RS-232 level. The RS-232 interface enables a connection of the module to a COM port on a host-PC. The RxD0 line of the transceiver is connected to the TxD line of the COM port, while the TxD0 line is connected to the RxD line of the COM port. The ground potential of the phyCORE-TC399 circuitry needs to be connected to the applicable ground pin on the COM port as well.

The microcontroller's on-chip UART does not support handshake signal communication. However, depending on user needs, hand-shake communication can be software emulated using port pins on the microcontroller. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module. Furthermore, there is the possibility of using the TTL signals of the two UART channels externally. These are available on the phyCORE-connector at X3C19/X3C20 (RXD7_TTL, TXD7_TTL) and X3D16/X3D17 (RXD0_TTL, TXD0_TTL). This becomes necessary if galvanic isolation of the interface signals is required. In this case, the transceiver U2 must not be populated.

Pin #	Signal	Signal Type	Voltage	Description
X3D23	TXD0_RS232	O	RS232	RS232 serial transmit signal
X3D22	RXD0_RS232	I	RS232	RS232 serial data receive signal
X3C23	TXD7_RS232	O	RS232	RS232 serial transmit signal
X3C21	RXD7_RS232	I	RS232	RS232 serial data receive signal
X3D17	TxD0 / P1400 / P1502 (refer to jumper J11/J14)	O	3V3	serial transmit signal
X3D16	RxD0 / P1401 / P1503 (refer to jumper J12/J13)	I	3V3	serial data receive signal
X3C20	P2201/TxD7	O	3V3	serial transmit signal
X3C19	P2204/RxD7	I	3V3	serial data receive signal

Table 13: Location of the UART Signals

9.2 USB to UART Bridge Host Interface

One USB to UART Bridge (CP2102) is located on the phyCORE-TC399 at U7. The CP2102 is a highly-integrated USB to UART Bridge Controller providing a solution to transmit and receive UART signals over USB from a host PC. A Royalty-free Virtual COM Port (VCP) device contains drivers provided by the chip manufacturer to allow a CP2102-based product to appear as a COM port to PC applications.

5V supply voltage from the USB VBUS must be applied on phyCORE-connector pin X3C30 as the CP2102 is bus-powered on the phyCORE-TC399. The TC399 UART0 (Rxd0/Txd) can be connected to communicate over USB to a host PC. This is done by closing jumper J46 and J47 (by default - OPEN) so that RxD0 of the TC399 is connected to the CP2102 UART-

Transmit and TxD0 of the TC399 is connected to the CP2102 UART-Receive.

Refer to jumper J46 and jumper J47 in *Table 9*. It is also possible to activate the /Boot and /PORST by using the R232 handshake Output Signals RTS (Request to Send) and DTR (Data Terminal Ready) provided by the CP2102. RTS can control the /Boot signal (for alternative Bootmode). DTS can control the /PORST signal (for system Reset).

In order to use this feature the optional resistors J44 and J45 must be populated with 0R (by default - unpopulated).

Pin #	Signal	Signal Type	Voltage Domain	Description
X3C30	USB VBUS	PWR_I	5V	5V VBUS
X3D37	USB_D+	I/O	USB	USB DATA+
X3D38	USB_D-	I/O	USB	USB DATA-

Table 14: Location of the USB Host Signals

Caution!
USB to UART Bridge is NOT connected to the TxD0 and RxD0 in the standard phyCORE TC1796 module configuration.

9.3 Ethernet Interface

Connection of the phyCORE-TC399 to a local area network (LAN) is possible with:

- on-board GbE PHY at U12
- on-board 10/100Mbit hardwired TCP/IP Ethernet Controller U2

9.3.1 Ethernet PHY (U12)

The GbE PHY at U12 is connected to the RGMII interface of the TC399. The PHY U12 operates with data transmission speeds of 10 Mbit/s, 100 Mbit/s or 1000 Mbit/s.

With an Ethernet PHY DP83867IRRGZ mounted at U12, the phyCORE-TC399 has been designed for use in 10Base-T, 100Base-T, and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyCORE-Connector X3.

Table 15 shows the location of the signals on the phyCORE-Controller.

Pin #	Signal	Signal Type	Voltage Domain	Description
X3B27	X_ETH0_AP	Gbit Ethernet Differential Transmit and Receive Signal	X3B27	X_ETH0_AP
X3B26	X_ETH0_AN	Gbit Ethernet Differential Transmit and Receive Signal	X3B26	X_ETH0_AN
X3B25	X_ETH0_BP	Gbit Ethernet Differential Transmit and Receive Signal	X3B25	X_ETH0_BP
X3B23	X_ETH0_BN	Gbit Ethernet Differential Transmit and Receive Signal	X3B23	X_ETH0_BN
X3A28	X_ETH0_CP	Gbit Ethernet Differential Transmit and Receive Signal	X3A28	X_ETH0_CP
X3A26	X_ETH0_CN	Gbit Ethernet Differential Transmit and Receive Signal	X3A26	X_ETH0_CN
X3A25	X_ETH0_DP	Gbit Ethernet Differential Transmit and Receive Signal	X3A25	X_ETH0_DP
X3A24	X_ETH0_DN	Gbit Ethernet Differential Transmit and Receive Signal	X3A24	X_ETH0_DN
X3D4	X_ETH0_LED0 (LINK)	Link LED output	X3D4	X_ETH0_LED0 (LINK)
X3C4	X_ETH0_LED1 (ACT)	ACT LED output	X3C4	X_ETH0_LED1 (ACT)

Table 15: Location of the Ethernet Signals

The Ethernet PHY is connected to the RGMII interface of the TC399. Please refer to the *TC399 Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network, some external circuitry is required. The required termination resistors on the analog signals (ETH0_A±, ETH0_B±, ETH0_C±, ETH0_D±) are integrated in the chip, so there is no need to connect external termination resistors to these signals. Connection to an external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+/C-, and D+/D- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit.

The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Caution!
Please see the *Ethernet PHY datasheet* when designing the Ethernet transformer circuitry.

9.3.2 Ethernet Controller (U21)

The Ethernet Controller at U21 is connected to external memory bus (EBU) interface, using /CS2 of the TC399. The Ethernet Controller U21 operates with data transmission speeds of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

The phyCORE-TC399 is equipped with a Ethernet Controller W5300. The W5300 is a single chip into which a 10/100 Ethernet controller, MAC, and TCP/IP are integrated. The Ethernet controller operates in 16-bit mode and is connected to /CS2 of the Microcontroller's External Bus Interface (EBU).

The Signals LINKLED (U21) is routed to pin X3C33 and can be connected to an LED to indicate the link status of media(10/100M). The Signals SPD_LED or TXLED (Transmit Act LED) can be routed to X3C34, configured by jumper J17 (see *Table 9*). On the phyCORE-TC399, the Ethernet controller W5300 is implemented to operate in direct address mode and internal PHY mode.

Please refer to the *W5300 datasheets* for information on how to initialize and program the Ethernet interface and for the needed transformer characteristics.

9.3.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the

phyCORE-TC399 is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

The MAC address has already been programmed into the serial SPI-EEPROM and should be used by your application. The location of the MAC address in the SPI-EEPROM is from 0x00 to 0x0B. The most significant byte is at address 0x00 and the least significant byte is at 0x0B.

Table 16 shows an example of a MAC address and how this address is stored in the SPI-EEPROM. Every position of the MAC address is stored as a binary value in the SPI-EEPROM U8. The example address is 0050C2A0C093.

SPI-EEPROM address	Stored Byte
0x00	00
0x01	00
0x02	05
0x03	00
0x04	0C
0x05	02
0x06	0A
0x07	00
0x08	0C
0x09	00
0x0A	09
0x0B	03

Table 16: Example of a stored MAC address

9.4 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bi-directional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE provides at least two SPI interfaces on the phyCORE-Connector X3.

Note:
The phyCORE-TC399 uses the SPI Interface SPI0 on board for the following devices:
SPI EEPROM U8 (SPI0_/ P2008/SLSO00)

9.5 I²C Interface

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE-TC399 contains two identical and independent multi-master fast-mode I^2C modules. The interfaces U2C0/I2C1 are available on the phyCORE-Connector.

Note:
To ensure the proper functioning of the I^2C interface, external pull resistors matching the load at the interface must be connected. There are no pull up resistors mounted on the module for I2C1.
The phyCORE-TC399 uses the I2C0 on board for the following devices:
RTC U9 Slave address of RTC-8564 is 0xA2/0xA3.

Table 17 lists the I^2C ports on the phyCORE-Connector.

Pin #	Signal	Signal Type	Voltage Domain	Description
X3D32	P1505/SDA0	I/O	3V3	Serial data of I2C module 0
X3C31	P1504/SCL0	O	3V3	Serial clock of I2C module 0
X3C24	P1113/SDA1	I/O	3V3	Serial data of I2C module 1
X3C25	P1114/SCL1	O	3V3	Serial clock of I2C module 1

Table 17: I^2C Interface Signal Location

9.6 CAN Interface

The phyCORE-TC399 is designed to house four CAN transceivers at U3, U4, U5 and U6 (SN65HVD23x). The CAN bus transceiver devices support signal conversion of the CAN transmit (CANTx) and receive (CANRx) lines. The CAN transceiver supports up to 120 nodes on a single CAN bus. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). In order to ensure proper message transmission via the CAN bus, a 120 Ohm termination resistor must be connected to each end of the CAN bus.

Furthermore, it is required that the CANH and CANL input/output voltages do not exceed the limiting values specified for the corresponding CAN transceiver (for the SN65HVD23x -2 VDC / +7 VDC). If the CAN bus system exceeds these limiting values optical isolation of the CAN signals is required.

For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-TC399. This requires purchasing a module without the on-board CAN transceivers installed. Instead, the TxDCANx/RxDCANx signals are routed to the phyCORE-connector with their TTL level. This requires Jumpers closed (refer to section 3 J59-J62 for details)

10 Real Time Clock (RTC-8564)(U9)

For real-time or time-driven applications, the phyCORE-TC399 is equipped with an RTC-8564 Real-Time Clock at U9. This RTC device provides the following features:

- Serial input/output bus (I2C), address 0xA2
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-TC399 is supplied with a +3VDC voltage at Pin X3C6C (VBAT_IN), the Real-Time Clock runs independently of the board's power supply. Programming the Real-Time Clock is done via I2C0 Interface (SCL0, SDA0). The I2C Slave address of RTC-8564 is 0xA2/0xA3.

The Real-Time Clock also provides an interrupt output that extends to the phyCORE connector X3D33D. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. An interrupt must be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. For more information on the features of the RTC-8564, refer to the corresponding data sheet.

11 User LED

The phyCORE provides one on board red user LED (D1). It can be controlled by setting GPIOP10_0 to the desired output level. A high-level turns the LED on, a low-level turns it off.

Figure 2 shows the location of the user LED D1.

12 On-Chip Debug Support Interface

The phyCORE-TC399 is equipped with:

- 16-pin OCDS1/JTAG interface X1 (figure 10)
- 10-pin DAP interface DAP1 (figure 11)

One of these connectors enables direct connection for debug devices on the module. The JTAG/DAP are connected to the phyCORE-Connector X3. Refer to *Figure 2* for the location of the OCDS1/JTAG and DAP connector.

Section 2 shows the pinout of the JTAG Signals on the the phyCORE-Connector.

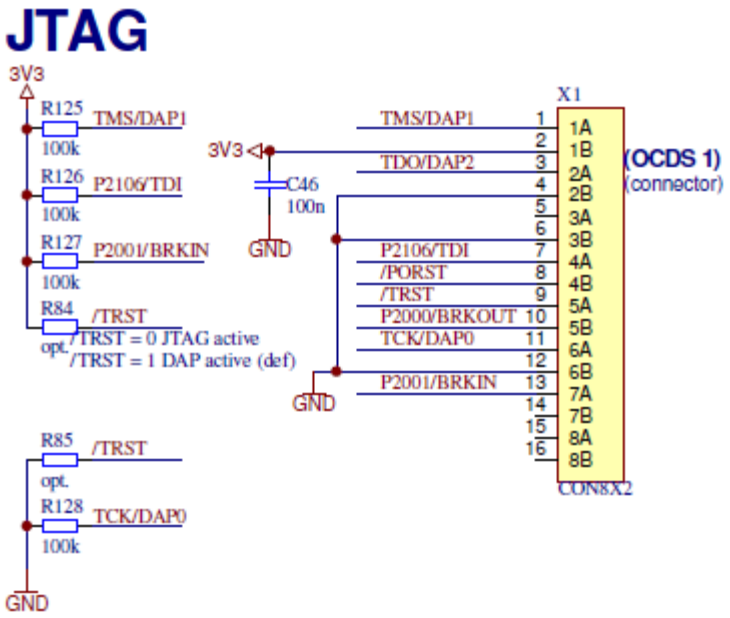


Figure 10: onBoard OCDS/JTAG connector

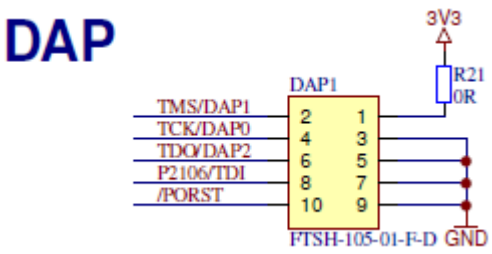


Figure 11: onBoard DAPG connector

13 Technical Specifications

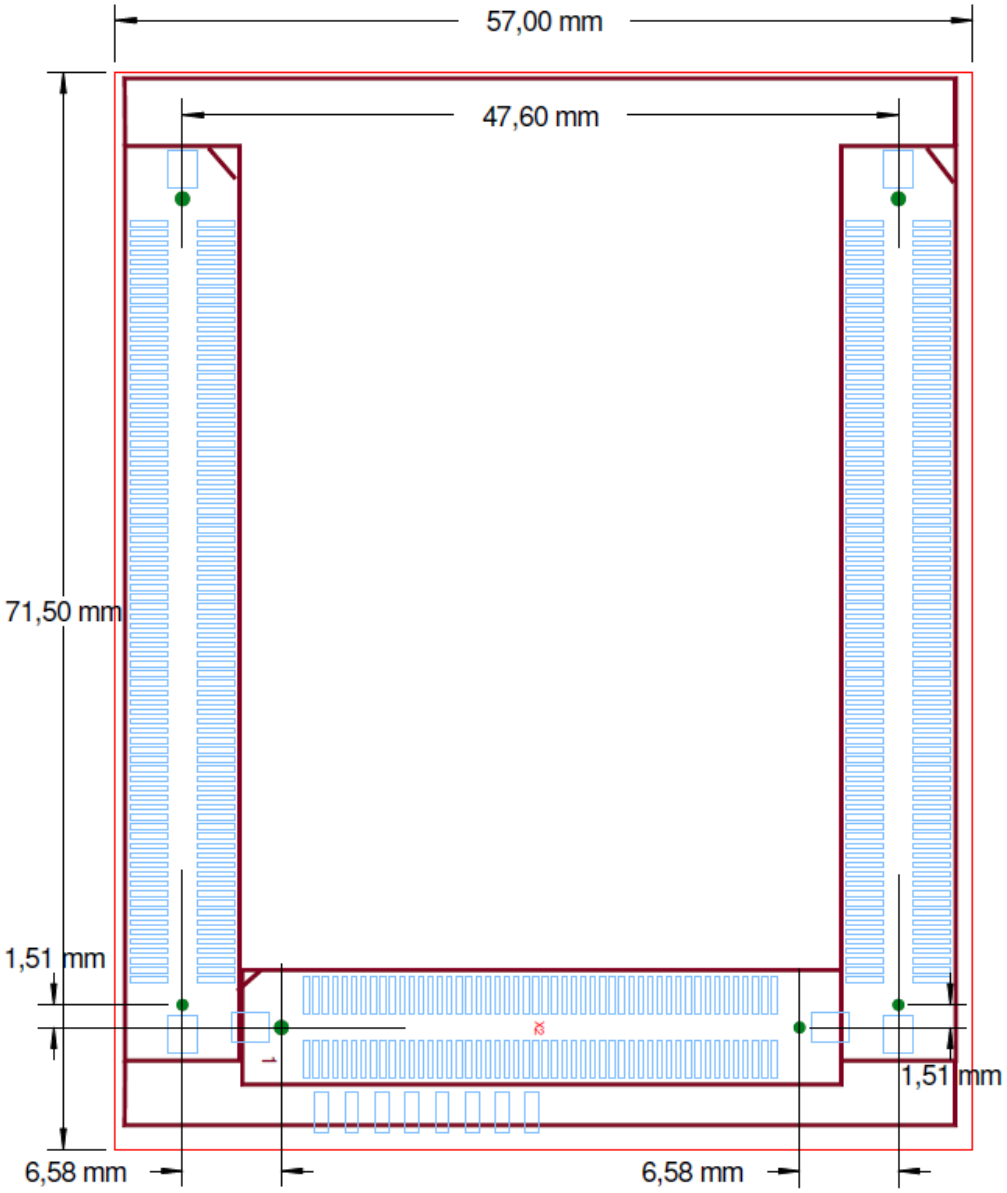


Figure 12: Physical Dimensions (top view)

The physical dimensions of the phyCORE-TC399 are represented in *Figure 12*. The module profile is max. 10 mm thick, with a maximum component height of 3.0 mm on the bottom (connector) side of the PCB and approximately 5.0 mm (without DAP1 connector) on the top (microcontroller) side. The board itself is approximately 1.6 mm thick.

Note:
To facilitate the integration of the phyCORE-TC399 into your design, the footprint of the phyCORE-TC399 is available for download (*Section 1*).

Additional specifications:

Dimensions:	57 x 71.5 mm
Weight:	24g
Storage temperature:	-55°C to +125°C
Operating temperature:	standard: -40°C to +85°C except ethernet W5300 -40°C to +80°C
Humidity:	95 % r.F. not condensed
Operating voltage:	3.3 V ±5 %
Power consumption:	Typ. 600mA

Table 18: Technical Specifications

These specifications describe the standard configuration of the phyCORE-TC399 as of the printing of this manual.

14 Hints for Intergrating and Handling the phyCORE-TC399

14.1 Integrating the phyCORE-TC399

Besides this hardware manual, more information is available to facilitate the integration of the phyCORE-TC399 into customer applications.

1. Many answers to common questions can be found at: https://www.phytec.eu/product-eu/system-on-modules/phycore-tc399/

2. The link “Carrier Board” within the category Dimensional Drawing leads to the layout data as shown in *Figure 13*. It is available in different file formats. Use of this data allows the user to integrate the phyCORE-TC399 SOM as a single component into a design.

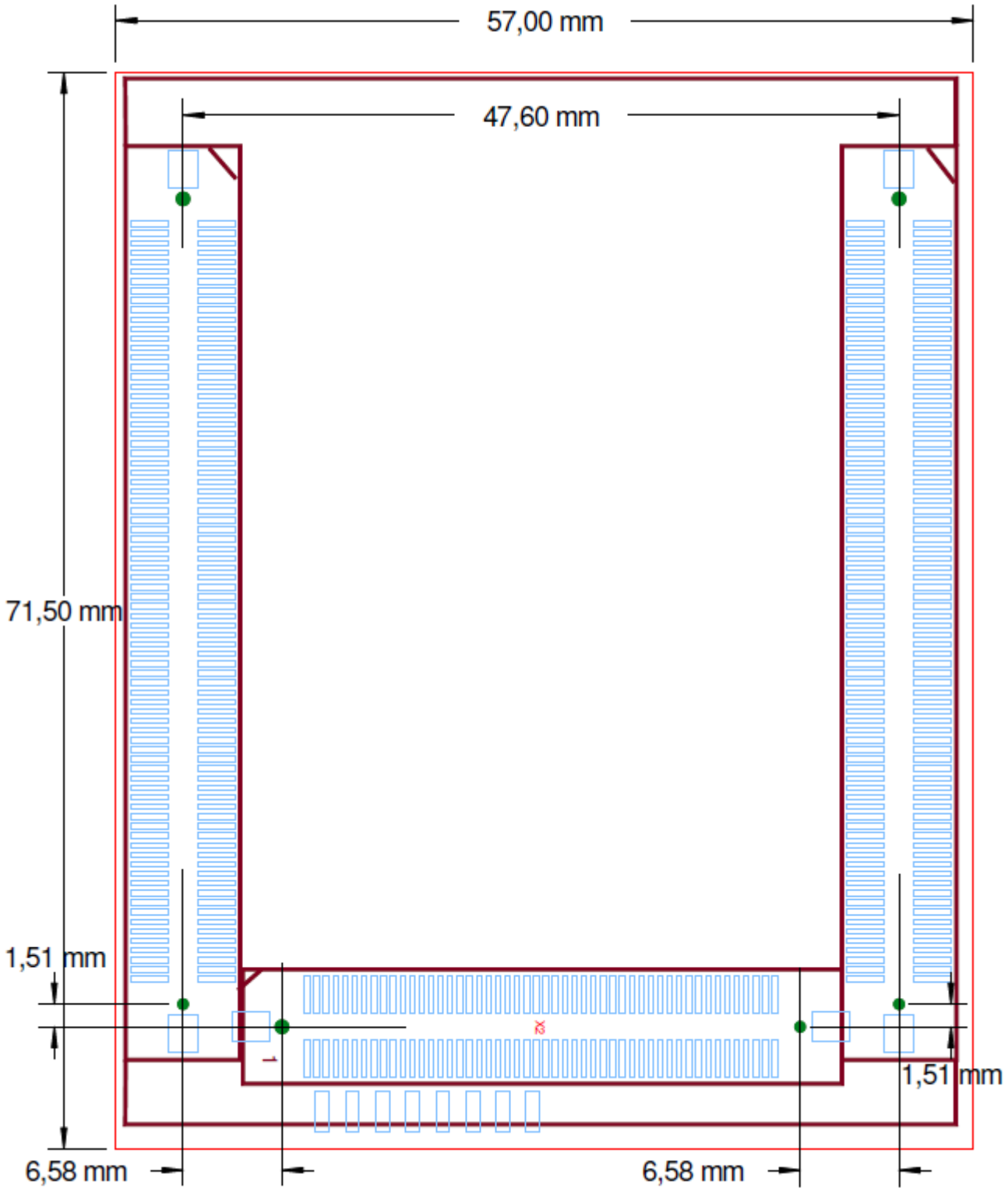


Figure 13: Footprint of the phyCORE-TC399

14.2 Evaluating the phyCORE-TC399 with the corresponding Evaluation Kit "KSP-022-KIT"

The KSP-0200-Kit includes:

- 1 x phyCORE-TC399
- 1 x Development Carrier Board (with on-board wiggler)
- 1 x expand pcb (to access all modules Signals on pcb) that enables the customer evaluating the phyCORE-TC399 prior designing the custom carrier board.

14.3 Handling the phyCORE-TC399

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering.

Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered components need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, hot air rework station or other desoldering method is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For maximum EMI performance, PHYTEC recommends, as a general design rule, connecting all GND pins to a solid ground plane. At the very least, all GND pin neighboring signals, which are being used in the application circuitry, should be connected to GND.

15 Revision History

Date	Version numbers	Changes in this manual
DD.MM.YYYY	Manual L-853E.A0	First edition. Describes the phyCORE-TC399 Prod #: KSP-0200-0.A0 PCB-Version: 4628.0

16 Index

Document: phyCORE-TC399
Document number: L-853e.A0

How would you improve this manual?

Did you find any mistakes in this manual? page

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