MQ292-01

EPSON

Application Manual

Real Time Clock Module

RTC-8563SA/JE

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Application Manual
RTC-8563SA/JE

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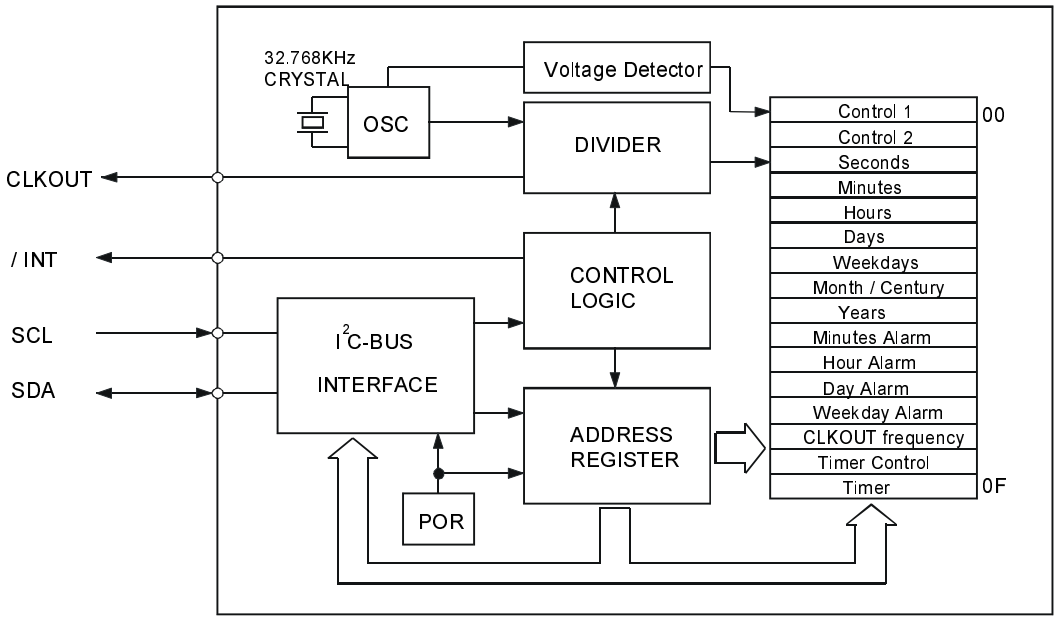
RTC-8563

- Built-in crystal unit running at 32.768KHz
- Compliant with I²C high-speed bus specifications (400KHz)
- Equipped with alarm, timer, and frequency output (32.768KHz, 1024Hz, 32Hz, 1Hz) features
- Inclusion of century bit to enable correct date even after year 2000
- Operating in wide voltage range from 1.8 to 5.5V, and in wide range of clock voltage from 1.2 to 5.5V
- Low power consumption at 0.3μA/3.0V (TYP.)
- Available in small package (SA : SOP-14 pin) and thin package (JE: VSOJ-20 pin)

■ Overview

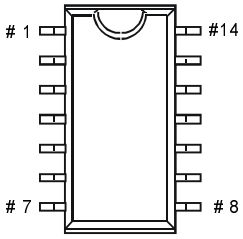
This module is a serial interface real time clock that has a built-in crystal unit. The module offers many functions such as calendar clock, alarm, and timer. All of them can be controlled with a two (2) lines interface. Also, the regular frequency output can be selected from programs. Because this module has multiple features packaged in the same surface, it is ideally suited for applications such as mobile phones, handy terminals or other small electronic systems.

■ Block diagram



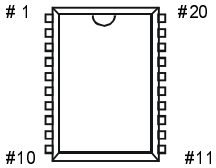
■ Terminal connections

RTC - 8563SA



SOP - 14pin

RTC - 8563JE



VSOJ - 20pin

■ Terminal description

Signal name	Pin No. SOP (VSOJ)	I/O	Signal description
SCL	2 (6)	Input	For input of the serial clock.
SDA	3 (7)	Bi-Directional	This pin synchronizes with a serial clock and input/output address, data, acknowledge bit, etc. The pin is an open-drain in output mode. Be sure to use the appropriate pull-up resistors according to the capacitance of the signal lines.
GND	5 (9)		This pin connects to the ground.
/INT	7 (10)	Output	This pin outputs an interrupt signal such as alarm and timer. The pin is an open-drain terminal.
VDD	11 (4)		This pin connects to the + power source.
CLKOUT	14 (5)	Output	This pin outputs frequency (32.768KHz,1024Hz,32Hz,1Hz) selected by the program. The pin is an open-drain terminal. When initial power is supplied (power supply starting from 0V), the power-on reset function causes 32.768KHz to be output. When output stops, the CLKOUT pin goes to LOW.
N.C.	1,4,6,9,10,12, 13 (1-3,11-20)		This pin is not connected internally. Be sure to connect using OPEN, or GND or VDD
(GND)	- (8)		This pin has the same voltage level as GND. Do not connect externally. *1

*1 For RTC-8563JE only, the eighth pin has the same voltage level as GND. Be sure not to connect externally. (There is no equivalent pin in the RTC-8563SA.)

*2 Be sure to connect a filter capacity of at least 0.1μF closely between VDD and GND.

■ Characteristics

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply Voltage	V_{DD}	Between V_{DD} and GND	-0.5	+6.5	V
Supply Voltage	I_{DD}	V_{DD} pin	-50	50	mA
Input Voltage	V_I	Input pin	GND-0.5	V_{DD} +0.5	V
Output Voltage	V_O	CLKOUT, /INT pips	GND-0.5	V_{DD} +0.5	V
DC Input Current	I_I		-10	10	mA
DC Output Current	I_O		-10	10	mA
Storage Temperature Range	T_{STG}	As single part	-55	+125	°C

2. Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage range	V_{DD}	I^2C-BUS access at 400 KHz	1.8	5.5	V
Clock voltage range	V_{DD}		V_{LOW}	5.5	V
Operating temperature range	T_{OPR}		-40	+85	°C

3. Oscillation characteristics

Parameter	Symbol	Condition	MAX.	Unit
Frequency precision	$\Delta f/fo$	Ta=+25°C, V_{DD}=3.0V	5 ± 23	ppm
Frequency temperature characteristics	top	Ta=+25°C, -10 to +70°C, V_{DD}=3.0V	+10 -120	ppm
Frequency voltage characteristics	f/V	Ta=+25°C, V_{DD}=1.2V to 5.5V	± 2	ppm/V
Oscillation startup-up time	t_{STA}	Ta=+25°C, V_{DD}=1.8V	3	sec
Aging	fa	Ta=+25°C, V_{DD}=3.0V	± 5	ppm/year

4. DC characteristics

If not specifically indicated, V_{DD}=1.8 to 5.5V, Ta= -40 to +85°C

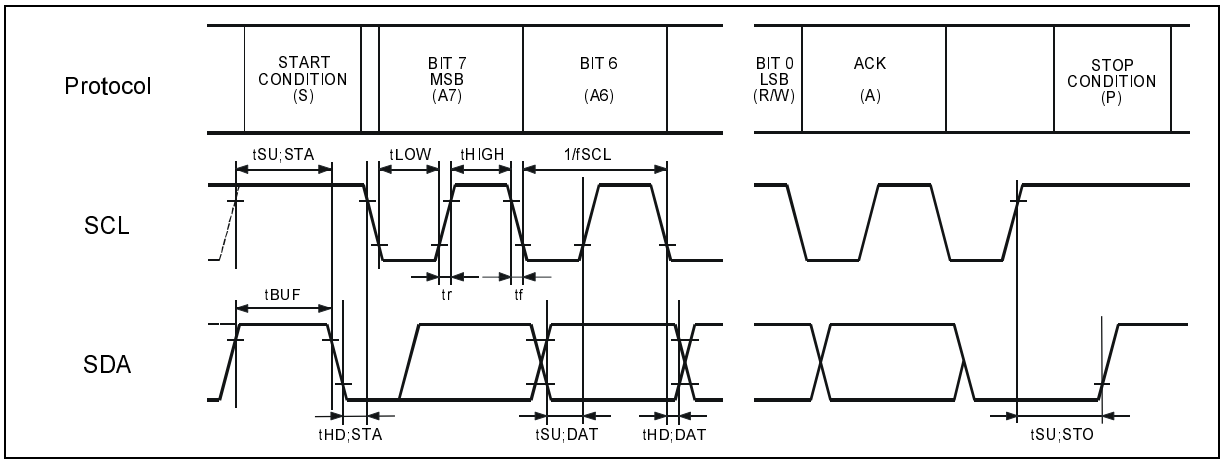
Parameter	Pin	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power current (during access)		I_{DDO}	f_{SCL}=400KHz f_{SCL}=100KHz			800 200	µA µA
Power current (not during access)		I_{DD}	f_{SCL}=0Hz, V_{DD}=5.0V f_{SCL}=0Hz, V_{DD}=3.0V f_{SCL}=0Hz, V_{DD}=2.0V		0.35 0.30 0.25	0.85 0.75 0.70	µA µA µA
Power current (not during access)		I_{DD32K}	f_{SCL}=0Hz, V_{DD}=5.0V f_{SCL}=0Hz, V_{DD}=3.0V f_{SCL}=0Hz, V_{DD}=2.0V		0.85 0.55 0.45	1.80 1.20 1.00	µA µA µA
"L" input voltage		V_{IL}		GND		0.3 × V_{DD}	V
"H" input voltage		V_{IH}		0.7 × V_{DD}		V_{DD}	V
"L" output voltage	SDA	I_{OL} (SDA)	V_{OL}=0.4V, V_{DD}=5V	-3			mA
"L" output current	/INT	I_{OL} (/INT)	V_{OL}=0.4V, V_{DD}=5V	-1			mA
"L" output current	CLKOUT	I_{OL} (CLKOUT)	V_{OL}=0.4V, V_{DD}=5V	-1			mA
Leakage current		I_{LO}	V_O=V_{DD} or GND	-1		1	µA
Low voltage detection		V_{LOW}			1.0	1.2	V

5. AC characteristics

If not specifically indicated, V_{DD}=1.8 to 5.5V, Ta= -40 to +85°C

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCL clock frequency	f_{SCL}				400	KHz
Tolerance spike time on bus	t_{SW}				50	ns
Start condition set-up time	$t_{SU,\ STA}$		0.6			μs
Start condition hold time	$t_{HD,\ STA}$		0.6			μs
SCL "L" time	t_{LOW}		1.3			μs
SCL "H" time	t_{HIGH}		0.6			μs
SCL and SDA rise time	t_r				0.3	μs
SCL and SDA fall time	t_f				0.3	μs
Data set-up time	$t_{SU;\ DAT}$		100			ns
Data hold time	$t_{HD;\ DAT}$		0			ns
Stop condition set-up time	$t_{SU;\ STO}$		4.0			μs

Timing chart



■ Registers

1. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	Control 1	TEST	0	STOP	0	TEST	0	0	0
01	Control 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02	Seconds	VL	4	2	1	8	4	2	1
03	Minutes	x	4	2	1	8	4	2	1
04	Hours	x	x	2	1	8	4	2	1
05	Days	x	x	2	1	8	4	2	1
06	Weekdays	x	x	x	x	x	4	2	1
07	Months/Century	C	x	x	1	8	4	2	1
08	Years	8	4	2	1	8	4	2	1
09	Minute Alarm	AE	4	2	1	8	4	2	1
0A	Hour Alarm	AE	4	2	1	8	4	2	1
0B	Day Alarm	AE	x	2	1	8	4	2	1
0C	Weekday Alarm	AE	x	x	x	x	4	2	1
0D	CLKOUT frequency	FE	x	x	x	x	x	FD1	FD0
0E	Timer control	TE	x	x	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

2. Notes

(1) Write to bit 'x' is not possible, and its read-out value is not fixed. Be sure to mask it after bit 'x' is read out.
(2) Be sure to set bit '0' of address 00,01 (Control1,2) to zero.
(3) All count data at address 02 through 05 and 08 through 0B is in the BCD format.
(4) If data and time are set to impossible values, the clock cannot operate correctly.
(5) While there is a bit at address 00 for setting the test mode, the test mode is a special operation mode that is used by EPSON for testing devices. Be sure not to set it to 1. If it is set to the test mode, all operations of the device will not be guaranteed. Therefore, be careful when handling address 00.

3. Register description

3.1. Control register 1

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	Control 1	TEST	0	STOP	0	TEST	0	0	0

TEST: The two TEST bits are for testing devices. Therefore be sure to set them to zeros. If they are accidentally set to 1, they may immediately modify the clock data or result in abnormal time.

STOP: The device's time function operates when this bit is zero. When the bit is set to 1, all count down chain circuit less than 1 second go into the zero clear state. If it is cleared together with time reporting, the time can be adjusted accurately up to one second. If the frequency output from the CLKOUT terminal is set to 32.768 KHz, the output may stop depending on the logical state of this bit.

3-2. Control register 2

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01	Control 2	0	0	0	TI/TP	AF	TF	AIE	TIE

TI/TP: If this bit is set to 0, when the timer counts down in the single operation mode and becomes zero, it sets the TF flag and then stops. If this bit is set to 1, when the timer in the repeat mode becomes zero, it sets the TF flag, and it furthermore reload the initial value and repeat to count down. As long as the TF flag is not cleared, the set is maintained.

AF: This is a flag bit which goes into the set state when an alarm occurs.

TF: This is a flag bit which goes into the set state when the timer counts down within the specified cycle and becomes zero.

AIE: This bit determines whether to output the alarm flag state to the /INT pin. When it is set to 1, AF=1 and /INT becomes LOW. When it is set to 0, the information is not output to the /INT pin.

TIE: This bit determines whether to output the timer flag state to the /INT pin. When it is set to 1, TF=1 and /INT becomes LOW. When it is set to 0, the information is not output to the /INT pin.

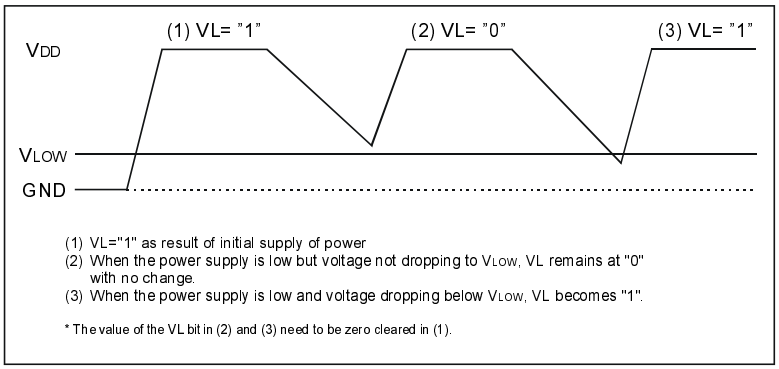
(Note) The /INT pin outputs the logical OR signal of alarm interrupt and timer interrupt. When an interrupt occurs, the AF/TF flag is read out. Therefore, be sure to check to see which interrupt event has occurred. If both alarm and timer are prohibited to have the /INT pin output. The /INT pin will not become LOW active. If all hardware interrupts cannot be used due to system constraints, after the above setup, be sure to use the software to monitor the interrupt flags for AF and TF.

3-3. Clock and calendar registers, and VL bit and century bit

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02	Seconds	VL	4	2	1	8	4	2	1
03	Minutes	x	4	2	1	8	4	2	1
04	Hours	x	x	2	1	8	4	2	1
05	Days	x	x	2	1	8	4	2	1
06	Weekdays	x	x	x	x	x	4	2	1
07	Months/Century	C	x	x	1	8	4	2	1
08	Years	8	4	2	1	8	4	2	1

If data and time are set to impossible values, the clock cannot operate correctly. Therefore pay attention when handling them.

VL: This is the bit for detecting low voltage. When the power source's voltage drops below V_{LOW}[V]*, this flag is set to 1. After the initial power-on, it is set to 1. If this flag is set to 1 after recovery from the backup state, this means during the backup the power was low, and all data need to be initialized.
However, because this bit is write cleared regardless of the data, before performing a write to this register, be sure to read out its value.



* See the description on DC characteristics.

C: This bit indicates change of century. When the year digit data overflows from 99 to 00, this bit is set. By presetting it to 0 while still in the 20th century, it will be set in year 2000, but in fact the first year in the 21 century should be 2001.

3-4. Alarm registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
09	Minute Alarm	AE	4	2	1	8	4	2	1
0A	Hour Alarm	AE	4	2	1	8	4	2	1
0B	Day Alarm	AE	x	2	1	8	4	2	1
0C	Weekday Alarm	AE	x	x	x	x	4	2	1

AE: This is the alarm control bit.
There is an MSB for each register of minute alarm, hour alarm, day alarm, and day of week alarm.
When this bit is set to 1, the appropriate register will be set to the alarm condition unconditionally.
When the AE bit in hour-alarm is set, alarm will occur at the specified minutes regardless of the hours.
In other words the alarm will occur at the specified minute of every hour.
Similarly, when minute and hour are set to AE, alarm occurs at the specified date.
Therefore, by combinations of AE-bits in this way a highly versatile alarm can be set.
But when all of the AE-bits are set, alarm will not occur.

Additional information on the alarm function:
When alarm condition is set all day.
First alarm is occurs.
Then you clear the AF-flag.
But, in same condition, alarm never occurs any more.
In same condition, alarm occurs only one time.
Therefore, use the AF-flag carefully.

3-5. CLKOUT frequency selection and timer registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	CLKOUT frequency	FE	x	x	x	x	x	FD1	FD0
0E	Timer control	TE	x	x	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

- Frequency output

Output frequency	FD1	FD0
32768Hz	0	0
1024Hz	0	1
32Hz	1	0
1Hz	1	1

At the above setting, the output frequency of the CLKOUT pin can be selected.
Output is possible when the FE of MSB of the D register is 1. (When it stops, the CLKOUT pin goes to LOW.)

- Timer control

Timer source clock	TD1	TD0
4096Hz	0	0
64Hz	0	1
1 second	1	0
1 minute	1	1

At the above setting, the count down rate of the timer can be selected.
When the TE of MSB of the E register is 1, the timer count down starts, and stops when it becomes 0.
The F register data counts down at the set frequency and when it becomes zero TF is set.
When the F register is read, the data during count down is read out.

- Timer register

It sets the initial value of the timer's count down. The format is binary.

■ Acess procedure

1. Characteristic of the I^2C-BUS

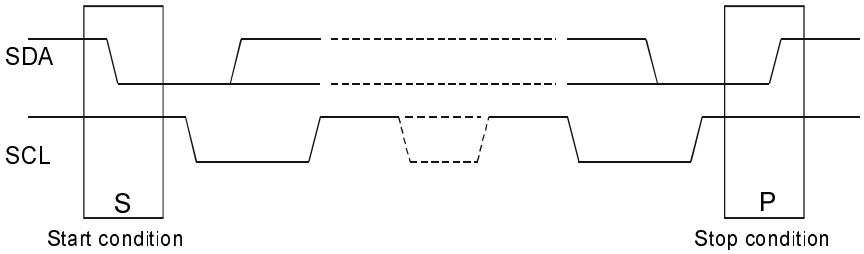
I^2C-BUS is a bi-directional interface that uses two (2) lines. This interface has two signal lines, which are SDA (data line) and SCL (clock line). Both of these lines are connected to the V_{DD} line via the pull-up registers. All ports must be open drain or open collector on the I^2C-BUS in order to be able to connect multiple devices on this bus using the AND-connection.

2. Bit transfer

The bit data transfer is executed for one bit on each one clock pulse of SCL line. When the device transmits the data, the data change should be executed while SCL line is at LOW. When the device receives the data, the data should be taken in while SCL is at HIGH.

3. Start condition and stop condition

When I^2C-BUS is not interfacing, the two control lines keep at HIGH. When SDA changes from HIGH to LOW, this is defined as a start condition. After that, actual data transfer is executed. When SCL is at HIGH and when SDA changes from LOW to HIGH, this is defined as a stop condition.

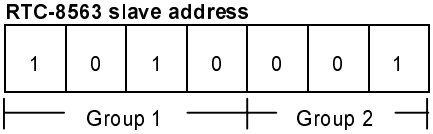


4. Slave address

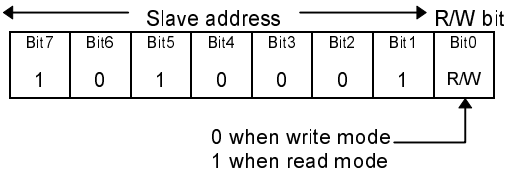
The I^2C-BUS devices do not have any chip select pins with the usual logic devices. All I2C-BUS devices have a fixed unique device number for each device built into them. The chip selection on the I^2C-BUS is executed when the communication starts and this device number is sent from I^2C-BUS as a slave address. The receiving device responds to the communication only if it matches the slave address.

The slave address is a 7-bit data which is made of a 4-bit fixed data (group 1) and 3-bits data (group 2). On the RTC-8563, the data in group 1 is 1010 and in group 2 is 001.

RTC-8563 slave address

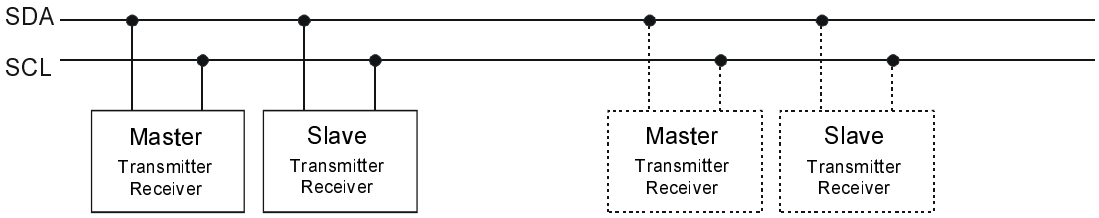


During the actual data transmission, the transmitted data contains both the slave address and the 8-bit data with the added R/W (read/write) bit.



5. System structure

A master is defined a device that controls interfacing of messages, and a slave is defined as a device which is controlled by the master. A transmitter is defined as a device transmitting messages,and a receiver is defined as the one receiving messages. In the case of the RTC-8563, controllers such as CPU are masters and the RTC-8563 is a slave. Each device can be transmitter and receiver.



6. Acknowledge

There is no limit to the byte size of data transmitted between the start and stop conditions. For each byte during interfacing, the receiver (receiving end) generates an acknowledge bit to the transmitter (sending end) to confirm that it has received the data. Because the acknowledge bit is LOW active, the transmitter sets the SDA line to HIGH, and sends out a clock pulse for the acknowledge bit. If the receiver can correctly receive the 8-bit data from the transmitter, it will set the SDA line to LOW when the clock for the last bit is finished. Because the I^2C-BUS lines are pulled-up, the SDA line of transmitter also turns to LOW. At this moment, the transmitter checks that the acknowledge has returned, and then continues to send out the next data. When the clock pulse for the acknowledge bit is finished, the receiver turns the SDA line to HIGH (release) and prepares to receive the next data.

When a master device is acting as a transmitter and acknowledge is confirmed from the receiver, if the next data is not sent/received but the stop condition is generated, it is possible to terminate the communication normally. When a master device is acting as a receiver and acknowledge bit is sent out as "1", it is possible to terminate the communication normally if the stop condition is generated.

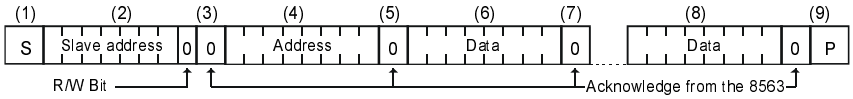
7. I^2C-BUS protocol

The following section describes the communications procedure where the master is CPU and the slave is the RTC-8563.

(1) Procedure for write at specified address

The RTC-8563 has an auto increment function of address. After the initial address is set, if only data continues to be sent, the receiving address on the 8563 is incremented by 1 byte. The procedure as follows:

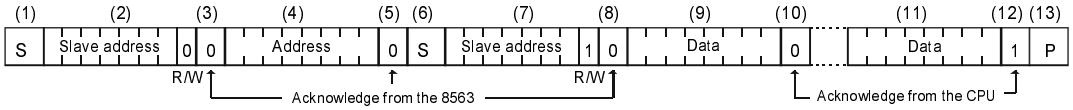
(1) The CPU sends out a start condition.
(2) The CPU sends out the slave address of the 8563 and the R/W bit, in write mode.
(3) Confirm acknowledge from the 8563.
(4) The CPU sends out the write address to the 8563.
(5) Confirm acknowledge from the 8563.
(6) The CPU sends out the data for write to the address specified in step (4).
(7) Confirm acknowledge from the 8563.
(8) If necessary repeat steps (6) and (7). The address will be automatically incremented internally on the 8563.
(9) The CPU sends out the stop condition.



(2) Procedure for read at specified address

According to the write mode, after the address to read is written, the read mode is set and the actual data read. The procedure as follows:

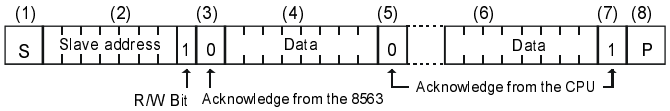
(1) The CPU sends out a start condition.
(2) The CPU sends out the slave address of the 8563 and the R/W bit, in write mode.
(3) Confirm acknowledge from the 8563.
(4) The CPU sends out the address read out from the 8563.
(5) Confirm acknowledge from the 8563.
(6) The CPU sends out the start condition (stop condition is not sent.)
(7) The CPU sends out the slave address of the 8563 and the R/W bit, in read mode.
(8) Confirm acknowledge from the 8563.(From here on, the CPU acts as a receiver and the 8563 as a transmitter.)
(9) Data at the address specified in step (4) is sent out from the 8563.
(10) The CPU sends out acknowledge to the 8563.
(11) If necessary repeat steps (9) and (10). The read address will be automatically incremented internally on the 8563.
(12) The CPU sends out the stop condition.



(3) Read procedure without specified address

Immediately after the read mode is set up, data can be read. In this case, the address is the address when the previous access ended, plus 1. The procedure is as follows:

(1) The CPU sends out a start condition.
(2) The CPU sends out the slave address of the 8563 and the R/W bit, in read mode.
(3) Confirm acknowledge from the 8563.(From here on, the CPU acts as a receiver and the 8563 as a transmitter.)
(4) Data at the last address in the previous access plus 1 is sent out from the 8563.
(5) The CPU sends out acknowledge to the 8563.
(6) If necessary repeat steps (4) and (5). The read address will be automatically incremented internally on the 8563.
(7) The CPU sends out acknowledge of "1".
(8) The CPU sends out the stop condi tion.



■ About power interruption and resume

To make sure 32.768 KHz of clock impulse can be output immediately after the power is supplied, this device comes with the built-in power-on reset circuitry. In order that each circuitry sequence at power-on can be synchronized for operation, the device is designed in a way that the oscillation signal from its built-in crystal unit enables the synchronization. The power-on reset results in logical initialization of bit set of each register, as well as supply of stable power to the analog circuitry such as oscillation circuitry and voltage detection circuitry. Therefore, be sure to enables power supply in a way that the power-on reset can definitely operate.

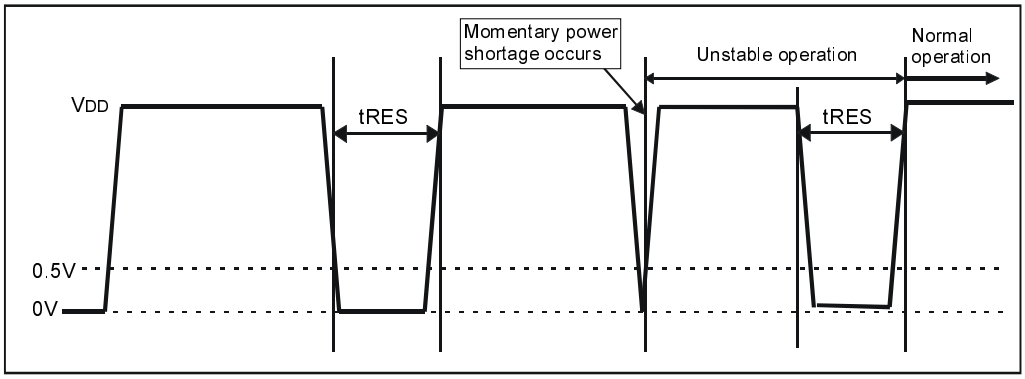
It takes about two seconds from when the built-in crystal unit stops its oscillation to when the power is supplied and stable oscillation begins. During this period after the power is supplied, the internal of the device is initialized. If the power is supplied again within this two seconds, the power-on reset function may not work normally. Specifically, the 32.768 KHz clock impulse output will stop, or the serial interface will go into the reset hold state so that access is not possible.

To make sure the power reset can definitely be performed, be sure to re-supply power to the device by following the conditions below.

1: Be sure to leave two seconds or more between power-off and power-on.
tRES=2sec (MIN)

2: The power-off mentioned above refers to the state where V_{DD} is 0.5V or less.

If momentary power shortage occurs so that the device fails to operate normally, be sure to re-supply the power.



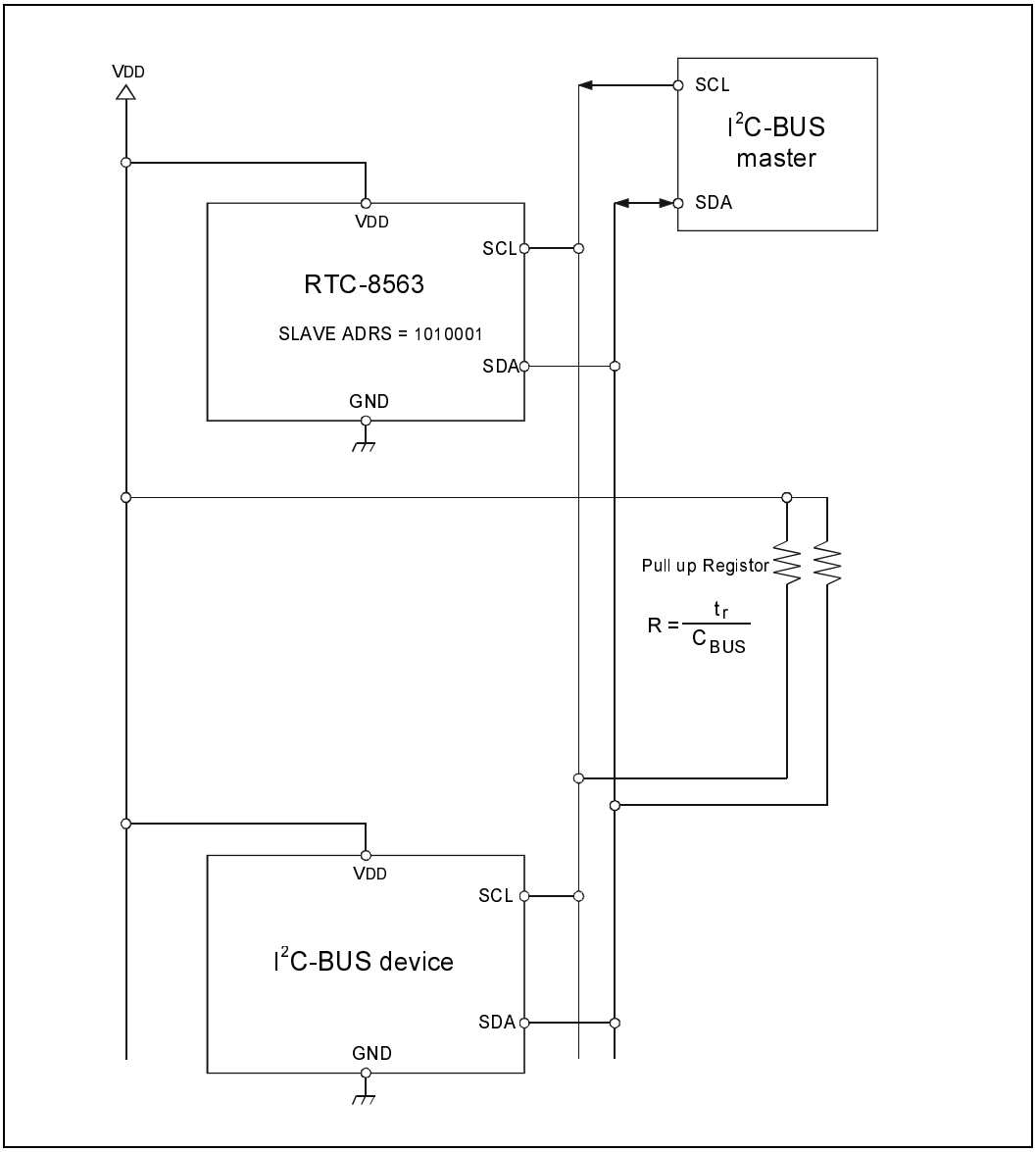
(1) When V_{DD} changes from 0V to the initial power supply, the device operates with no problems.

(2) The device also operates with no problems when it returns from the backup state.

(3) When momentary power shortage occurs where V_{DD} returns from below 0.5V within two seconds, the device may not operate normally.

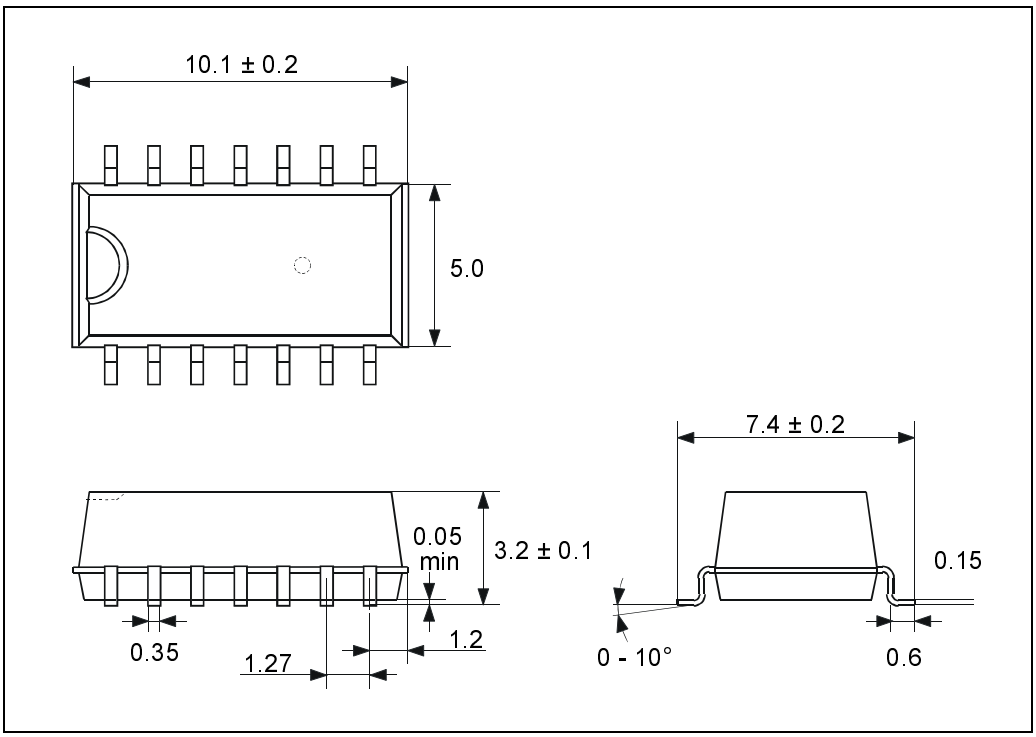
(4) In the case communication with the device becomes not possible after power is re-supplied, this is likely because the power-on reset cannot work normally. If this happens, re-supply the power by following the conditions above.

■ Typical connection to micro computers

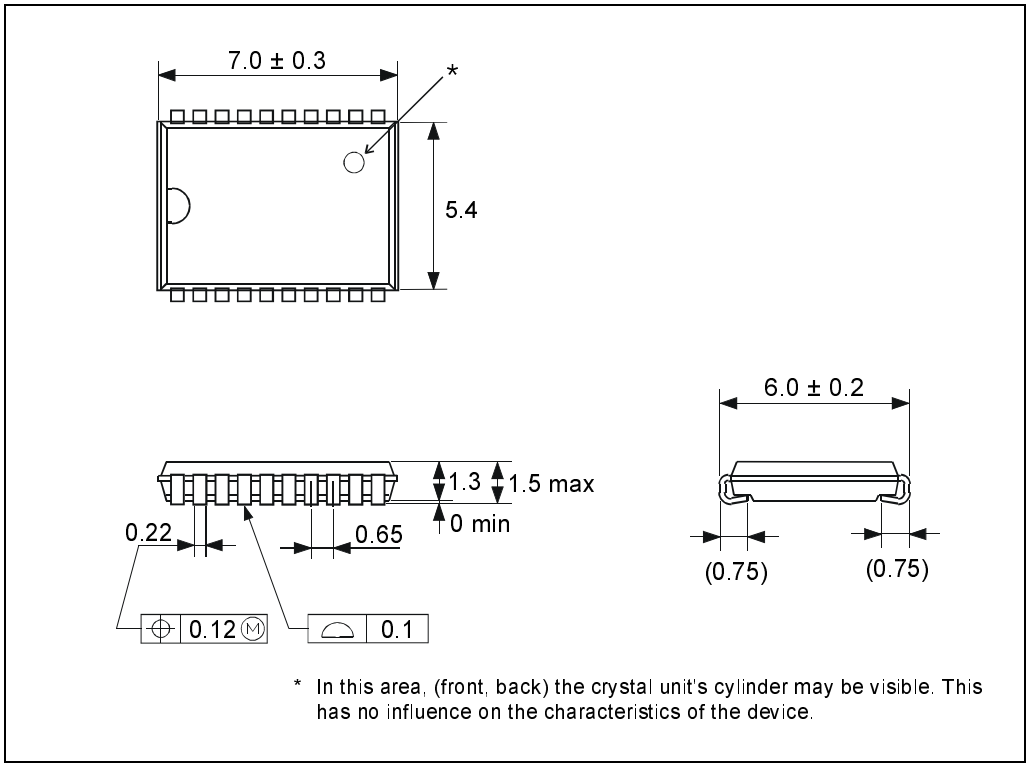


■ External dimension

- RTC-8563SA (SOP 14-pin)

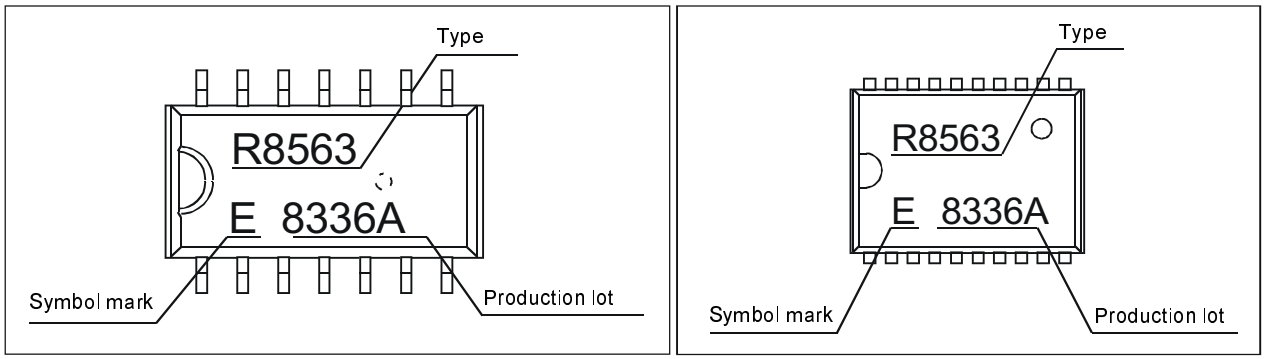


- RTC-8563JE (VSOJ 20-pin)



■ Marking layout

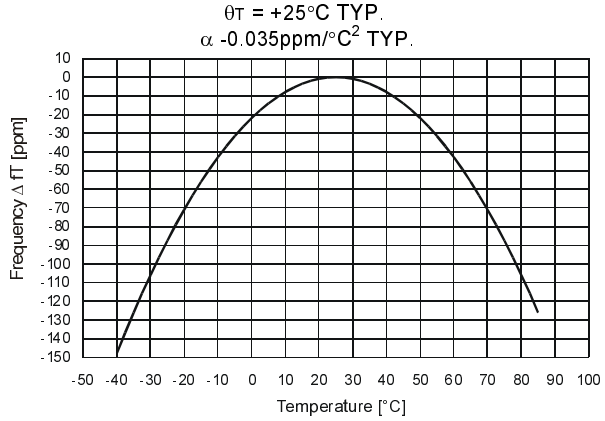
- RTC-8563SA (SOP 14-pin)



Note: The above indication shows the markings and outlines their general positions.It is not a specification of the type faces, sizes, and positions of the characters.

■ Reference data

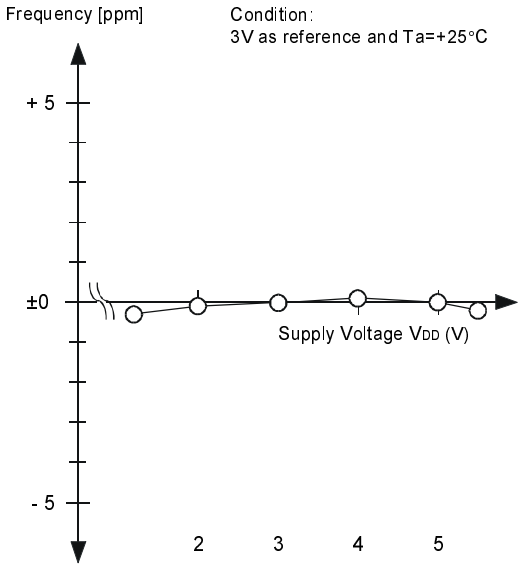
(1) Frequency temperature characteristics example



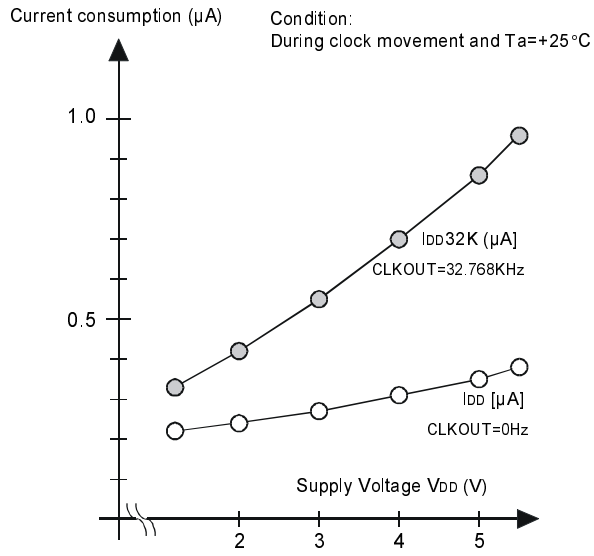
Finding the frequency stability (clock accuracy)

1. The frequency temperature characteristics can be approximated by using the following formula:
   $\Delta f_T(ppm)=(\theta_T-\theta_X)^2$
   - Δf_T (ppm) : Frequency deviation at target temperature
   - α (ppm/°C) : Secondary temperature coefficient (-0.035±0.005ppm/°C²)
   - θ_T (°C) : Peak temperature (25°C±5°C)
   - θ_X (°C) : Target temperature
2. To determine the overall clock accuracy, add the frequency precision and the voltage characteristics:
   $\Delta f/f(ppm) = \Delta f/f_0 + \Delta f_T + \Delta f_V$
   - $\Delta f/f$ (ppm) : Clock accuracy at a given temperature and voltage (frequency stability
   - $\Delta f/f_0$ (ppm) : Frequency precision
   - Δf_T (ppm) : Temperature dependent frequency deviation
   - Δf_V (ppm) : Voltage dependent frequency deviation
3. Finding the daily deviation:
   Daily deviation = $\Delta f/f \times 10^{-6} \times 86400$ (seconds)
   The clock error is one second per day at 11.574 ppm.

(2) Example of the frequency/voltage characteristics



(3) Example of the current consumption/voltage characteristics



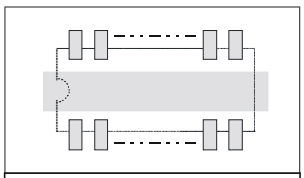
■ Application notes

(1) Notes on handling

In order to enable this module to operate at low power level, the C-MOS circuitry was used in the design of the chip. Note the following cautions when handling it:

1. Static electricity
While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

2. Noise
If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1μF as close as possible to the power supply pins (between V_{DD} and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module. Do not connect signal lines to the shaded area in the figure shown on the right and, if possible, embed this area in a GND land.


Example for the RTC-8563SA

3. Voltage levels of input pins
When the input pins are at the mid-level , this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to V_{DD} or GND.

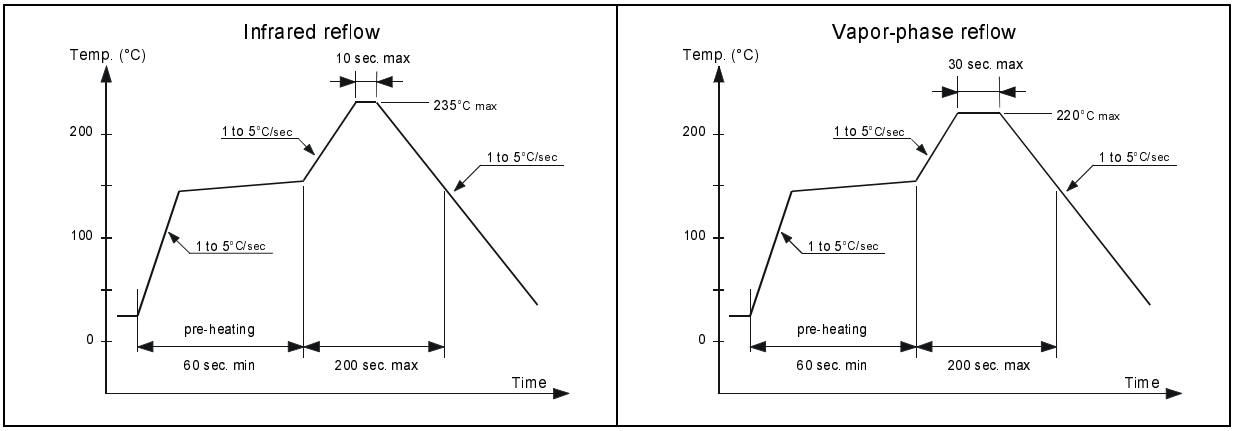
4. Handling unused input pins except (V_{DD}) pin
Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

(2) Notes on packaging

1. Soldering temperature conditions
If the temperature within the package exceeds 260°C, the characteristics of the crystal unit will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Also, check again if the mounting conditions are later changed.

Soldering conditions: Not higher than 260°C for no more than twice at 10 seconds,
or not higher than 230°C for no more than 3 minutes

Examples of SMD soldering conditions



2. Mounting equipment
While this module can be used with general-purpose mounting equipment, the internal crystal unit may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

3. Ultrasonic cleaning
Depending on the usage conditions, there is a possibility that the crystal unit will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

4. Mounting orientation
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

5. Leakage between pins
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.