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TC1775

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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TC1775 Documentation Addendum

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Previous Version:	V 1.0, 2001-07	
Page	Subjects (major changes since last revision)	
–	changes from V 1.0 to V 1.1 see change bars;	

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1 Introduction

This document describes corrections, changes, and improvements for the two parts of the TC1775 User's Manual V2.0 2001-02, the System Units book and the Peripheral Units book. These corrections will be considered with the next update of these User's Manual documents.

The referenced documents to this addendum are:

- TC1775 System Units User's Manual, V2.0, Feb. 2001 (**Link to the PDF**)
  Ordering No.: B158-H7780-X-X-7600
- TC1775 Peripheral Units User's Manual, V2.0, Feb. 2001 (**Link to the PDF**)
  Ordering No.: B158-H7781-X-X-7600
- TC1775 Data Sheet, V1.1, Sep. 2001 (**Link to the PDF**)

2 User's Manual - System Units Part

Page 1-3, Table 1-2

The definition of "U" must be changed into:

"Access permitted in User Mode 1 only.

Note: User Mode definitions see bit PSW_IO at Page 2-20"

Page 3-18

The following paragraph will be added on the bottom of this page and before the "Note" paragraph on the next page:

"When a disabled module is switched on by writing an appropriate value to its MOD_CLC register, status bit DISS changes from 1 to 0. During the phase, where the module becomes active any write access to corresponding module registers (when DISS is still set) will generate a bus error. Therefore, when enabling a disabled module, application software should check after activation of the module once whether DISS is already reset, before a module register will be written to."

Page 3-22, Table 3-5

The row for register STM_CLC must be corrected into:

STM_CLC	STM	enabled	■	–	–	–	–	–

Page 5-7, Section 5.3.1

The first sentence of the paragraph "When both of these conditions ...." is replaced by the following three sentences:

"When both of these conditions are met the $\overline{\text{HDRST}}$ output is released and tri-stated by the TC1775. If within this tri-state phase $\overline{\text{HDRST}}$ is still driven by an external device, the TC1775 remains in the reset condition as long as $\overline{\text{HDRST}}$ is at low level. When $\overline{\text{HDRST}}$ is again pulled to high level externally, the power-on reset sequence is terminated."

Page 5-7, Section 5.3.2

The last two paragraphs from the bottom must be replaced by the following new paragraph (see CR106566):

"The external hardware reset pin $\overline{\text{HDRST}}$ serves as an external reset input as well as a reset output. It is an active-low, bidirectional open-drain pin with an internal weak pull-up. An active-low signal at this pin causes the chip to enter its internal hardware reset sequence at the next system clock (f_{SYS}) transition. For synchronization purposes, $\overline{\text{HDRST}}$ must be at low level at least for two system clock cycles. $\overline{\text{HDRST}}$ is not actively driven by the TC1775 during a hardware reset sequence. If other hardware is reset by the signal line connected to $\overline{\text{HDRST}}$, the $\overline{\text{HDRST}}$ driving device must meet timing requirements for this hardware. After the TC1775 has terminated its hardware reset sequence internally, flag RST_SR.HDRST is set.

When $\overline{\text{HDRST}}$ is driven low by the TC1775 in software reset or in Watchdog Timer reset, the duration of $\overline{\text{HDRST}}$ low pulse is 16 × t_{SYS} (t_{SYS} is the period of the system clock with frequency f_{SYS}), this means 400 ns at f_{SYS} = 40 MHz."

Page 5-8 Section 5.3.3

At the end of this section the following paragraph should be added:

"During a software reset operation the $\overline{\text{HDRST}}$ output signal is generated when RSTREQ.RREXT = 1. Note, that if after the end of such a software reset operation ($\overline{\text{HDRST}}$ output released and tri-stated by the TC1775) $\overline{\text{HDRST}}$ is still driven low by an external device, the TC1775 detects an external hardware reset condition and starts executing it as described in **Section 5.3.2**."

Page 5-11, Table 5-2

The two rows with Module/Function = "System Timer" and "Reset output pin $\overline{\text{HDRST}}$" must be corrected into:

System Timer	■	■	Optional	Not affected	■
Reset output pin $\overline{\text{HDRST}}$	■	■	Optional	Tri-stated	■

Page 5-9, Last paragraph of 5.3.4

In the last but one sentence "RSDBG, " should be deleted. This flag is not available.

Page 5-9

The text in the last paragraph beginning with "If a Watchdog Timer error occurs ...." until the end of this section on the next page 5-10 should be replaced by the following new paragraph:

"However, the reset circuitry of the TC1775 is designed to detect a double reset condition of the Watchdog Timer. If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1775 is held in reset until a power-on reset or hardware reset occurs (see also **Chapter 18**)."

Page 6-9, Second paragraph of 6.3.3.5

The following sentence is added at the end of this paragraph: "Note also that the external NMI status flag NMISR.NMIEXT is not set after this Deep Sleep Mode exit case because the reset sequence clears NMISR.NMIEXT again after it has been set shortly through the falling edge on the $\overline{\text{NMI}}$ pin."

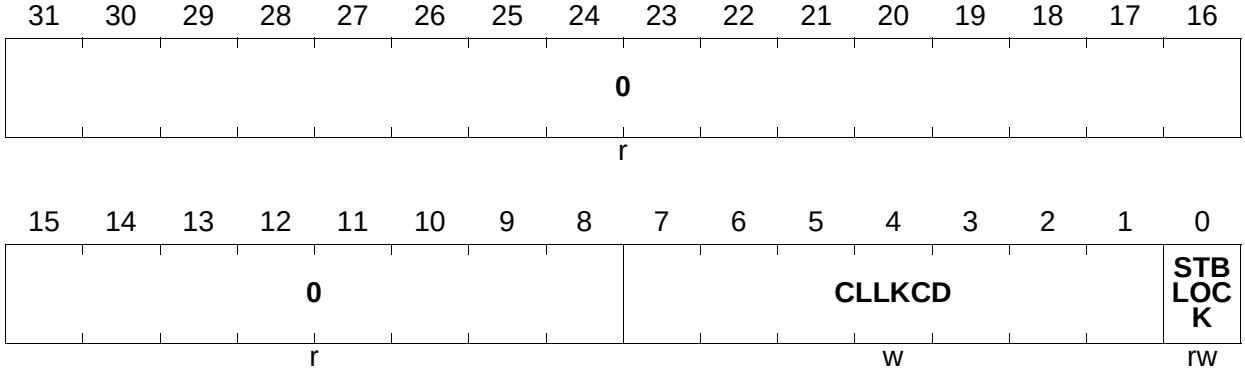
Page 7-5

In the last three paragraphs of the description below "Segment 11", the "and" between the address region values should be replaced by "to".

Page 9-11

The description of register DMU_CON must be corrected in the following way:

DMU_CON
DMU Control Register **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
STBLOCK[1)]	0	rw	**Lock Standby Data Memory** Bit can be set by writing a 1 to it (in supervisor mode only). Bit can only be reset (in supervisor mode only) by writing a 0 to it together with the appropriate clear lock code. 0 Normal operation of standby data memory 1 Standby data memory is locked. No read or write access of/to standby SRAM is possible. The state of STBLOCK after power-on reset is undefined. A hardware or software reset does not effect this bit.
CLLKCD	[7:1]	w	**Clear Lock Code** This bit field has to be written with 65$_H$ together with STBLOCK = 0 to reset the lock of the standby RAM.
0	[31:8]	r	**Reserved**; read as 0; should be written with 0.

1) This bit field is not available in the TC1775 BA11 step.

Page 11-54, Figure 11-18

In Figure 11-18 the block for registers P13_ALTSEL0 and P13_ALTSEL1 must be exchanged.

Page 11-36, Table 11-14

Column "Alternate Function": "EBU inactive" must be replaced by "Trace disabled". Also the note below Table 11-14 is changed into "Alternate functions of Port 5 (trace outputs) are controlled by hardware (bit SCU_CON.ETEN, see also **Chapter 4**)".

Page 12-15, Second paragraph

"A[26:0]" should be replaced by "A[25:0]".

Page 12-21, 12-22 (Figure 12-6), and 12-62

The TC1775 provides an additional demultiplexed read timing feature called "Early Sample". This feature is shown in the corrected **Figure 12-6** and controlled via bit 26 (called ES for "Early Read Sample Select") in register EBU_BUSCONx. EBU_BUSCONx.ES must be added as described on **Page 9**).

Due to this new feature, the paragraph starting with "Phase 2: ..." on page 12-21 must be replaced by the following description:

- "Phase 2: This cycle is always part of a read access. Please note that the read signal is deactivated (high) on the falling edge of CLKOUT. The data input is sampled and latched with this clock edge (EBU_BUSCONx.ES = 0) or with the rising edge of CLKIN when early sample is enabled with EBU_BUSCONx.ES = 1."

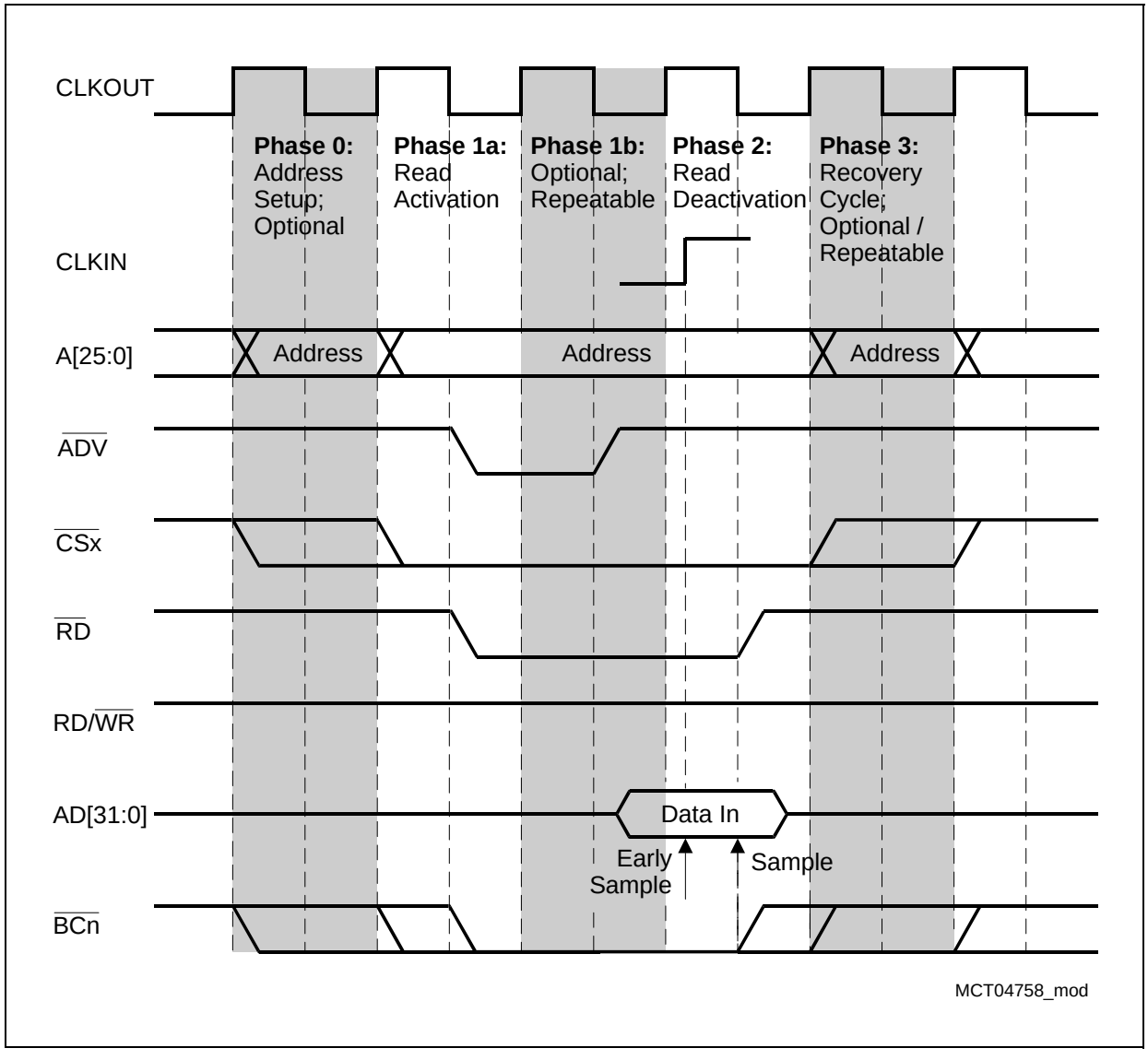


Figure 12-6 Basic Read Access Timing in Demultiplexed Mode

EBU_BUSCONx (x = 3-0)

EBU Bus Configuration Register x **Reset Value: E802 61FF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WR DIS	ALEC		BCGEN		ES	AGEN		CMULTR		WAIT		WAI TINV	SET UP	PORTW	
rw	rw		rw		rw	rw		rw		rw		rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WAITRDC							WAITWRC			HOLDC		RECOVC		CMULT	
rw							rw			rw		rw		rw	

ES	26	rw	**Early Read Sample Select** 0 Reads are performed with regular timing. Data is sampled with the falling edge of CLKOUT. (default after reset) 1 Early read sampling of data is enabled. Data is sampled with the rising edge of CLKIN.

Page 12-44, Update of Figure 12-16

Figure 12-16 should be update with the following drawing:

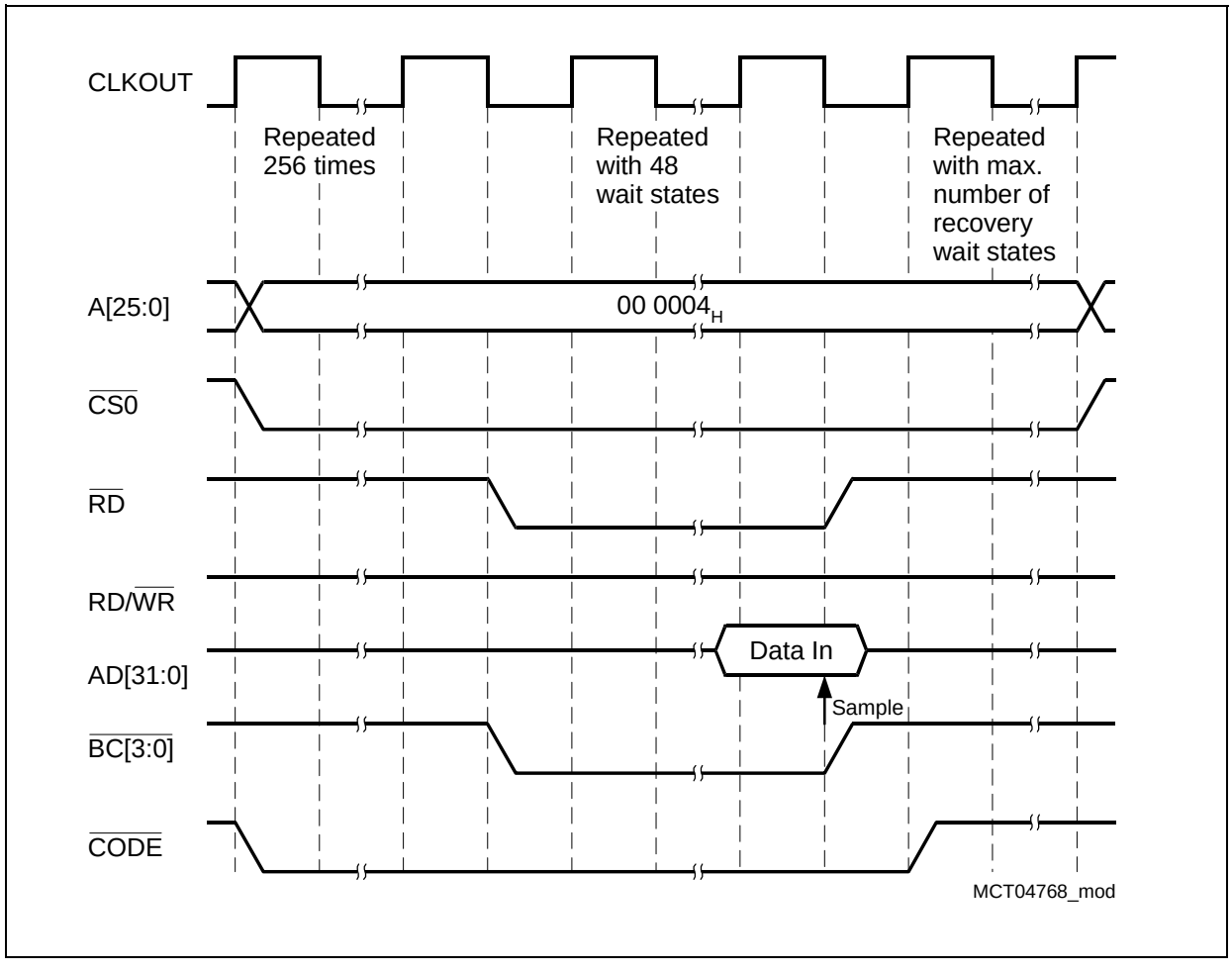


Figure 12-16 EBU Boot Process after Reset

Page 12-61

Bit EBU_ADDSELx.REGEN is of type "rw" instead of "r". It can be written, of course.

Page 12-70

The correct reset value of EBU_EXTCON should be 3C08 0240_H.

Page 14-4

"Note" paragraph should be deleted and its text (sentence) should be added to the table footnote [1] (at its end).

Page 14-12, Section 14.4.1, second paragraph

In the first sentence "The CPU detects a zero-to-one transition of the NMI input signal..." should be corrected into "The CPU detects a one-to-zero transition of the NMI input signal"

Page 14-13

The following "Note" paragraph should be added to the description of bit NMIEXT:

Note: This bit is reset after an exit from Deep Sleep Mode through pin NMI when bit PMG_CON.DSRW has been set before (full reset sequence executed).

Page 15-7, Section 15.3.1.3

In this paragraph "R5 and R6" should be replaced by "R4 and R5".

Page 15-80

Description of SUB.F instruction should be corrected form "Subtract the sign-extended contents ...." into "Subtract the zero-extended contents ....". Further, the "Operation" code should be "R[b] = R[b] - zero_ext(FPI[R[a]])".

Page 16-7, Table 16-2

The definition for the acknowledge code ACK must be corrected into:

ACK = 01_B: SPT
ACK = 10_B: RTY
ACK = 11_B: ERR

Page 16-8, Table 16-4

In the TC1775, block transfers are not used by the FPI Bus master units. Therefore, Table 16-4 with the last sentence of the paragraph above will be modified into:

"Note that block transfers (OPC = 0100_B to 0110_B) and split transactions (OPC = 1000_B to 1110_B) are not used in the TC1775.

Table 16-4 FPI Bus Operation Codes (OPC)

OPC	Description	OPC	Description
0000_B	Single Byte Transfer (8-bit)	**1000_B**	Split Block Transfer Request (1 transfer)
0001_B	Single Half-Word Transfer (16-bit)	**1001_B**	Split Block Transfer Request (2 transfers)
0010_B	Single Word Transfer (32-bit)	**1010_B**	Split Block Transfer Request (4 transfers)

Table 16-4 FPI Bus Operation Codes (OPC) (cont'd)

OPC	Description	OPC	Description
0011_B	Single Double-Word Transfer (64-bit)	1011_B	Split Block Transfer Request (8 transfers)
0100_B	2-Word Block Transfer	1100_B	Split Block Response
0101_B	4-Word Block Transfer	1101_B	Split Block Failure
0110_B	8-Word Block Transfer	1110_B	Split Block End
0111_B	Reserved	1111	No operation

Note: Shaded FPI Bus transactions are not used in the TC1775."

Page 17-1, Bullet list

The two points in the bullet list:

- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

should be replaced by the following three bullet points:

- Counting starts automatically after a reset operation
- STM is reset under following reset causes (see also Chapter 5.3):
  - Wake-up reset (PMG_CON.DSRW must be set)
  - Watchdog reset
  - Software reset (RST_REQ.RRSTM must be set)
  - Power-on reset
- STM is not reset at a hardware reset ($\overline{\text{HDRST}}$ = 0)

Page 18-2

The first sentence of the last but one paragraph "Double Reset Detection" must be replaced by the following sentence:

"If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1775 is held in reset until a power-on reset or hardware reset occurs."

Page 18-18

The second paragraph "Double Watchdog Errors are detected ....." must be replaced by the following paragraphs:

"The purpose of the Double Watchdog Error feature is to avoid loops such as: Reset - software does not start correctly - prewarning - watchdog reset - software does not start correctly - ....."

The WDT has an internal counter that generates internally a constant reset after a second watchdog error. This counter can be cleared only by external reset sources (power-on reset or hardware reset)."

Page 18-29

In table cell "Field", bit name for bit 0 should be "ENDINIT".

Page 20-27

The functionality described in section 20.4.5 "Trace with External Bus Address" is not available. Therefore, this section must be deleted.

Page 21-1, Table 21-1

The definition of "U" must be changed into:

"Access permitted in User Mode 1 only.

Page 21-10

In Table 21-4, a "32" should be added to the "Access Mode" "Read" and "Write" cells for PCP Data Memory and PCP Code Memory (as in Table 15-14 on page 15-93).

Pages 21-21 and 21-21

The long name (description) of registers TB and RB in Table 21-5 must be corrected:

– SSC0_TB = "SSC0 Transmit**ter** Buffer Register"
– SSC0_RB = "SSC0 Receive**r** Buffer Register"
– SSC1_TB = "SSC1 Transmit**ter** Buffer Register"
– SSC1_RB = "SSC1 Receive**r** Buffer Register"

Page 21-46 and 21-51

The long name (description) of registers MSS0 and MSS1 in Table 21-5 must be corrected:

– ADC0_MSS0 = "ADC0 **Module** Service Request Status Register 0"
– ADC0_MSS1 = "ADC0 **Module** Service Request Status Register 1"
– ADC1_MSS0 = "ADC1 **Module** Service Request Status Register 0"
– ADC1_MSS1 = "ADC1 **Module** Service Request Status Register 1"

3 User's Manual - Peripheral Units Part

Page 2-12, Second paragraph

"± 16" and in asynchronous modes and "± 4" should be replaced by "÷ 16" and "÷ 4".

Page 2-24

"FDV contains the .." should be corrected into "FD_VALUE contains the ...".

Pages 2-25 and 2-26

The long name (description) of registers TBUF and RBUF in must be corrected:

– TBUF = "Transmit Buffer Register"
– RBUF = "Receive Buffer Register"

This correction also requests a change on the bottom of pages 1-7 and 2-3: correct is "... On a transmit buffer .." and " ... On a receive buffer ..".

Pages 3-21

The long name (description) of registers TB and RB in must be corrected:

– TB = "Transmit Buffer Register"
– RB = "Receive Buffer Register"

Page 3-18

After the last paragraph (and therefore before the note on the next page), the following paragraph should be added for clarification:

"When a disabled module is switched on by writing an appropriate value to its MOD_CLC register, status bit DISS changes from 1 to 0. During the phase, where the module becomes active any write access to corresponding module registers (when DISS is still set) will generate a bus error. Therefore, when enabling a disabled module, application software should check after activation of the module once whether DISS is already reset, before a module register will be written to."

Page 5-8

Typo: second paragraph "The SDLM ..." under 5.1.4.3: "... Bus-side receive buffer ..."

Page 6-39 and 6-40

Bits T2ADIR and T2BDIR should be marked as "rh" instead of "rw".

Page 7-52

3. paragraph from the top “Note: ...”: in this Note paragraph, “GTC” and “GTCXR” must be replaced by “LTC” and “LTCXR”.

Page 7-84

The code

```
if (GTCk.Capture_opposite_timer) then
   GTCk.X = GTm.Timer
else ......
```

must be corrected into

```
if (GTCk.Capture_opposite_timer) then
   GTCk.X = GT!m.Timer
else ......
```

Page 7-90

Table row “LTCk.X_write_access”: comment “Internal value set to indicate the LTCk.X was modified ....“ is extended into “Internal value set to indicate the LTCk.X was modified (written, incremented, or reset) ....”

Page 7-96

Bit 0 to 5 of FPCCTR1 are “rwh” bits (not “rw” bits). The paragraph ““Bit protection is ...” in the bit description will be completed by: “(see also Note on **Page 7-124**).” The Note on page 7-124 is described at section **“Page 7-124 to 7-126”** of this document.

Pages 7-99 and 7-100

Bits PDLCTR.ERR0 and PDLCTR.ERR1 are "rh" instead of "rw".

Page 7-104

The bit description for bit PLLCTR.PEN must be completed with the following sentence: “Bit protection is implemented for PEN to allow read-modify-write instructions. (see also Note on **Page 7-124**).”. The Note on page 7-124 is described at section **“Page 7-124 to 7-126”** of this document.

Page 7-109

Description of bit field GTCTRm.MUX should be extended as follows:

```
000 = Clock bus line CLK0 selected
001 = Clock bus line CLK1 selected
010 = Clock bus line CLK2 selected
011 = Clock bus line CLK3 selected
```

100 = Clock bus line CLK4 selected
101 = Clock bus line CLK5 selected
110 = Clock bus line CLK6 selected
111 = Clock bus line CLK7 selected

Page 7-118

Description of bit field LTCTRk.OCM must be corrected as follows:

OCM = $X11_B$: LTCk data output line is forced with 1.

Page 7-124 to 7-126

The type of all "rw" bits of registers SRS0, SRS1, SRS2, and SRS3 must be changed into "rwh". Further the following footnote must be added to "rwh" bits in the register bit description tables: "Bit protection is implemented to allow "read-modify-write" instructions."

Page 7-124 on top, below paragraph "7.2.11 ...": the following note paragraph will be added:

Note: The write protected bits in the Service Request State Registers are not changed during a read-modify-write instruction, i.e. when hardware sets e.g. an request state bit between the read and the write of the read-modify- write sequence. It is guaranteed that only the intended bit(s) is/are effected by the write-back operation.

Page 8-34

The first formula on this page should be replaced by

"$V_{AREF}[0] \leq V_{DDA} + 0.1V$; $V_{DDA} \leq 5V$"
"$V_{AREF}[0] \leq V_{DDM} + 0.05V$; $V_{DDM} \leq 5V$"

Further on the bottom the relation should be corrected into

"$0\ V \leq V_{AREF} \leq V_{DDM} + 0.1\ V$"
"$0\ V \leq V_{AREF} \leq V_{DDM} + 0.05\ V$"

At the bottom of this page, the following two additional notes should be added:

Note: Is is not recommended in general to set V_{AREF} below 50% of V_{DDM}.

Note: The analog input voltages V_{AIN} must be in the range between V_{AGND} and the selected V_{AREF}.

Page 8-41

The 2nd sentence in section "8.1.8.3 Timing of external Multiplexer" is extended:

"Therefore, the information to drive an external multiplexer is available one f_{ADC} clock before the sample time begins".

Page 8-56 and 8-57

The register long name of MSS0, MSS1, and SRNP in Table 8-13 must be corrected:

– MSS0 = "Module Service Request Status Register 0"
– MSS0 = "Module Service Request Status Register 1"
– SRNP = "Service Request Node Pointer Register"

4 Data Sheet

Page 59, Table 8

The following footnote [2] must be added to header cell "f_{SYS}" of Table 8:

[2] Depending on the selected system frequency f_{SYS}, the number of clocks for interrupt arbitration cycles must be selected as follows: $f_{SYS} \leq 30$ MHz: ICR.CONECYC = 1, $f_{SYS} > 30$ MHz: ICR.CONECYC = 0.

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