Application Note

CS8900A FREQUENTLY ASKED QUESTIONS

1. Application Note 181 says that interrupts are not supported in 8-bit mode. Is this really true?

Yes, this really is true. Interrupts are NOT supported in 8-bit mode. They might appear to work for a while but will eventually fail.

2. What free TCP/IP software does Cirrus Logic provide for use with the CS8900A?

None. Some recommended sources for TCP/IP are US Software, http://www.ussw.com/products/introduction/tcpip/ and Interniche, http://www.iniche.com/products/tcpip.htm. Both have products that are CS8900A compatible.

3. I see that the CS8900A has I/O mode and Memory Mode. Is there a performance advantage to using Memory Mode?

I/O Mode is 99.6% as fast as Memory Mode. Also, since the CS8900A defaults to I/O AND you don't need glue logic in most systems in I/O Mode Cirrus recommends I/O mode.

4. I just got my boards back and I want to verify operation of the CS8900A. What do I do?

First plug in a 10BaseT cable from the RJ-45 on your device to a hub. Check for a link light on both sides.

Next read the Packet Page Data Port (Offset 0xC from the CS8900A base address in your system, I/O Mode). You should get 0x0E63 or 0x630E (depending on byte ordering of your processor).

Next write 0x0102 to Packet Page Pointer Port (Offset 0xA). Read the Packet Page Data Port. You should get 0x3.

5. When I read from the CS8900A I get garbage data.

First get a copy of Application Note 83 from the Cirrus web site. Check your schematic against the schematic checklist on page 4. If there is no link light (see item 4) then you have a hardware problem since the CS8900A should link with just power on.

Also, check your timing. TIOR2, TIOR3, TIOW2 and TIOW3 are the key timing parameters you must meet. For example -- You must provide 10nS of address/AEN stable before IOR# goes active.

6. What is the input and output capacitance of the CS8900A pins?

Input Capacitance CIN Max=10pF

Output Capacitance COUT Max=20pF

Input/Output Capacitance CIO Max=20pF

CIRRUS LOGIC
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

7. I need the algorithm to program the Hash Table Filter.

You can download a sample program from the CS8900A drivers page. Go to the Cirrus web site, http://www.cirrus.com/Drivers/ethernet/ethernet.cfm. Download "hash.zip."

8. What are Theta J/A and Theta J/C for the CS8900A?

Theta J/A = 37.7 C/w (0 m/s air flow) Nominal

Theta J/C = 2.2 C/w (0 m/s air flow) Nominal

9. Does Cirrus supply MAC addresses?

No. You need to get MAC address from IEEE. Go to http://standards.ieee.org/regauth/oui/index.shtml to apply for a company identifier from IEEE. A MAC address (sometimes called an Individual Address) is made up of a 3 byte company identifier and a 3 byte number assigned by the company.

That is IEEE will give your company a unique 3 byte number. Then for every device manufactured your company will assign the last 3 bytes of the number.

10. Do I need an EEPROM in my design?

No. When there is no EEPROM then the CS8900A will default to I/O Base Address 0x0300. You will need to store the MAC address somewhere in FLASH or other non-volatile memory.

11. Do you have a sample connection diagram for my processor?

There are several connection diagrams shown in Application Note 83. These include a 68302, ARM 7 and Hitachi SH3. There are so many processors that it is impossible to have a sample for every one. Please read "CS8900A: Connecting to non-ISA Bus Systems" in Application Note 83.

12. What is the MTBF for the CS8900A?

We have Op-Life Qual data for rev B, C, and D of CS8900A.

Rev B: 1161 devices, 500 hours, 0 failure. -> 26 FIT -> 38,400,000 MTBF

Rev C: 315 devices, 168 hours, 0 failure. -> 280 FIT -> 3,570,000 MTBF

Rev D: 315 devices, 168 hours, 0 failure. -> 280 FIT -> 3,570,000 MTBF

Rev C/D combined: 730 devices, 168 hours, 0 failures. -> 140 FIT -> 7,140,000 MTBF

Rev B has much better FIT result because the production Qual plan for rev C/D did not require as high of a sample size and stress duration.

There were only minor metal rev changes from Rev B to Rev D. Rev D is the current shipping version.

13. In the sample connection diagrams I see SHBE# and AEN connected to a chip select from the processor. Also, only 3 address lines are connected. Why?

Let's cover this one at a time.

SBHE# must toggle to put the CS8900A into 16-bit mode. SBHE# is guaranteed to toggle when connected to CS#. It will always be low during a read or write of the CS8900A. This also means that you can only do 16-bit reads or writes. No 8-bit accesses.

AEN can be used as an active low chip select when DMA is not used.

When the CS8900A powers up with no EEPROM it defaults to I/O Mode with a Base Address of 0x0300. This is why address lines [A9:A8] are tied high.

So, the CS8900A always sees 0x30x on its address lines. Reads and writes are gated by using AEN as a chip select.

Since accesses are always 16-bit how does the CS8900A handle odd length frames?

When sending an odd length frame software will still "bid" for the odd number of bytes. Software will do (frame bytes + 1)/2 16-bit writes to the CS8900A. The CS8900A will ignore the extra byte.

When reading an odd length frame software will do (frame bytes + 1)/2 16-bit reads. Software will pass the correct frame length to the upper layer. The upper layer will ignore the extra byte.

14. How do I program the EEPROM connected to the CS8900A?

You can download a sample program from the CS8900A drivers page. Go to the Cirrus web site, http://www.cirrus.com/Drivers/ethernet/ethernet.cfm. Download "mfg.zip."

15. The spec defines VIXH (page 111, XTAL1 input high voltage when operating with external clock) as 3.5 Volt min. I presume this is for a VDD of 5V. What is VIXH for a VDD of 3.3V?

The spec for 3.3V operation is 2.4V.

16. Where can I get pricing and availability information for the CS8900A Integrated Circuit or the CRD8900A-1 Eval. Board kit?

You can contact: Insight Electronics at: 1-800-677-7716 or Nu-Horizons at: 1-631-396-5000. You can also request a sample by going to http://www.cirrus.com and clicking on “samples” in the left column.

17. I have ordered the CRD8900A-1 kit , and would like the data sheets/specs for this evaluation board. Where can I locate them?

Information on the CS8900 reference design board is in app note AN83, starting on page 15: http://www.cirrus.com/pubs/an83.pdf?DocumentID=260.

18. We received CS8900A-IQ, through a distributor, in moisture sealed packaging. There was no Jedec Moisture Level markings on the package. Is there a moisture sensitivity rating?

This product is qualified to Jedec Level III.

19. Where can I find drivers for the Cs8900, Cs8920, Cs8900a?

Our CS8900 drivers are available on the internet at:
http://www.cirrus.com/Drivers/ethernet/ethernet.cfm.

20. I'm connecting the CS8900A to a big endian processor and have switched the high and low order byte connections (D8:15 -> D0:7 and D0-7 -> D8:15). I want to be sure that I maintain byte order when doing a memory space transfer of packets, but require byte swapping when writing to the control registers on the ethernet controller.

The CS8900 assumes a "little-endian" ISA-type system. However, network byte order is always big-endian. Therefore to minimize software manipulation of frame data in ISA systems, the CS8900 byte-swaps frame data internally. The control and status registers are not byte swapped.

In a big-endian system (e.g. Motorola) you can either byte-swap the network data (to reverse the byte swapping done internally to the CS8900) in software or you can do it in hardware (byte swap the data lines to the chip). Byte swapping the data lines is much more efficient; you will only need to byte swap the control/status/counter values in software and not the frame data. (Most of the read/writes to the chip are frame data.) Since network byte order is always big endian this scheme works without special support on the other end of the network.

21. I want to make an embedded system with cs8900a using 8 bit mode. Do you have some generic C code available with examples of polling mode ?

We have available at our web site at: http://www.cirrus.com/Drivers/ethernet/ethernet.cfm -the VxWorks driver with source code. Porting to 8-bit mode is the customer's responsibility.

22. What is the simplest way of getting my CS89000A up and running if I am using an embedded ethernet application?

Download our loop.zip file . Read the readme file first to get instructions on how to construct a loopback connector and run this file. Please note that for external loopback mode to work you may need to set the full duplex(fdx) bit in testctl. This should give you simple receive and transmit capability with the CS8900A using the Embedded processor of your choice.

23. The schematics in the app notes show that there are .01uF 2kV capacitors going pins 15 and 10 of the transformer to ground. These parts are marked DO NOT STUFF. Is the purpose of these caps to prevent EMI / ESD emissions/susceptibility?

It's there to help EMI issues. The reason for the 2KV rating is that that side of the transformer should withstand 1500Vrms for 1 minute. Also, it is OK to substitute .01uF caps instead of .1uF caps. The only required capacitor is on pin 7, the center tap for TX+/-.

24. I can get a link with a 10Mb hub but I get no link with a 10/100Mb hub or switch.

Clear bit 9, AutoAUI/10BT, in the LineCTL register. Here's what is happening: When the AutoAUI/10BT bit is set, the CS8900A waits for signal on either the AUI port or the 10BaseT port. It does not send out any link pulses on the 10BaseT port. The 10/100 hub is sending out Fast Link Pulses. The CS8900A doesn't interpret Fast Link Pulses as a valid signal so it never switches to 10BaseT mode. When you clear the AutoAUI/10BT bit then the CS8900A will send Normal Link Pulses which will cause the 10/100 hub to switch to 10BaseT mode.

25. It says that we should wait 10ms after a reset to access registers. It also indicates that InitD is set and SiBusy is clear reset when reset is complete. Does this mean that I can poll the Self Status register through the I/O Map instead of creating some sort of firmware delay to determine when the controller's other registers can be accessed?

Yes you can poll Register 16 (self status) instead of insert delay time. In fact this is a better way than inserting a delay. INITD=high will tell you when initialization is complete. SIBUSY=0 will let you know that the EEPROM is being accessed.

26. I've written my own driver for the CS8900A. Eventually the chip stops receiving data and all I get are RxMiss events. What can cause this?

If you issue a skip command before reading the status and length of the frame the internal buffers may not clear properly. So, before issuing a skip command read the RxStatus and RxLength of the current frame.

27. I get a lot of TxUnderRun errors but I'm not using early transmits. I didn't think you could get this kind of error without using early transmits.

The TxUnderRun error can occur if you do not limit the transmit path of your driver. You should modify the driver so that only one transmit is allowed to be in progress at a time. Set Tx Interrupts using the TxCFG register. Then use the TxEvent to indicate that the current Tx operation is complete before starting the next one. You can see how this can be done in our sample drivers.

28. Is the CS8900A-CQ3 5V tolerant?

The CS8900A-CQ3 and -IQ3 are not 5V tolerant. There are voltage protection diodes on all I/O lines that will turn on whenever the voltage on the I/O line is greater than V_{dd} + .7V or less than V_{ss} - .7V.

29. I'm laying out my board and I need to know what kind of traces to use on the transmit and receive lines. Are there different requirements for 3.3V or 5V operation?

The recommended trace characteristics are the same for 3.3V and 5V operation. TX+ and TX- should be 25Ω single ended transmission line traces to the transformer. RX+ and RX- should be 50Ω single ended transmission line traces to the transformer. Traces from the transformer to the RJ45 should be 50Ω. Keep the TX series resistors, cross over cap and RX terminating resistor close to the CS8900A.

Note that in 3.3V mode the TX series resistors are either 7.9Ω or 8.1Ω. One would also try to make the TX+/- traces the same impedance as the series resistors. However, the traces get exceedingly wide and the 25Ω is a good compromise.


SMART
Analog
™