3.0 Volt-only Burst Mode Flash Memory Technology

Introduction

AMD, the technology leader in Flash memories, has developed a new generation of high-performance, single-power-supply flash memory devices. The Am29BL162C device is the first burst mode low-voltage flash memory device from AMD. This device allows read access times as fast as 18 ns, while performing read, program, and erase operations using only a single 2.7 volt power supply. This device offers all of the features of AMD's industry-standard 2.7 volt-only Am29LVxxx devices with substantially faster access times, making it the ideal choice for low-power, high performance applications. In addition, this device is 5 volt I/O tolerant, allowing it to be easily used in 5 volt systems. The Burst Mode interface of the Am29BL162C has been designed with inputs from industry-leading microprocessor manufacturers, simplifying the design-in process for system designers.

The following is an abbreviated list of the Am29BL162C distinctive characteristics:

- ❑ 18 ns burst access time
- ❑ 65 ns initial access time
- ❑ 2.7 V to 3.6 V device V_{CC} operating range
- ❑ 5 V I/O tolerant on data, address, and control signals
- ❑ 32 word-linear burst sequence
- ❑ Minimum 1,000,000 program/erase cycle guarantee per sector

For a complete list of features, operational description and specifications see publication number 22142 (Am29BL162C data sheet).

In a typical embedded application, the memory system may contain DRAM for code execution and Flash for control code storage. The control code is typically downloaded from the flash and executed from DRAM to take advantage of the faster read access times of DRAM. With the fast data access of the Am29BL162C, the need for this shadow DRAM is eliminated in many cases, and the code can be executed directly from the flash memory. This allows the CPU's read cycle to be maximized and lowers the overall system cost by eliminating the redundant DRAM.

In addition, many of today's systems still operate at mixed voltages. This is due, in part, to 5.0-volt devices that must be used on the board, such as ASICs, processors, etc. As these devices often control the system data and address buses, the system bus must operate at 5.0 volts. In order to interface these buses to lower-voltage memory devices, voltage translators must be designed into the system to translate the higher system bus voltage down to the lower voltage tolerated by the memory device. The Am29BL162C has 5 volt I/O and control signal

tolerance, so that DC-to-DC converters are no longer required. This leads to lower overall system cost.

Block Diagram

Internally, the Am29BL162C is designed with the same leading-edge design as the traditional 29LVxxx family of devices, with some additional read control logic. This read control logic was modified to allow the flash device to provide a seamless burst interface and allow 18 ns burst access times. This additional logic is incorporated into the burst state controller and burst address counter blocks in the block diagram below.

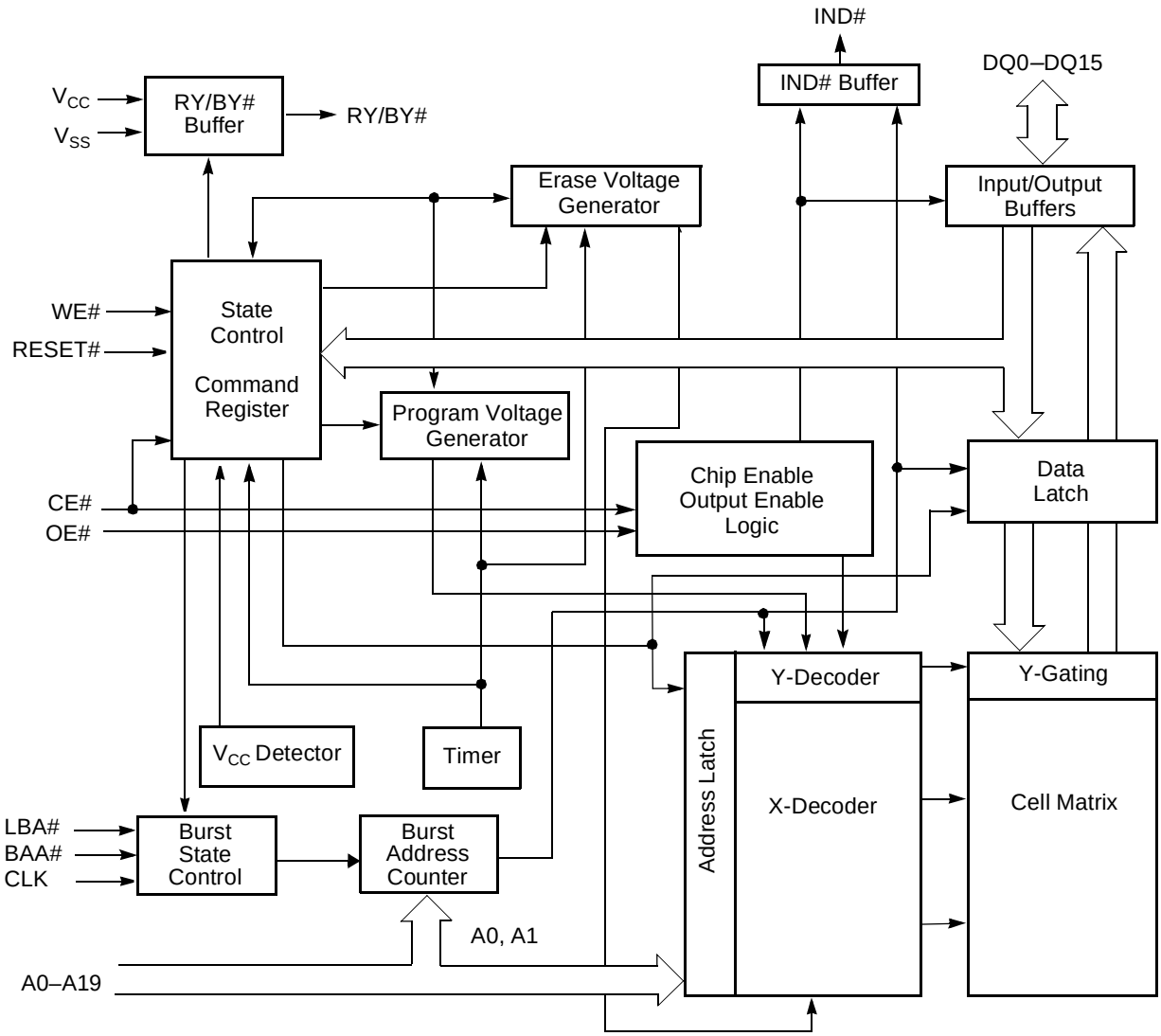

Figure 1. Am29BL162C Block Diagram

Read Operation

The Am29BL162C will power-up in an “asynchronous read” operating mode. In this mode, the device operates like a conventional Flash device (Am29LVxxx) and supports only asynchronous, random reads, not synchronous burst reads. To support burst reads, the Am29BL162C must be put into the bust mode by writing the Burst Enable command sequence. To exit the burst mode, the device must be given the Burst Disable command sequence.

Random Read Operation

In the asynchronous mode the Am29BL162C has two control functions which are used to obtain data at the outputs. CE# should be used for device selection. OE# is the output control and should be used to gate data to the output pins after the device is selected.

Burst Mode Read Operation

In order to operate in burst mode, three additional control pins have been added. These control pins allow easy interfacing to a wide range of microprocessors with minimal glue logic to achieve high performance burst read capability. These additional pins are as follows: Load Burst Address (LBA#), Burst Address Advance (BAA#), and Clock (CLK).

The burst mode read operation is a synchronous operation tied to the rising edge of the clock. The microprocessor or microcontroller supplies only the initial address. All subsequent addresses are automatically generated by the device at the rising edge of subsequent clock cycles by asserting the BAA# signal.

The burst read cycle consists of an address phase and a corresponding data phase. During the address phase, the Load Burst Address (LBA#) pin must be held low for one clock period. At the rising edge of CLK, the starting burst address is loaded into the internal burst address counter.

During the data phase, the first burst data is available after the initial access time (t_{ACC}) from the rising edge of CLK. For subsequent burst data, an active Burst Address Advance (BAA#) and the rising edge of the CLK will increment the counter and supply the remaining data in the appropriate sequence in the specified burst access time (t_{BACC}). The stream of data will be provided as long as the BAA# pin is asserted.

The timing diagram in Figure 2 demonstrates this burst mode operation.

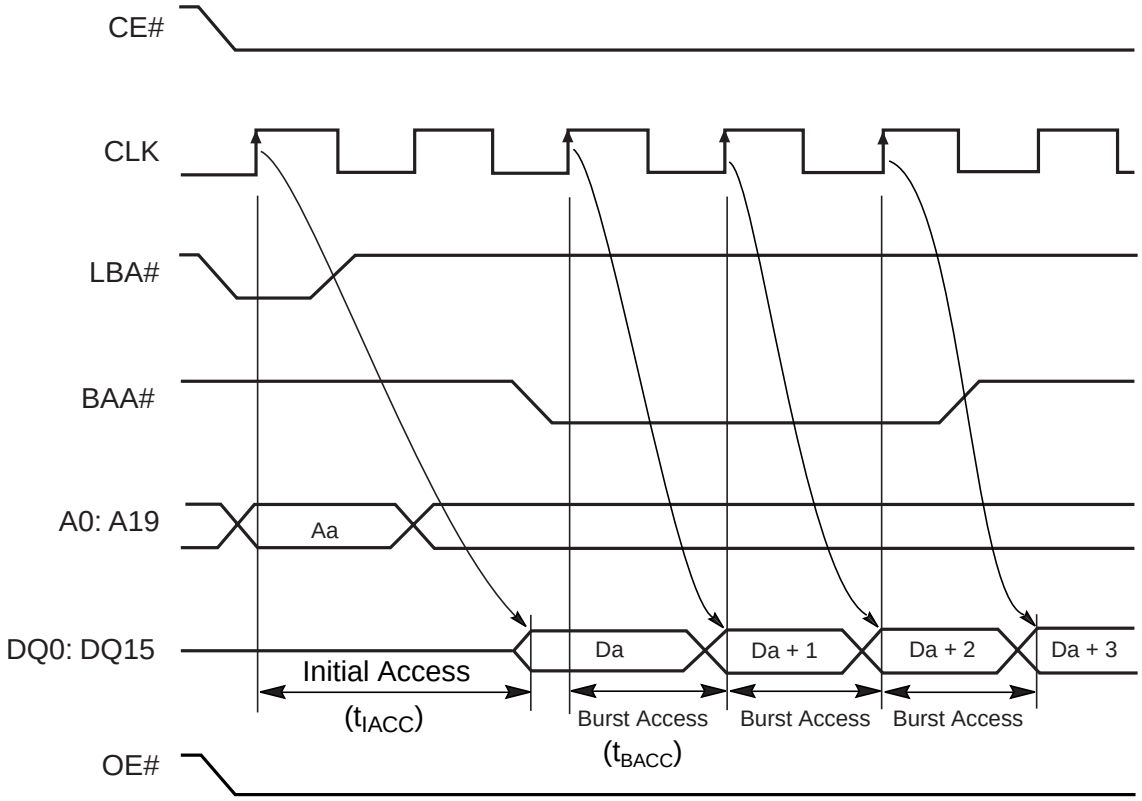

Figure 2. Burst Mode Read Operation

Burst Configuration

The Am29BL162C provides a 32 word sequential burst and is used to support microprocessors that implement an instruction pre-fetch queue and to support large data transfers during system configuration.

In this linear mode, the Am29BL162C will deliver a continuous sequential word stream starting at the specified word and will wrap around when the end of the 5 bit counter is reached (11111). For example, if the initial address is xxxx0h, the data order will be 0-1-2-3…. 28-29-30-31-0-1…; if the initial address is xxxx2h, the data order will be 2-3-4-5…..28-29-30-31-0-1-2-3…; and if the initial address is xxxx8h, the data order will be 8-9-10-11….30-31-0-1-2-3-4-5-6-7-8-9….Data will be repeated if more than 32 clocks are supplied.

IND#: End of Burst Indicator

This active low output signal indicates the end of the burst sequence. It has the same output driving characteristic as the typical data output DQ signal. It becomes low in the same data output cycle as the last word in the burst sequence.

For processors that do not wish to receive wrap around data, the LBA# and a new address need to be issued to the Flash in order to receive data from the next burst range. Wrap around data is defined as the data after last word in the burst range, e.g. word 0, 1, and so on, after word 31 in the 32 word linear mode.

Summary

Technology leadership, experience and creativity of AMD's engineering resources have once again led to the arrival of the next generation of high performance flash memory devices. These burst mode low voltage devices offer burst read access times of 18 ns, with initial access times of 65 ns. The high performance, reduced power consumption, and industry-leading guaranteed minimum endurance of 1,000,000 cycles combine to make this family and ideal choice for cost-sensitive, performance-driven applications.

One AMD Place
P.O. Box 3453
Sunnyvale,
California 94088-3453
USA
(408) 732-2400
(800) 538-8450
TWX: 910-339-9280
TELEX: 34-6306

TECHNICAL SUPPORT
USA & CANADA non-PC CPU: (800) 222-9323
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USA & CANADA PC CPU E-mail: hw.support@amd.com
EUROPE & UK: +44-(0)1276 803299
Fax: +44-(0)1276 803298
BBS: +44-(0)1276 803211
FRANCE: 0800 90 8621
GERMANY: 089-450-53199
ITALY: 1678-77224
EUROPE E-mail: euro.tech@amd.com
FAR EAST Fax: (852) 2956-0599
JAPAN: 03-3346-7550
Fax: 03-3346-7848
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