

# **phyCORE-PXA270**

## **Hardware Manual**

**Edition March 2006**

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 <a href="mailto:order@phytec.de">order@phytec.de</a>	1 (800) 278-9913 <a href="mailto:sales@phytec.com">sales@phytec.com</a>
Technical Support:	+49 (6131) 9221-31 <a href="mailto:support@phytec.de">support@phytec.de</a>	1 (800) 278-9913 <a href="mailto:support@phytec.com">support@phytec.com</a>
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	<a href="http://www.phytec.de">http://www.phytec.de</a>	<a href="http://www.phytec.com">http://www.phytec.com</a>

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## Preface

This phyCORE-PXA270 Hardware Manual describes the board's design and functions. Precise specifications for the Intel PXA270 microcontroller series can be found in the enclosed PXA270 microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /OE). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

### **Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-PXA270**



PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

#### **Note:**

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-PXA270 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

- (1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
- (2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.



## **1 Introduction**

The phyCORE-PXA270 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-PXA270 is a subminiature (70 x 57 mm) insert-ready Single Board Computer populated with Intel's Xscale PXA270 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the module can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the PXA270 controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-PXA270.

**The phyCORE-PXA270 offers the following features:**

- Single Board Computer in subminiature form factor (70 x 57 mm) according to phyCORE specifications
- All applicable controller and other logic signals extend to two high-density 160-pin Molex connectors
- Processor: Intel XScale PXA270 max. 520 MHz clock
  
- **PXA270 Core Features:**
  - 32-bit ARM™ Core Version 5TE ISA compliant
    - ARM thumb instruction support
    - ARM DSP enhanced instructions
  - Intel Media Processing Technology
    - Enhanced 16-bit multiply
    - 40-bit accumulator
  - Intel Wireless MMX Coprocessing Technology
    - SSE Instructions set
    - 64-bit architecture with 16 Registers
  - 32 kB data and 32 kB instructions cache
  - 2 kB mini data and 2 kB mini instructions cache
  - 256 kB on-chip SRAM
  - Instructions and Data Memory Management Unit
  - Branch target buffer
  - Debug Capability via JTAG Port
  - 0-520 MHz CPU speed
  - Low-power consumption and high performance
  - Special I<sup>2</sup>C Powermanagement bus

- **PXA270 System Features:**

- Memory controller with DMA
  - 4 \* SDRAM 64 MB each
  - 4(5) \* SRAM, FLASH ROM (4 of which sync.)
- Clock and Power Controllers
- USB Client Interface and Host Interface
- 2 \* PCMCIA / Compact Flash
- 2 \* MMC card resp. SD card and MemoryStick
- Interface for SIM-Cards
- LCD controller
- Matrix Keyboard Controller
- Quick Capture Interface for CMOS image sensor
- AC97 / I<sup>2</sup>C controller
- 4 UARTs
- Synchronous Serial Protocol ports (SSP and NSSP)
- I<sup>2</sup>C interface
- Mobile Scalable Link for Highspeed Communication
- 4 \* PWM
- RTC
- OS timer
- General purpose I/O pins (GPIO)
- Interrupt control

- **phyCORE-PXA270 Memory Configuration<sup>1</sup>:**

- SDRAM: 64 MByte (128 MByte) 32-bit 100 MHz
- Flash-ROM: 32 MByte (8 MByte, 16 MByte, 64 MByte)  
synchronous/ asynchronous 32-bit (16-bit)
- I<sup>2</sup>C EEPROM 4 kByte

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<sup>1</sup> Please contact PHYTEC for more information about additional module configuration options.

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- **phyCORE-PXA270 Features:**

- Power supply for PLL, on-chip SRAM CAN and Core power control via IPM Controller
- Reset control for module and periphery ICs
- SJA1000 CAN controller
- 10/100Mbps LAN91C111 Ethernet controller, 32-bit
- Configuration storage EEPROM for Ethernet controller
- MAX7301 / MAX69577301 GPIO expander
- Full RS-232 transceiver for FF-UART
- Real-Time Clock RTC8564 with wakeup function
- External battery backup for RTC
- 2.0 mm JTAG port on module edge
- Multi-Media card connector
- Two indicator LEDs for system information
- All required Chip Select signals and interrupts can be configured via jumpers on the module

- **phyCORE-PXA270 Operating Systems:**

- Linux
- WinCE 5.0

## 1.1 Block Diagram

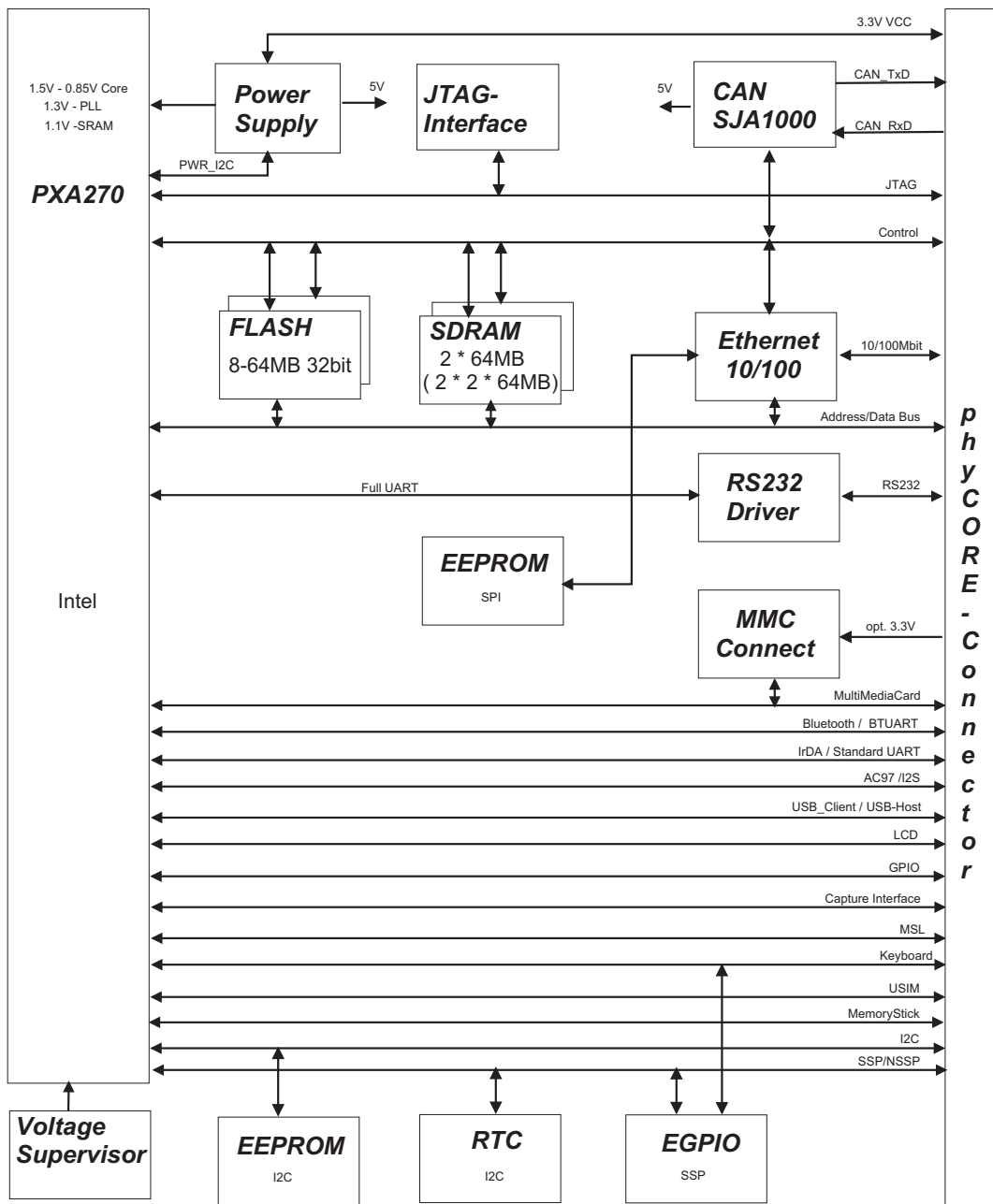


Figure 1: Block Diagram phyCORE-PXA270

## 1.2 View of the phyCORE-PXA270

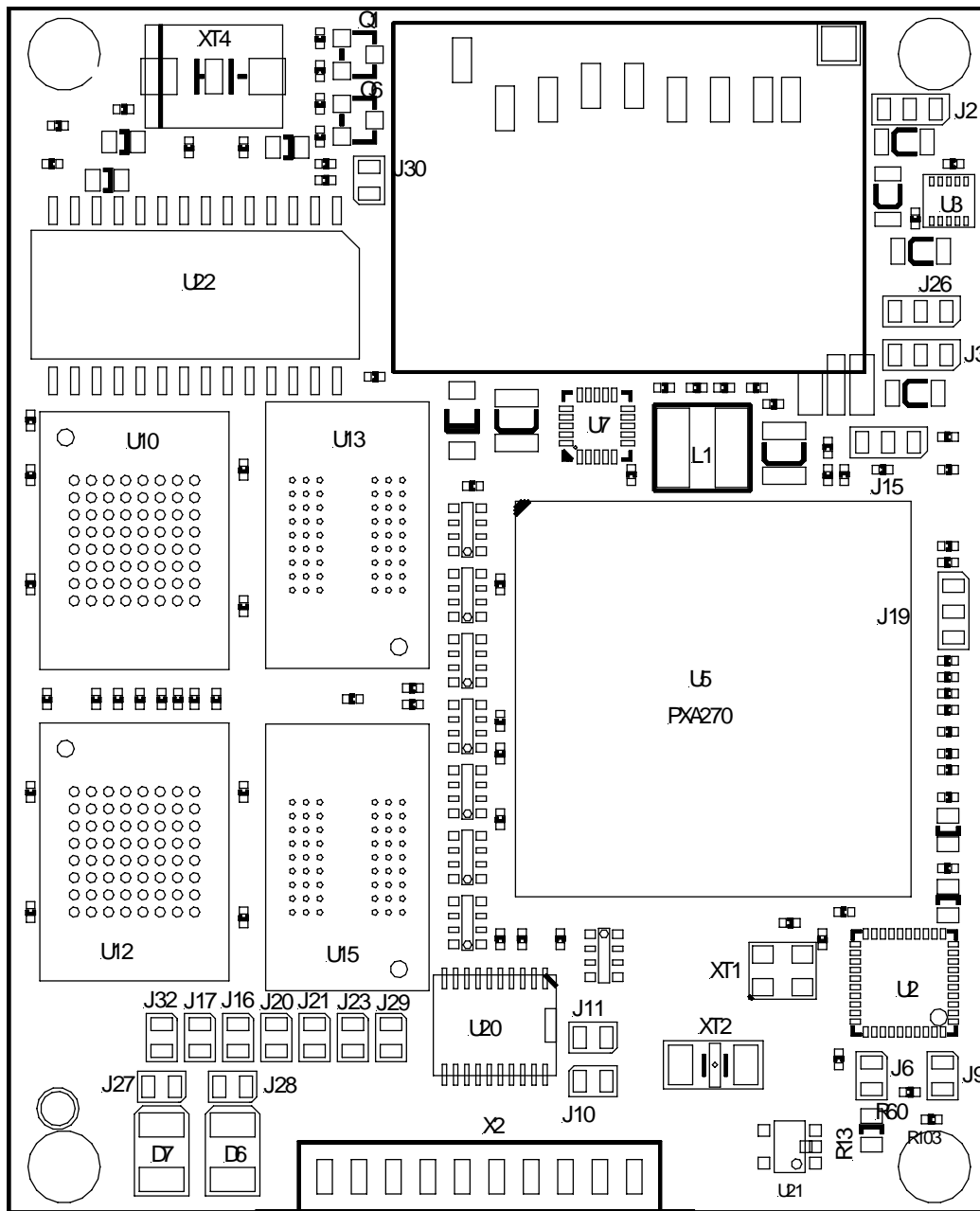


Figure 2: View of the phyCORE-PXA270 (Top), PCB Revision 1235.2

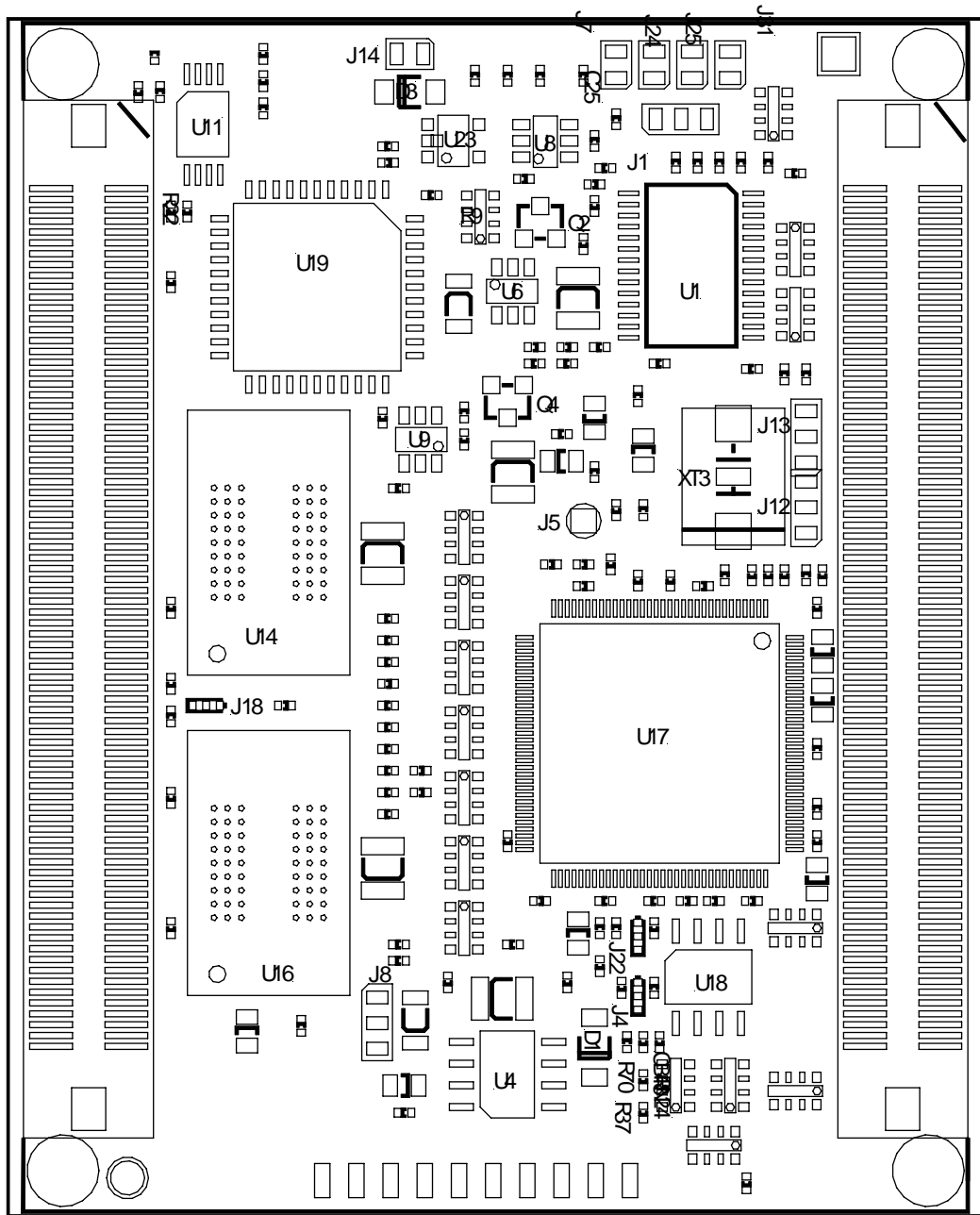


Figure 3: View of the phyCORE-PXA270 (Bottom), PCB Revision 1235.2

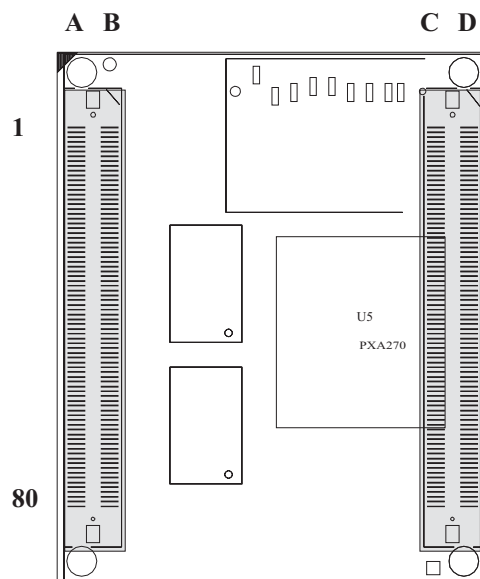




## 2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-PXA270 to be plugged into any target application like a "big chip".



*Figure 3: Pinout of the phyCORE-PXA270 (Top View)*

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector, as well as descriptions of possible alternative functions. Please refer to the Intel PXA270 Electrical, Mechanical and Thermal Specification for details on the functions and features of controller signals and port pins.

Pin Number	Signal	I/O	Comments
<b>Pin Row X3A</b>			
1A	CLKIN	I	Optional external clock input of the processor
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	CLK_REQ	I/O	Indicates Clocksource
4A	GPIO0	I/O	Processor I/O port, <i>alternative: interrupt</i>
5A	/CS_2	I/O	Freely available /CS signal of the processor, <i>alternative: GPIO78</i>
6A	/CS_4	I/O	Chip Select signal of the processor, <i>alternative: GPIO80</i>
8A	/WE	O	Write-enable signal for SDRAM, SRAM and Flash devices. Please note that the /PWE signal must be used for I/O components.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A, 36A	A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23, A24	I/O	Address lines
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	D1, D2, D4, D7, D9, D10, D12, D15, D18, D19, D20, D22, D25, D27, D28, D30	I/O	Data lines
34A, 35A	DQM_1, DQM_2	O	Byte enable signals
48A	RDY	I/O	Ready signal of the processor, <i>alternative: GPIO 18</i>
49A	RDnWR	O	Bus control signal of the processor

Pin Number	Signal	I/O	Comments
<b>Pin Row X3A</b>			
50A, 51A	DREQ_0 DVAL_0	O	DMA request signal DREQ0 <i>alternative: GPIO 115</i> DVAL0 <i>alternative: GPIO 116</i>
53A,	/SDCKE_0	O	Clock enable for synchronous memory
55A, 56A	/SDCLK_0 /SDCLK_1	O	Clock signal for synchronous memory
58A, 59A	/PCE_1 /PCE_2	I/O	PCMCIA Chip Select resp. byte control signal, <i>alternative: GPIO85/54</i>
60A	/PWAIT	I/O	PCMCIA wait signal, <i>alternative: GPIO56</i>
61A	/IOIS16	I/O	PCMCIA 16-bit access <i>alternative: GPIO57</i>
63A	/PREG	I/O	PCMCIA register control signal <i>alternative: GPIO55</i>
64A	/LAN_CS	I	I/O Chip Select for LAN controller
65A	/LAN_DATA	I	DATA Chip Select for LAN controller
66A	L_VSYNC	O	Refresh sync signal from the LCD panel with internal frame buffer <i>alternative: GPIO14</i>
68A	L_PCLK	I/O	LCD pixel clock <i>alternative: GPIO76</i>
69A	L_LCLK	I/O	LCD line clock <i>alternative: GPIO75</i>
70A	L_FCLK	I/O	LCD frame clock <i>alternative: GPIO74</i>
71A	L_BIAS	I/O	LCD enable <i>alternative: GPIO77</i>
73A, 74A, 75A, 76A, 78A, 79A, 80A	L_DD3, L_DD5 L_DD6, L_DD8, L_DD11, L_DD13 L_DD14	I/O	LCD data <i>alternative: GPIO61, GPIO63, GPIO64, GPIO66, GPIO69, GPIO71, GPIO72</i>
<b>Pin Row X3B</b>			
1B	STBY	I	STBY = 1 /SDRAM buffered by VBAT
2B	SYS_ENA	O	System power switch signal
3B	GPIO_1	I/O	Processor I/O port, <i>alternative: interrupt</i>
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND	-	Ground 0 V
5B	/CS_1x		If J19 = 2+3 then /CS signal for second on-board 16-bit Flash, <i>alternative: GPIO15</i>

Pin Number	Signal	I/O	Comments
<b>Pin Row X3B</b>			
6B	/CS_5	I/O	Chip Select signal of the processor, can be used to access the LAN controller, <i>alternative: GPIO33</i>
7B	/OE	O	Output enable signal of the processor
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B 36B	A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22, A25	I/O	Address lines
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D0, D3, D5, D6, D8, D11, D13, D14, D16, D17, D21, D23, D24, D26, D29, D31	I/O	Data lines
33B, 35B	DQM_0, DQM_3	O	Byte enable signals
47B	/CS_0	O	Chip Select for on-board Flash
48B	/CS_1	I/O	If J19 = 2+3 then /CS signal for second on-board 16-bit Flash, <i>alternative: GPIO15</i>
50B	/SDCS_0	O	/CS SDRAM bank #0
51B	/SDCS_1	O	/CS SDRAM bank #1
52B	/SDCS_2,	IO	/CS SDRAM bank #2 <i>alternative: GPIO20</i>
53B	/SDCS_3	IO	/CS SDRAM bank #3 <i>alternative: GPIO21</i>
55B	/SDCLK_2	O	Clock signal for synchronous memory
56B	/SDRAS	O	/SDRAS control signal for SDRAM
57B	/SDCAS	O	/SDCAS control signal for SDRAM
58B	/PSKSEL	I/O	Card0/1 select <i>alternative: GPIO 79</i>
60B	/PWE	I/O	PCMCIA memory write signal and I/O write signal <i>alternative: GPIO 49</i>
61B	/POE	I/O	PCMCIA memory read signal <i>alternative: GPIO 48</i>
62B	/PIOR	I/O	PCMCIA I/O read signal <i>alternative: GPIO 50</i>
63B	/PIOW	I/O	PCMCIA I/O write signal <i>alternative: GPIO 51</i>
65B	/LAN_IRQ	I/O	Interrupt LAN controller
66B	L_CS	O	LCD CS <i>alternative: GPIO 19</i>
67B	L_DD16	O	LCD data <i>alternative: GPIO 86</i>
68B	L_DD17	O	LCD data <i>alternative: GPIO 87</i>

Pin Number	Signal	I/O	Comments
<b>Pin Row X3B</b>			
70B, 71B, 72B, 73B, 75B, 76B 77B, 78B 80B	L_DD0, L_DD1, L_DD2, L_DD4, L_DD7, L_DD9, L_DD10, L_DD12, L_DD15	I/O	LCD data bus <i>alternative: GPIO 58, GPIO 59, GPIO 60, GPIO 65, GPIO 67, GPIO 68, GPIO 70, GPIO 73</i>
<b>Pin Row X3C</b>			
1C, 2C	+3V3	P	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C 72C, 77C	GND	P	Ground 0 V
4C	VMMC	P	Optional supply voltage for internal MMC card
5C	VBAT	P	Input for external battery
6C	VCC_LCD	P	VCC for LCD Port
8C	USB_H_PWR	P	Over-current indicator from ports 3, 2 and 1
9C	USIM_VCC	P	VCC (3.0 V or 1.8 V) USIM
10C	/RESIN	I/O	/Reset input for reset controller at U9
11C	/RESET_OUT	I/O	/Reset output of the PXA270 processor
13C	NSSP_TxD	I/O	Network SPI TxD signal, used for CAN Controller <i>Alternative: GPIO 81</i>
14C	NSSP_CLK	I/O	Network SPI Clock signal <i>Alternative: GPIO 84</i>
15C	NSSP_RxD	I/O	Network SPI RxD signal <i>Alternative: GPIO 82</i>
16C	NSSP_FRM	I/O	Network SPI Frame signal, used for CAN Controller <i>alternative: GPIO 83</i>
18C	IR_TXD	O	IrDA TxD <i>Alternative: GPIO 47</i>
19C	IR_RXD	I	IrDA RxD <i>Alternative: GPIO 46</i>
20C	FF_RI_DETECT	O	RI-Detect FF-UART (for interrupt)
21C	FF_/INVALID	O	Invalid level FF_UART
23C	/ACRESET	O	/RESET AC97 <i>Alternative: GPIO 113</i>
24C	SYNC	I/O	SYNC AC97 <i>Alternative: GPIO 31</i>

Pin Number	Signal	I/O	Comments
<b>Pin Row X3C</b>			
25C	BITCLK	I/O	BITCLK <i>Alternative: GPIO 28</i>
26C	nc		No connect
28C	SDATA_IN_0	I/O	SDATA_IN0 (AC97 interface) <i>Alternative: GPIO 29</i>
29C	SDATA_OUT	I/O	SDATAOUT <i>Alternative: GPIO 30</i>
30C	SDA	I/O	I <sup>2</sup> C data from processor <i>Alternative: GPIO 118</i>
31C	SCL	I	I <sup>2</sup> C clock from processor <i>Alternative: GPIO 117</i>
33C	/LAN_LED_A-	O	LED A LAN controller, freely configurable
34C	/LAN_LED_B	O	LED B LAN-Controller, freely configurable
35C	LAN_TPI-	O	LAN negativer input
36C	LAN_TPO-	O	LAN negativer output
38C	OTG_ID	I	OTD ID Input USB Controller
39C	PWM0	O	PWM output #0 <i>Alternative: GPIO 16</i>
40C	PWM1	O	PWM output #1 <i>Alternative: GPIO 17</i>
41C	/TRST	O	JTAG reset
43C	USIM_IO	IO	USIM I/O Data. Receive and transmit data connection
44C	nc		No connect
45C	MMC_DAT2_CS0	O	MMC_C0 for external MMC card <i>Alternative: GPIO 110</i>
46C	MMC_DAT3_CS1	O	MMC_C1 for internal MMC card <i>Alternative: GPIO 111</i>
48C, 49C, 50C, 51C, 53C	GPIO114, GPIO9 GPIO10, GPIO12, GPIO90	I/O	GPIOs <i>Alternative: interrupt signals</i>

Pin Number	Signal	I/O	Comments
<b>Pin Row X3C</b>			
54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C	EGPIO0, EGPIO1, EGPIO3, EGPIO6, EGPIO8, EGPIO9, EGPIO11, EGPIO14, EGPIO16, EGPIO17, EGPIO18, EGPIO22, EGPIO24, EGPIO25, EGPIO27	I/O	Additional GPIOs generated by the MAX7301 / MAX6957 IC
73C	SSP_RXD	I	SPI RxD signal <i>Alternative: GPIO 26</i>
74C	SSP_TXD	O	SPI TxD signal <i>Alternative: GPIO 25</i>
75C	/CS_EGPIO	I	SSP /CS1 signal for MAX7301 / MAX6957 ( EGPIO )
76C	/CAN_CS	I	/CS signal for SJA1000 ( CAN )
78C	/CAN_INT	O	CAN Interrupt
79C	CANRXD	I/O	CAN RxD signal
80C	CANTXD	I/O	CAN TxD signal
<b>Pin Row X3D</b>			
1D, 2D	VCC	P	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	-	Ground 0 V
4D, 5D	VCC1	P	Optional external supply voltage V <sub>CORE</sub> for processor, 3-5.0 V
6D	VCC_BB	P	VCC Baseband
7D	USB_H_ENA	O	USB Controller Power Switch signal
8D	SYS_ENAB	O	System Power Switch signal
10D	/RESET	O	Reset output from reset controller
11D	/BATT_FAULT	I	Low battery voltage indication
12D	/VCC_FAULT	I	Low supply voltage indication
13D	PWR_ENAB	O	PXA-Core Power Signal
15D	BT_CTS	I	CTS Bluetooth UART <i>Alternative: GPIO 44</i>
16D	BT_RXD	I	RXD Bluetooth UART <i>Alternative: GPIO 42</i>

Pin Number	Signal	I/O	Comments
<b>Pin Row X3D</b>			
17D	BT_TXD	O	TXD Bluetooth UART <i>Alternative: GPIO 43</i>
18D	BT_RTS	O	RTS Bluetooth UART <i>Alternative: GPIO 45</i>
20D	FF_/SHDN	I	FF-UART power on
21D	FL_WP_PEN	I	Flash Write Protect
22D	RS_RXD	I	FF-UART RxD signal (RS-232)
23D	RS_TXD	O	FF-UART TxD signal (RS-232)
25D	RS_RTS	I	FF-UART RTS signal (RS-232)
26D	RS_CTS	I	FF-UART CTS signal (RS-232)
27D	RS_DSR	I	FF-UART DSR signal (RS-232)
28D	RS_DTR	O	FF-UART DTR signal (RS-232)
30D	RS_RI	I	FF-UART RI signal (RS-232)
31D	RS_DCD	I	FF-UART DCD signal (RS-232)
32D	USB_C_P	I/O	USB Client positive, from processor
33D	USB_C_N	I/O	USB Client negative, from processor
35D	LAN_TPI+	O	LAN input positive
36D	LAN_TPO+	O	LAN output positive
37D	USB_H_P	I/O	USB Host Controller positive, from processor
38D	USB_H_N	I/O	USB Host Controller negative, from processor
40D	TDI	I	JTAG TDI signal
41D	TDO	O	JTAG TDO signal
42D	TMS	I	JTAG TMS signal
43D	TCK	I	JTAG TCK signal
45D	MMC_CLK	I/O	MMC_CLK signal
46D	MMC_DAT0	I/O	MMC_DAT signal
47D	MMC_CMD	I/O	MMC_CMD signal
48D	MMC_DAT1	I/O	MMC_DAT1 signal
50D, 51D, 52D, 53D	GPIO11, GPIO13, GPIO52, GPIO91,	I/O	GPIOs, <i>alternative: interrupt signals</i>
55D, 56D, 57D, 58D, 60D, 61D, 62D, 63D, 65D, 66D, 67D, 68D, 70D	EGPIO2, EGPIO4, EGPIO5, EGPIO7 EGPIO10, EGPIO12, EGPIO13, EGPIO15, EGPIO19, EGPIO20, EGPIO21, EGPIO23, EGPIO26	I/O	Additional GPIOs generated by the MAX7301 / MAX6957 IC with 7 interrupt- capable inputs for connection to a matrix keyboard



Pin Number	Signal	I/O	Comments
<b>Pin Row X1D</b>			
71D	SSP_EXTCLK	I	SPI external clock <i>alternative: GPIO 27</i>
72D	SSP_CLK	O	SPI clock signal <i>alternative: GPIO 23</i>
73D	SSP_SFRM	I/O	SPI frame signal <i>alternative: GPIO 24</i>
75D	FL_DIS	I	Signal to disable internal Flash
76D	SSP_SYSCLK	I/O	SYSCLOCK SSP <i>Alternative: GPIO 53</i>
77D	PWR_SDA	I/O	Power I2C Serial Data/Address signal <i>Alternative: GPIO 4</i>
78D	PWR_SCL	O	Power I2C Serial Clock Line signal <i>Alternative: GPIO 3</i>
80D	/INT_RTC	O	Interrupt output RTC

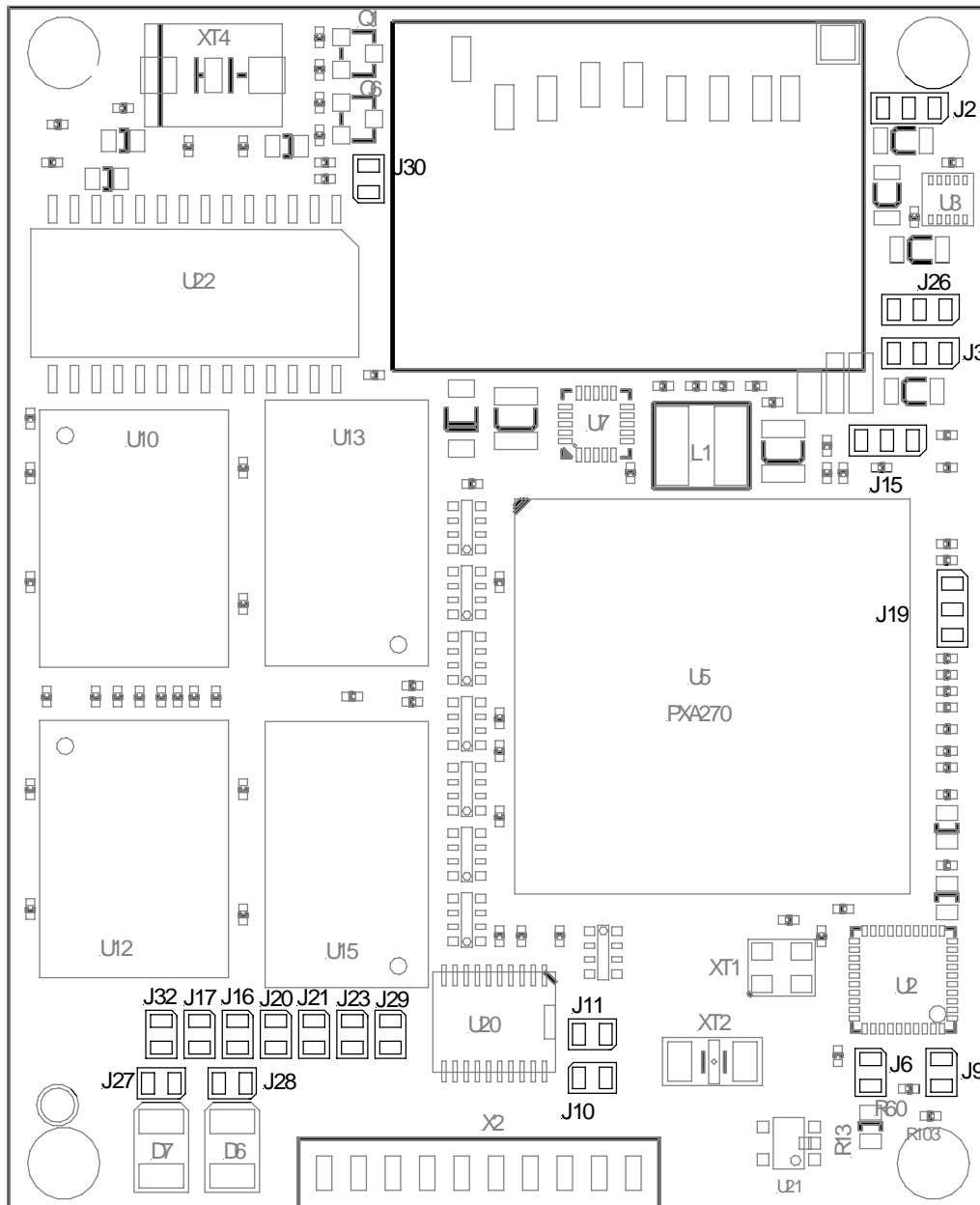
Table 1: Pinout of the phyCORE-connector X1

The section "Initializing the phyCORE-PXA270" shows all GPIO signals and their default settings.



### 3 Jumper

For configuration purposes, the phyCORE-PXA270 has 32 solder jumpers, some of which have been installed prior to delivery. *Figure 6* illustrates the numbering of the jumper pads, while *Figure 4* and *Figure 5* indicate the location of the jumpers on the board.



*Figure 4: Location of the Jumpers (Controller Side)*

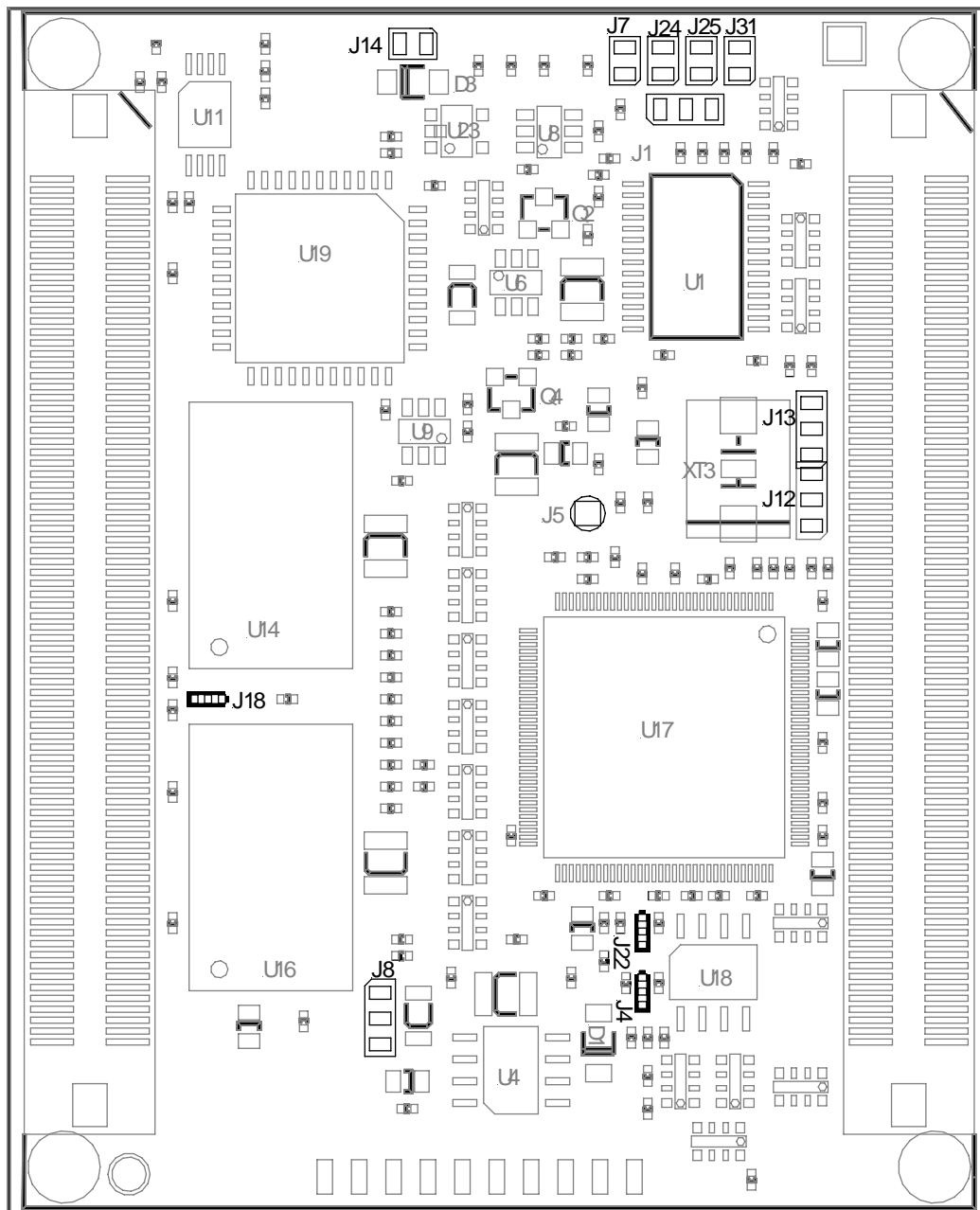


Figure 5: Location of the Jumpers (Connector Side)



Figure 6: Numbering of the Jumper Pads

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
<b>J1</b>		This jumper configures the supply voltage for the on-board MM card.
1 + 2 2 + 3	X	MM card supplied via VCC. MM card supplied externally via VMMC.
Package Type		0R in SMD 0805
<b>J2</b>		This jumper configures the supply input voltage for the voltage regulator generating the VCORE voltage.
1 + 2 2 + 3	X	Voltage regulator supplied by VCC. Voltage regulator supplied by external VCC1.
Package Type		0R in SMD 0805
<b>J3</b>		This jumper configures the supply input voltage for the LCD port.
1 + 2 2 + 3	X	LCD port supplied via VCC. LCD port supplied externally via VCC_LCD.
Package Type		0R in SMD 0805
<b>J4</b>		This jumper configures the organization for the SPI EEPROM connected to the Ethernet controller.
1 + 2 2 + 3	X	Using an SPI EEPROM from another manufacturer. Using an Atmel AT93C46 SPI EEPROM.
Package Type		0R in SMD 0805
<b>J5</b>		Vcore test jumper J1X1
Package Type		Pin only
<b>J6</b>		This jumper configures the SPI /CS signal for the MAX7301 / MAX6957 GPIO expander controller.
closed open	X	/CS signal for MAX7301 / MAX6957 connected to SSP_SFRM (GPIO24). External /CS signal used for MAX7301 / MAX6957, connected via phyCORE-connector.
Package Type		0R in SMD 0805
<b>J7</b>		This jumper configures the MCC_WP signal
closed open	X	MCC_WP signal for MM card connected to GPIO10. MCC_WP signal for MM card is open
Package Type		0R in SMD 0805

Jumper	Default	Comment
<b>J8</b>		This jumper configures the supply input voltage for the Baseband port.
1 + 2 2 + 3	X	Baseband port supplied via VCC. Baseband port supplied externally via VCC_BB.
Package Type		0R in SMD 0805
<b>J9</b>		This jumper configures the interrupt signal for the MAX7301 / MAX6957 GPIO expander controller.
closed open	X	Interrupt signal for MAX7301 / MAX6957 connected to GPIO27. External interrupt signal used for MAX7301 / MAX6957, connected via phyCORE-connector.
Package Type		0R in SMD 0805
<b>J10/J11</b>		These jumpers connect the I <sup>2</sup> C bus with the 24C08 I <sup>2</sup> C EEPROM at U4.
closed open	X	On-board SDA and SCL signals connected to I <sup>2</sup> C EEPROM. External SDA and SCL signals used for I <sup>2</sup> C EEPROM, connected via phyCORE-connector.
Package Type		0R in SMD 0805
<b>J12</b>		This jumper configures the supply voltage for the USIM CARD.
closed open	X	USIM card supplied via VCC. USIM card supplied externally via on-board regulator
Package Type		0R in SMD 0805
<b>J13</b>		This jumper configures the CLK_REQ input
1 + 2 3 + 3	X	Internal clock source (13.000 MHz) External clock source (13.000 MHz)
Package Type		0R in SMD 0805
<b>J14</b>		This jumper configures the standby supply voltage for the SDRAM.
opened closed	X	SDRAM standby supply via VBAT. No SDRAM standby supply.
Package Type		0R in SMD 0805

Jumper	Default	Comment
<b>J15</b>		This jumper selects the bus interface for the on-board boot Flash.
1 + 2	X	32-bit boot Flash
2 + 3		16-bit boot Flash
Package Type		100k in SMD 0805
<b>J16</b>		This jumper configures the /CS signal for the LAN91C111 Ethernet controller at U17.
closed	X	/CS signal for LAN91C111 connected to /CS5 of the PXA270 processor.
open		External /CS signal used for LAN91C111, connected via phyCORE-connector.
Package Type		0R in SMD 0805
<b>J17</b>		This jumper configures the Ready signal for the LAN91C111 Ethernet controller at U17.
closed	X	LAN_RDY signal from LAN91C111 connected to RDY input of the PXA270 processor.
open		LAN_RDY signal from LAN91C111 can be connected externally, available on phyCORE-connector (X3A66).
Package Type		0R in SMD 0805
<b>J18</b>		Flash WP or PEN on FL_WP_PEN.
1 + 2	X	FL_WP_PEN is /PEN.
2 + 3		FL_WP_PEN is /WP.
open		
Package Type		0R in SMD 0805
<b>J19</b>		/CS1 configuration
1 + 2	X	/CS1 is routed to phyCORE-connector pin X3B5.
2 + 3		/CS1 is routed to phyCORE-connector pin X3B48.
Package Type		0R in SMD 0805
<b>J20</b>		This jumper configures the Ethernet interrupt.
closed	X	Ethernet interrupt is connected to GPIO_52
open		Ethernet interrupt is connected to an external signal (labeled LAN_IRQ, pin X3B65).
Package Type		0R in SMD 0805

Jumper	Default	Comment
<b>J21</b>		This jumper enables the Ethernet EEPROM.
closed		Ethernet EEPROM is disabled.
open	X	Ethernet EEPROM is enabled.
Package Type		0R in SMD 0805
<b>J22</b>		Ethernet /WE signal configuration.
1 + 2	X	Ethernet /WE is connected to /PWE (VLIO interface) on the PXA270.
2 + 3		Ethernet /WE is connected to /WE (SRAM/ROM interface) on the PXA270.
Package Type		0R in SMD 0402
<b>J23</b>		This jumper connects the /CAN_INT signal to GPIO114.
closed	X	/CAN_INT is connected to GPIO114.
open		/CAN_INT needs to be connected externally (X3C78).
Package Type		0R in SMD 0805
<b>J24</b>		This jumper configures the MCC_DAT2_CS0 signal.
closed		MMC_DAT2_CS0 is connected to the MMC card connector.
open	X	MMC_DAT2_CS0 is open.
Package Type		0R in SMD 0805
<b>J25</b>		This jumper configures the MMC_DAT1 signal.
closed		MMC_DAT1 is connected to the MMC card connector.
open	X	MMC_DAT1 is open.
Package Type		0R in SMD 0805
<b>J26</b>		RS-232 transceiver FORCEON input configuration.
1 + 2		RS-232 FORCEON is connected to GND ( <i>see MAX3245EAI RS-232 transceiver data sheet for details</i> ).
2 + 3	X	RS-232 FORCEON is connected to the FF_/INVALID signal.
Package Type		0R in SMD 0805



Jumper	Default	Comment
<b>J27 / J28</b>		LED configuration, red LED D6 connected to GPIO90 (J28), green LED D7 to GPIO91 (J27).
closed	X	LED D6 (red) is connected to GPIO90, D7 (green) to GPIO91.
open		LEDs not used.
Package Type		1kOhm in SMD 0805
<b>J29</b>		RTC interrupt configuration.
closed	X	RTC interrupt is connected to GPIO_0.
open		RTC interrupt needs to be connected externally (X3D80).
Package Type		0R in SMD 0805
<b>J30</b>		This jumper configures the Flash reset.
closed	X	Flash reset connected with RESET_OUT.
open		No Flash reset.
Package Type		0R in SMD 0805
<b>J31</b>		This jumper configures the MMC_DETECT signal.
closed	X	MMC_DETECT signal for MMC card connected to GPIO_9.
open		MMC_DETECT signal for MMC card not connected.
Package Type		0R in SMD 0805
<b>J32</b>		This jumper configures the Ethernet EEPROM bank.
closed	X	EEPROM bank 0 full configuration.
open		EEPROM bank 7 configuration MAC only.
Package Type		0R in SMD 0805

Table 2: Jumper Settings



## 4 Power System and Reset Behavior

The phyCORE-PXA270 is only supplied with a single supply voltage. However it is possible to power the MMC card, LCD port, Baseband port and the internal voltage regulator of the Vcore voltage externally.

Supply voltage 1: +3.3 V (VCC)  
Supply voltage 1: +3.0 V (VBAT)  
Supply voltage 3: +3.3 V (VCC1) optional  
Supply voltage 4: +3.3 V (VMMC) optional  
Supply voltage 5: +3.3 V (VCC\_LCD) optional  
Supply voltage 6: +3.3 V (VCC\_BB) optional  
Supply voltage 6: +3.3 V (VCC\_USIM) optional

### **Caution!**

The VMMC, VCC\_LCD and VCC\_BB voltage must not be connected without VCC being supplied at the same time.

### **Power-On Behavior**

During standard operating mode all components of the module are supplied by a common 3.3 V (VCC) supply voltage. The chronological order for turning on the individual voltages as well as the reset signal is defined on the module. The SDRAM content is undefined after power-on, which is why the system will always reboot and initialize the memory.

The voltage VMMC, VCC\_LCD, VCC\_USIM and VCC\_BB (if configured as an option) can be switched on or off while VCC is present.

### **Power-Off Behavior**

In the standard operating mode, all components including the SDRAM, are supplied by a common 3.3 V (VCC) supply voltage. If the VCC is turned off, the SDRAM can be supplied via VBAT and operated in self-refresh mode to maintain its data. *See the following Deep-Sleep mode paragraph for more details.*

## Deep-Sleep Mode

The phyCORE-PXA270 supports the controller's Deep-Sleep mode. In this mode the SDRAM runs in self-refresh mode and is supplied by the VBAT power. Hence, all other supply voltages can be turned off. The PXA270 controller provides a special SYS-ENA signal for the purpose of turning supply voltages on or off:

- SYS\_ENA = "1" turns supply voltages on
- SYS\_ENA = "0" turns supply voltages off

The SDRAM supply circuitry implemented on the phyCORE-PXA270 requires that the VBAT voltage is lower than the VCC supply voltage. PHYTEC recommends a regulated VBAT voltage in the range of 3.0 V to 3.1 V. The lowest supply voltage required to maintain the DRAM self-refresh is 2.7 V.

The phyCORE-PXA270 has a current draw of < 5 mA when operated in Deep-Sleep mode. It is possible to disable the VCC to VBAT supply switching for the SDRAM with the help of Jumper J14. If VBAT for SDRAM is disabled then only the RTCs and some controller functions are supplied.

## RESET Configuration

A system reset is released with the help of reset controller U9 using the /RESIN signal or a drop of the VCC supply voltage. Reset of the PXA270 core is generated via U6. The /RESIN signal or a drop of the VBAT voltage will release a core reset. If a core reset based on a VCC supply voltage drop is desired then the signal /RESIN must be activated by an external reset controller.

The JTAG reset is released with the help of reset controller U8 using /TRST or a drop of the VCC supply voltage.

## Power Management

Various power management functions are implemented on the phyCORE-PXA270 module. The controller can switch the Vcore voltage regulator on or off independently. Furthermore the controller offers a number of power saving possibilities. *For more on the power saving features refer to the PXA270 data sheets.*

## 5 VCore Supply Voltage

The PXA270 processor requires a core voltage of 1.3 V. This voltage can be configured in a range between 0.9 V and 1.55 V in 0.05 V increments depending on the power management mode. The voltage regulator for the Vcore, VCC\_SRAM and VCC\_PLL is located on the phyCORE-PXA270 at U7. The Vcore regulator has over 90 % efficiency. The controller can turn the switching regulator on or off using the PWR\_EN output. The regulator can be supplied with the module's VCC or by an external voltage via solder jumper J2. The external voltage regulator supply option should only be used during battery operation. The Vcore input voltage can then be generated directly from the battery voltage.

<b>J2</b>	<b>Description</b>
1 + 2	Input voltage for Vcore voltage regulator supplied by the on-board +3.3 V (VCC) operating voltage.
2 + 3	Input voltage for Vcore voltage regulator supplied by an external source ranging from +3.3 V to +5 V.

*Table 3: Jumper J2 for Vcore Supply Voltage*

The default value of the Vcore voltage following a hardware reset is 1.3 V. The regulator can be configured via the processor's PWR\_I<sup>2</sup>C bus.



## 6 System Memory

The controller PXA270 provides a configurable memory interface for:

- 4 \* SDRAM with max. 256 MByte each
- 3 (4) \* asynchronous or synchronous ROM/Flash/RAM/IO with max. 64 MByte each
- 2 \* asynchronous ROM/Flash/RAM/IO with max. 64 MByte each

The internal MMU and the configurable memory interface of the PXA270 processor enable it to adapt the memory model during runtime with the help of software. The configuration of the Boot-ROM can be set on the phyCORE module using solder jumper J15 (refer to section 3).

### 6.1 Memory Model Following Reset

The memory model following a hardware reset only activates the controller's /CS0 signal. Access using this /CS signal is configured with the BOOT\_SELx connection. Closing Jumper J15 connects the corresponding boot select signal BOOT\_SEL to GND potential resulting in a low level being read by the PXA270 processor.

J15	Description
1 + 2	32-bit asynchronous Boot ROM
2 + 3	16-bit asynchronous Boot ROM

Table 4: Boot Configuration via BOOT\_SEL Pin

After reset the memory range of /CS0 is pre-initialized to 64 MByte. Therefore all configuration options from 16 MByte to 64 MByte can be addressed with 2\*16-bit Flash devices connected to /CS0. By default the access occurs with 32-bit data bus width in asynchronous mode. The Flash contains a boot loader starting at address 0x00000000 which performs all necessary initialization steps for the PXA270 processor.

## 6.2 Runtime Memory Model with the U-Boot Loader

The runtime memory model is selected via software by configuring the internal registers of the PXA270 processor. The U-Boot loader, which belongs to the standard delivery package, configures the following memory model:

/CS0	2 * 16-bit Flash memory 16 to 64 MByte asynchronous or synchronous (optional 16-bit Flash memory 8 MByte async.)
/CS1	free (pre-configured for 16-bit asynchronous ROM/RAM)
/CS2	free (pre-configured for 16-bit VLIO interface)
/CS3	not used (PSKSEL PCMCIA)
/CS4	free (pre-configured for 16-bit VLIO interface)
/CS5	free or Ethernet chip with 32-bit VLIO interface
/SDCS0	64 MByte 2*16-bit SDRAM
/SDCS1	optional 64 MByte 2*16-bit SDRAM
/SDCS2	free (optional 256-MB Configuration)
/SDCS3	free (optional 256-MB Configuration)

The configuration can be adapted to user requirements during runtime with the exception of the SDRAM registers. The following table shows the default values for the /CS0... /CS5 signals of the PXA270 controller.

PXA270 Register	Default Value
MSC0	0x12CB 12B3
MSC1	0x128C 128C
MSC2	0x1234 128C

Table 5: /CS0..5 Init Values



### 6.3 SDRAM Memory (U13/U15)

The phyCORE-PXA270 is populated with a 64 MByte, 32-bit data width SDRAM memory. This memory bank is created by using two SDRAM devices with 32 MByte each and 16-bit data bus at U13 and U15. This bank is also referred to as SDRAM bank 0. The total SDRAM memory can be expanded to 128 MByte by populating the second bank (bank 1) at U14 and U16 with additional memory devices. The configuration of bank 1 corresponds to the configuration of bank 0.

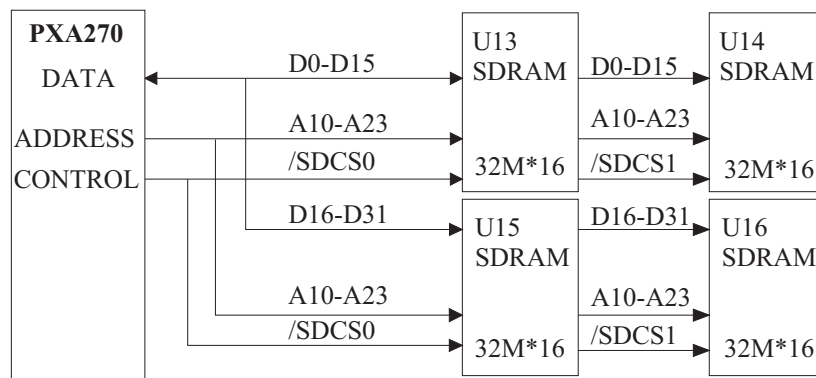


Figure 7: SDRAM 32-128 MB Connection to PXA270

Upon special request the phyCORE-PXA270 can also be populated with 256 MByte SDRAM. In this configuration 64M\*16 SDRAM memory chips populate U13-U16, with 2 Chip Selects controlling each SDRAM device.

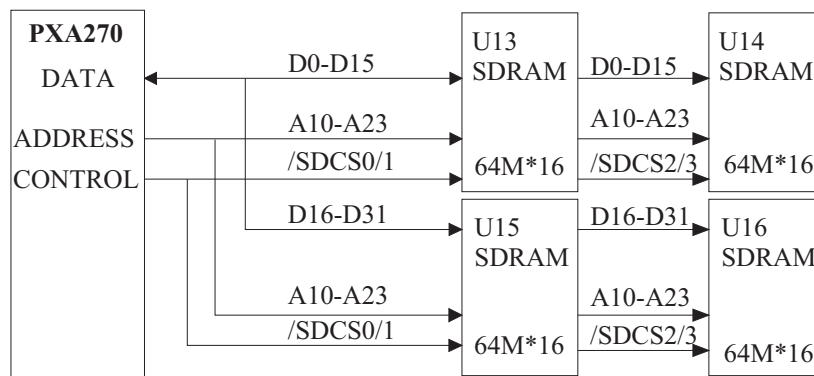


Figure 8: SDRAM 128-256 MB Connection to PXA270

<b>SDRAM</b>	<b>Configuration (also refer to the PXA270 controller documentation)</b>														
Range	16 M*32-bit (2 * 16-bit SDRAM each)														
Bus Width	32-bit														
Address Mode	SA1111 Address Mode														
Address Scheme	2*13*10*16														
Assignment	A2	A2	A2	A2	A2	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1
	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
	A1	B1	B0	A1	A1	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	2			1	0										
Clock Rate	100 MHz														

Table 6: SDRAM Configuration

SDRAM initialization is performed by a boot loader or the operating system following a power-on reset and must not be changed at a later point by any application code. The following table shows the initialization values for bank 0/1 as an example.

<b>PXA270 Register</b>	<b>Initialization Values</b>
MDCNFG	0xAC80AC9
MDREFR	0x2213E018
MDMRS LP	0x0000 0000
MDMRS	0x0032 0032

Table 7: SDRAM Init values

The physical memory areas of SDRAM bank 0 to bank 3 are shown in the following table. Using the PXA270's internal MMU it is possible to assign different virtual addresses to these banks at any time.

<b>SDRAM Bank</b>	<b>Start Address</b>
Bank 0	0xA000 0000
Bank 1	0xA400 0000
Bank 2	0xA800 0000
Bank 3	0xAA00 0000

Table 8: SDRAM Address Ranges

## 6.4 Flash Memory (U10/U12)

Use of Flash as non-volatile memory on the phyCORE-PXA270 provides an easily reprogrammable means of code storage. Intel Strata Flash is used as the Flash device for the phyCORE-PXA270. The Flash devices operate in 16-bit mode. Two individual Flash chips are connected to the 32-bit data bus on the module. The device at U10 is connected to the low data bus (D0-D15) and the device at U12 is connected to the high data bus (D16-D31).

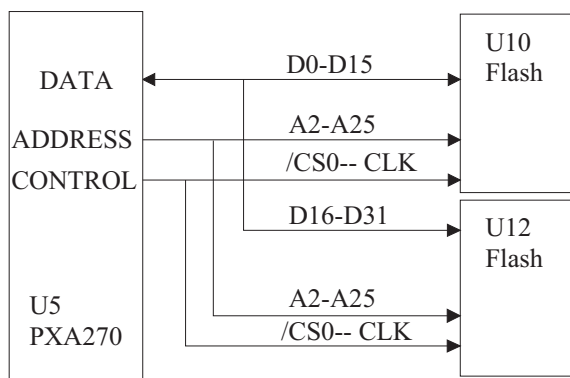


Figure 9: Flash Connection to PXA270

The Flash devices can operate in asynchronous as well as synchronous mode. Currently the asynchronous mode is used on the phyCORE-PXA270.

Flash	Configuration
Range	8M* 32-bit (2* 16-bit 28F128J3D Intel Strata Flash each)
Access	32-bit
Clock Rate	Asynchronous

Table 9: Flash Configuration

The physical memory area of the Flash bank is shown in the following table. Using the internal MMU of the PXA270 it is possible to assign different virtual addresses to this Flash bank at any time.

Flash	Start Address
Bank 0	0x0000 0000

Table 10: Flash Address Ranges

Use of Flash memory enables in-circuit programming of the module. The Flash devices on the phyCORE-PXA270 are programmable at 3.3 VDC. Consequently, no dedicated programming voltage is required. As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase block cycles.

## 6.5 External Address and Data Bus

The address and data bus of the PXA270 is accessible on the Molex connector at X3. The address/data bus operates on the module with a clock speed of 100 MHz. It is therefore absolutely necessary to decouple the address/data bus when using it for external circuitry. The decoupling circuits should be located as close to phyCORE-connector at X3A/B as possible. The optimal signal trace length is less than 40 mm!

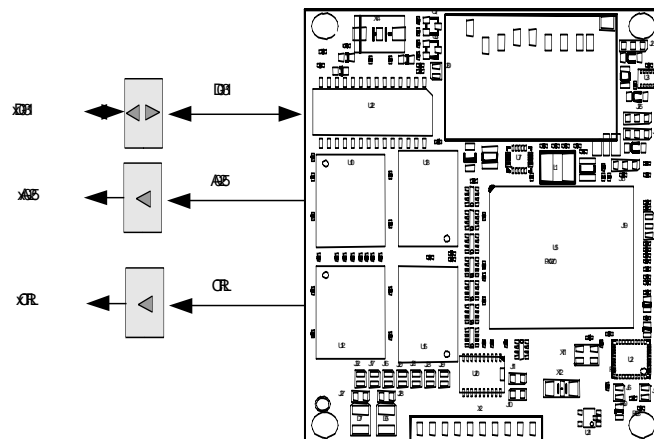


Figure 10: Decoupling the Address/Data Bus for External Connections

## 7 Ethernet Controller (U17)

Connection of the phyCORE-PXA270 to the world wide web (WWW) or a local area network (LAN) is possible with the on-board SMSC LAN91C111 10/100 Mbps Ethernet controller populating the module at U17. This Ethernet controller features an integrated PHY layer. Thus the external components required to connect the phyCORE-PXA270 to a LAN are limited to the transformer, the RJ45 socket and a few discrete components. Support for this Ethernet chip is available by a wide range of operating systems, such as Linux, WinCE and QNX.

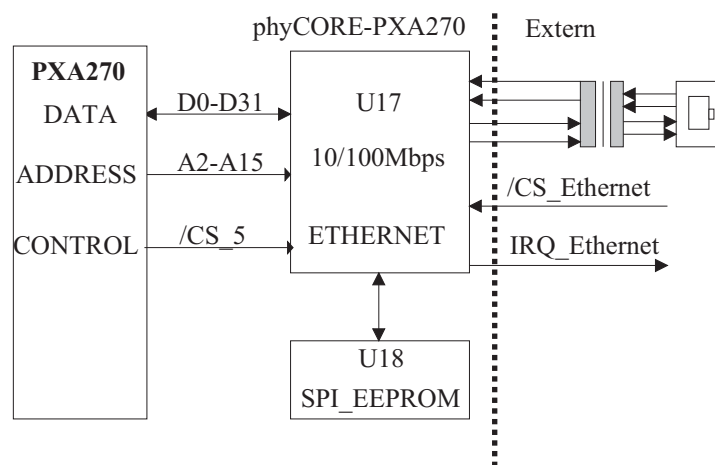


Figure 11: Ethernet Connection to PXA270

The Ethernet controller is connected to the data bus with a 32-bit width and can be configured via Jumpers J16, J17, J20, J22 and J32. Jumper J15 is used to connect the interrupt signal of the LAN91C111 with a corresponding input on the PXA270 processor or to external logic. The interrupt is being used as active high edge triggered.

J20	Description
closed	LAN91C111 interrupt signal connected to GPIO52 on the PXA270 processor.
open	External interrupt signal used for LAN91C111, connected via phyCORE-connector.

Table 11: Ethernet Controller Interrupt Signal Connection

The /CS signal for the LAN91C111 Ethernet controller at U17 can be connected to the PXA270 processor's /CS5 signal using Jumper J16. The Ethernet controller's offset of 0x300 has to be noted when accessing the chip.

<b>J16</b>	<b>Description</b>
closed	/CS signal for LAN91C111 connected to /CS5 of the PXA270 processor.
open	External /CS signal used for LAN91C111, connected via phyCORE-connector.

Table 12: Ethernet Controller /CS Signal Connection

The Ethernet controller provides a READY output that can be connected to the /RDY input of the controller using Jumper J17. It is also possible to combine various signal sources externally if multiple components need to use the processor's RDY input.

<b>J17</b>	<b>Description</b>
closed	LAN_RDY (ARDY) signal from LAN91C111 connected to RDY input of the PXA270 processor.
open	LAN_RDY (ARDY) signal from LAN91C111 not used or connected externally, available on phyCORE-connector (X3A66).

Table 13: Ethernet Controller READY Output Connection

The VLIO interface on the PXA270 is used as the memory interface for the Ethernet controller. For this reason the /WE signal from the Ethernet controller is connected to the /PWE signal on the PXA270.

<b>J22</b>	<b>Description</b>
1 + 2	PXA270 VLIO memory interface with /PWE
2 + 3	PXA270 SRAM/ROM memory interface with /WE

Table 14: Ethernet Controller Memory Interface Connection

The Configuration Eeprom for the Ethernet Controller has 8 Banks.

<b>J32</b>	<b>Description</b>
closed	EEPROM have full Configuration
open	EEPROM save MAC only

Table 15: Ethernet Controller Memory Interface Connection

The physical memory area for the Ethernet chip is defined in the following table (see Table 16). An offset of 0x300 has to be added to the address of /CS5 if Jumper J16 is closed. When using an external /CS signal the same procedure applies, add an offset of 0x300 to the address of the external /CS signal.

Ethernet	Start Address
/CS5 + OFFSET	0x1400 0000 + 0x0000 0300 = 0x1400 0300

Table 16: Memory Area Ethernet Controller

Connection to an external Ethernet transformer should be done using very short signal lines. The lines TPI+/TPI- and TPO+/TPO- should be routed in pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals. Furthermore, the impedance of the signal lines should be taken into consideration during the design and layout process.

### Caution!

Please note the design specifications provided by SMSC when creating the Ethernet transformer circuitry.

## 8 PCMCIA Connection

The Intel PXA270 processor supports two PCMCIA sockets. These cannot be connected directly to the address and data bus of the processor. Proper operation requires external decoupling between the address/data bus and the PCMCIA sockets. *The circuitry required for implementing one or two external PCMCIA sockets is described in the corresponding Intel application notes.*

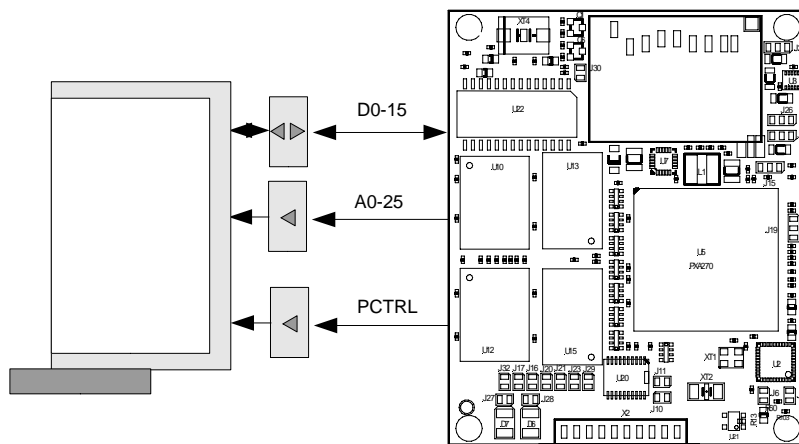


Figure 12: PCMCIA Connection to phyCORE-PXA270



## 9 CAN Controller (U22)

The Phillips SJA1000 FullCAN controller is implemented on the phyCORE-PXA270. The CAN controller is connected to the PXA270 via the PCMCIA interface socket 0 and address A25 =1. The Control PLD U19 generates the multiplexed data/address bus for the CAN controller. The 5 V power supply for the CAN controller is located on the phyCORE-PXA270.

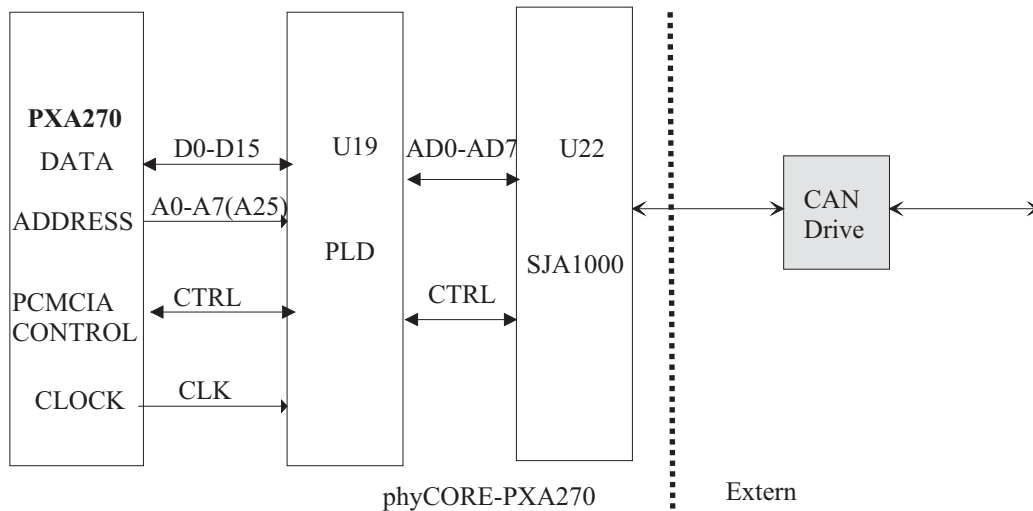


Figure 13: CAN Controller Connection

The CAN controller's interrupt output can be connected to various signals via Jumper J23.

J23	Description
closed	Interrupt signal from SJA100 connected to GPIO114 on PXA270.
open	Interrupt signal can be connected to external device.

Table 17: CAN Controller Interrupt Signal

There is no on-board CAN transceiver implemented on the phyCORE-PXA270. Thus connection to an external transceiver in the application circuitry is required when using this module in a CAN system.



## 10 phyCORE LEDs

A yellow RUN and a red BUSY LED are provided on the phyCORE-PXA270 indicating the state of the module. These LEDs can be controlled via operating system functions using pins GPIO91 (RUN) and GPIO90 (BUSY).

**Note:**

The voltage USIM (3.0 V) is required to operate the LEDs.

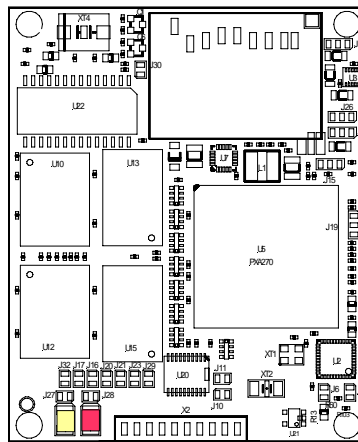


Figure 14: phyCORE-PXA270 LEDs

Jumper J27 configures the RUN LED. Closing this jumper with a 1 kOhm resistor (0805 footprint) will connect the LED to GPIO91.

J27	Description
closed with 1 kOhm	RUN LED_B connected to GPIO91 on PXA270.
open	RUN LED_B not used.

Table 18: RUN LED (Yellow) D6

Jumper J28 configures the red BUSY LED. Closing this jumper with a 1 kOhm resistor (0805 footprint) will connect the LED to GPIO90.

J28	Description
closed with 1 kOhm	BUSY LED_A connected to GPIO90 on PXA270
open	BUSY LED_A not used

Table 19: BUSY LED (Red) D7

## 11 LCD Connection

The Intel PXA270 processor supports a wide variety of passive and active LCDs. *Additional information about the LCD support feature is available in the Intel data sheets.* We recommend decoupling the LCD data and control lines from the PXA270 pins using applicable line driver circuits. The brightness of the LCD's background light can be adjusted using one of the controller's PWM signals.

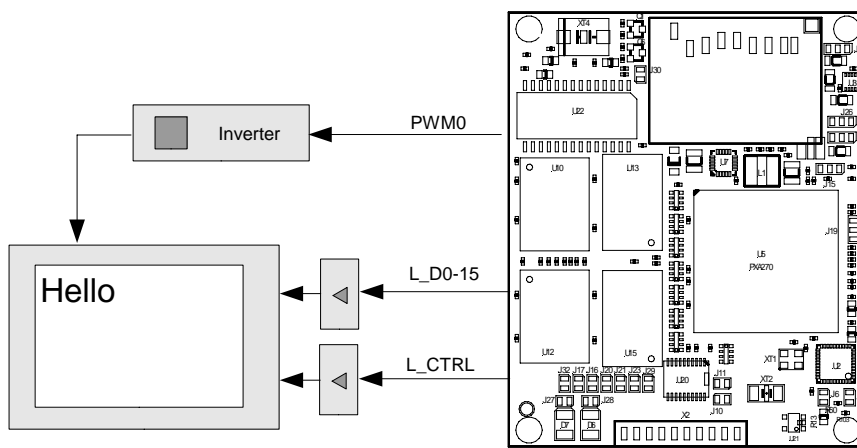


Figure 15: LCD Connection to phyCORE-PXA270

The example circuitry connection shown in the figure above refers to the control of the LCD with a fixed color depth setting. Multiplexers are required if the color depth needs to be able to vary between 16-bit and 8-bit because the RGB color information is distributed over LDD0-7 for 8-bit and LDD0-15 for 16-bit or LDD0..17 for 18-bit.

## 12 Serial Memory

### 12.1 I<sup>2</sup>C EEPROM (U4)

The phyCORE-PXA270 is populated with a non-volatile memory with a serial interface (I<sup>2</sup>C interface) to store configuration data and operational parameters that need to be saved in the event of a power loss. According to the memory configuration of the module, an E<sup>2</sup>PROM (4 to 32 kByte) or FRAM can be mounted at U4. Jumpers J10 and J11 connect the I<sup>2</sup>C bus signals SDA/SCL from the PXA270 processor with the EEPROM. These I<sup>2</sup>C bus signals are also routed to the phyCORE-connector at X3. This allows for an external connection of these signals to other I<sup>2</sup>C devices.

*A description of the I<sup>2</sup>C memory protocol of the specific memory component at U4 can be found in the respective Data Sheet.*

J10, J11	Description
closed	SDA and SCL from PXA270 connected to EEPROM at U4.
open	External SDA and SCL signal used for accessing the EEPROM.

Table 20: Jumper Configuration J10/J11 for Serial Memory at U4

The bootloader on the module uses this memory to store its configuration data. The EEPROM memory size is 4 kByte. Additional technical data is given in the following table.

Capacity	I <sup>2</sup> C Clock	Address Pins	Write cycles	Data retention	Device	Manufacturer
4 KByte	400 kHz	A2, A1, A0	1,000,000	100 years	24WC32	Any

Table 21: Technical Data for Serial Memory at U4

## 12.2 MultiMedia Card (MMC)

The phyCORE module provides a receptacle socket for a MultiMedia card. The MM cards are available in capacities of 8 MByte to 1 GByte. Using such memory cards allows for easy expansion of the on-board memory configuration of the phyCORE-PXA270 to new application requirements retroactively.

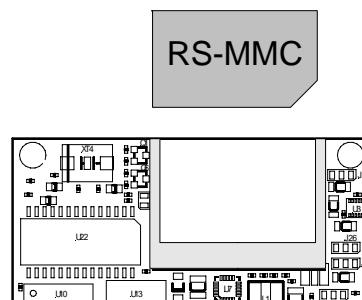


Figure 16: MMC Connector on the phyCORE-PXA270

The on-board MMC connector at X1 is controlled using the PXA270 processor's MMCS1 signal. The second interface (MMCS0 signal) is available for external use. The MMC socket signals Detect and WriteProtect are externally available and can be used as needed. Jumper J1 determines the source of the supply voltage for the MM card. The on-board 3.3 V VCC voltage is used as default. Setting Jumper J1 to position 2+3 can be useful for implementing special power saving modes, during which the external VMMC is only switched on in the event of an access to the card.

### Caution!

The VMMC voltage must not be connected without VCC being supplied at the same time.

J1	Description
1 + 2	MMC card supplied via VCC.
2 + 3	MMC card supplied externally via VMMC.

Table 22: MultiMedia Card VMMC Configuration

Detection of an inserted MMC card at X1 is possible via the MMC\_DET signal. A low level indicates that a card is in the socket. This signal is connected to GPIO\_9 on the PXA270 controller when Jumper J31 is closed with a 0 Ohm resistor.

<b>J31</b>	<b>Description</b>
closed	MMC card detect connected to GPIO9
open	MMC card detect not used

Table 23: MultiMedia Card Detect Configuration

The MMC\_WP signal indicates with a low signal level that an inserted MM card is write-protected. Jumper J7 connects this signal to GPIO\_10 on the PXA270 controller.

<b>J7</b>	<b>Description</b>
closed	MMC card write protect connected to GPIO10
open	MMC card write protect not used

Table 24: MultiMedia Card WriteProtect Configuration

Jumpers J24 and J25 can be used to configure a 4-bit data bus. This feature is not used for MMC cards.

<b>J24 / J25</b>	<b>Description</b>
closed	MMC card provides 4 data lines
open	MMC card provides 1 data line (default)

Table 25: MultiMedia Card Data Bus Configuration





## 13 Serial Interfaces

### 13.1 RS-232 Interface

The Intel PXA270 processor features four internal UARTs. Three of them are supported in the current version of the phyCORE-PXA270. The on-chip FF-UART (full function) is a UART that supports all modem signals and a maximum transfer rate of 230.4 kBaud. This interface is used on the phyCORE-PXA270 for communication with the host-PC. The RS-232 transceiver for this interface is located on the module at U1. The minimal wiring for establishing a connection between the PC and the phyCORE is shown in the figure below. Additional modem signals are available at phyCORE-connector X3.

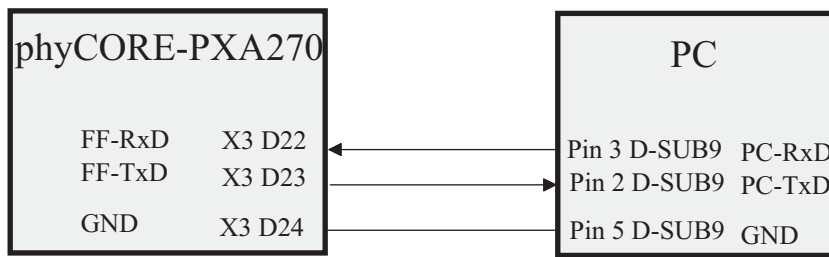


Figure 17: FF-UART Connection

The on-chip BT-UART (Bluetooth) is a high speed UART that supports baud rates up to 921.6 kBaud and can be connected to a Bluetooth module. This BT-UART only supports the signals BT\_RxD, BT\_TxD, BT\_CTC and BT\_RTS. These signals extend to the phyCORE-connector of the phyCORE-PXA270. The serial interface is intended for controlling Bluetooth send/receive modules, but it can also be used as a normal UART.

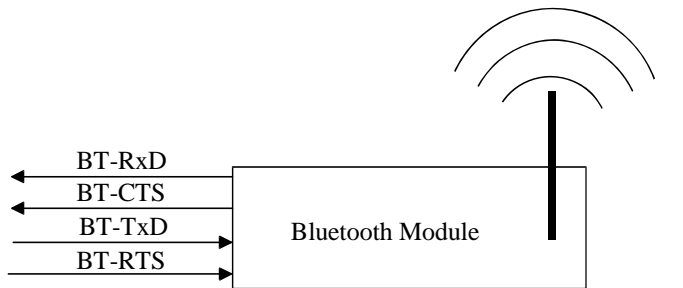


Figure 18: BT-UART Connection

The STD-UART (standard) only provides the signals STD\_RxD and STD\_TxD. No modem signals are supported. The maximum transfer rate is 230.4 kBaud. The STD-UART has a special mode for controlling IrDA transmitters.

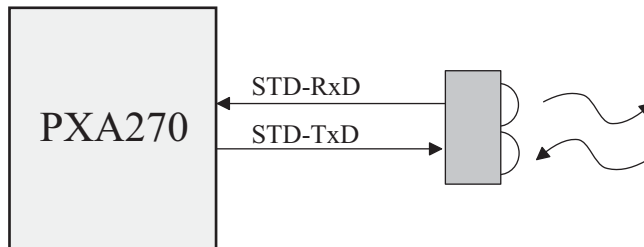


Figure 19: STD\_UART Connection

The on-chip HW-UART is a high speed UART that supports baud rates up to 921.6 kBaud. This HW-UART only supports the signals HW\_RxD, HW\_TxD, HW\_CTC and HW\_RTS.

The HW-UART interface pins are available either via the BT-UART pins or the PCMCIA general purpose I/O pins. The routing is selected by PXA270 register configuration. When using the HW-UART through the PCMCIA pins, the signal /PWE cannot be defined as HW-UART pin (HW\_RxD) because it is required for the VLIO memory interface.

## 13.2 AC97 Interface

The Intel PXA270 processor integrates an AC97 interface for controlling sound decoder chips such as the Wolfson AC97 sound controller. One of the special features of the Wolfson device is an integrated touch controller.

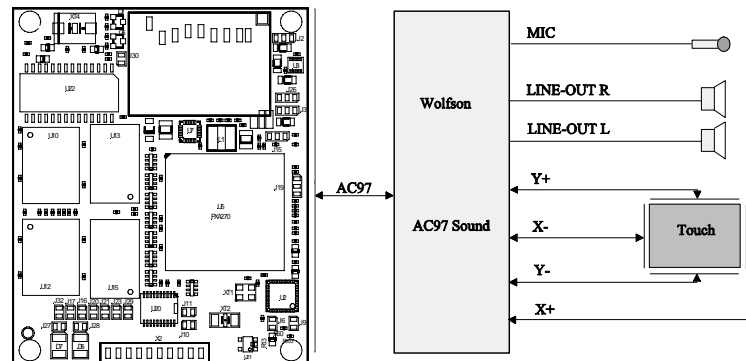


Figure 20: AC97 Interface with Wolfson

13.1.1 All signals of the AC97 interface are routed to the phyCORE-PXA270 Molex connector.

### 13.2.1 GPIO Expander (U2)

The Intel PXA270 processor features a 17-bit Matrix keyboard interface. As an alternative the phyCORE-PXA270 is populated with a MAX7301/ MAX6957 GPIO expander IC. The MAX7301/ MAX6957 has the following features:

- SPI interface
- 28 GPIO ports
- 7 interrupt-capable inputs
- One interrupt output

All GPIO signals are routed to the module's phyCORE-connector. One of the special features of the MAX7301/ MAX6957 controller is its capability to control matrix keyboards. *Refer to the MAX7301/ MAX6957 datasheet for more details on this function.*

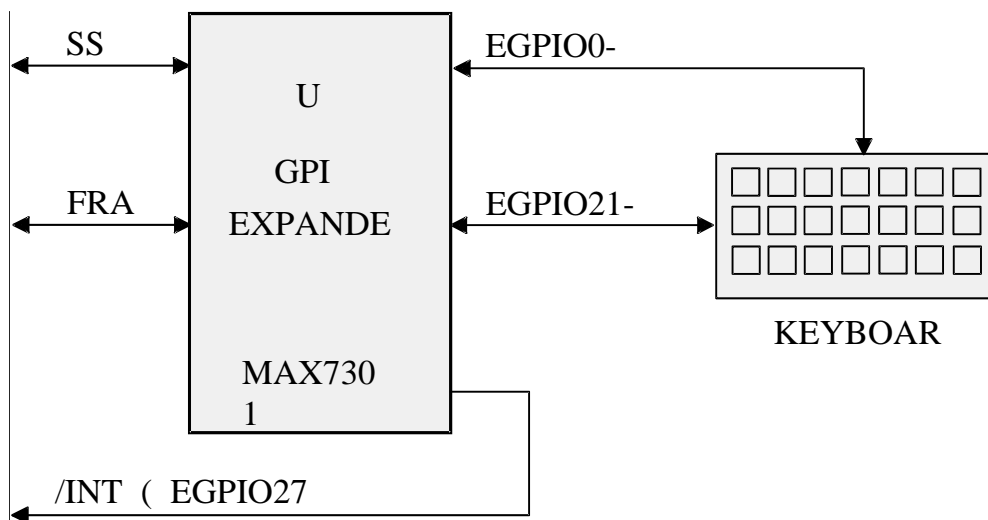


Figure 21: MAX7301/ MAX6957 Connection

The MAX7301/ MAX6957 can be connected externally as well as on-board using Jumpers J6 and J9. Jumper J6 configures the SPI /CS signal while J9 is used to connect the interrupt signal.

<b>J6</b>	<b>Description</b>
closed	/CS signal for MAX7301 / MAX6957 connected to SSP_SFRM on PXA270.
open	External SPI /CS signal used for GPIO expander

*Table 26: SPI /CS Signal for MAX7301/ MAX6957*

<b>J9</b>	<b>Description</b>
closed	Interrupt signal from MAX7301 / MAX6957 connected to SSP_EXTCLK on PXA270.
open	Interrupt signal can be connected to external device.

*Table 27: Interrupt Signal MAX7301 / MAX6957*

### 13.3 Real-Time Clock RTC-8564 (U20)

For real-time or time-driven applications, the phyCORE-PXA270 is equipped with an RTC-8564 Real-Time Clock at U20. This RTC device provides the following features:

- Serial input/output bus (I<sup>2</sup>C), address 0xA2, up to 400 kHz bus frequency
- Power consumption
  - I<sup>2</sup>C bus active (400 kHz): < 1 mA
  - I<sup>2</sup>C bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-PXA270 is equipped with a battery (VBAT), the Real-Time Clock runs independently of the board's power supply.

Programming the Real-Time Clock is done via the I<sup>2</sup>C bus. The Real-Time Clock also provides an interrupt output that extends to GPIO0 on the PXA270 via Jumper J29. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. An interrupt must be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.*

**Note:**

13.4 After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*)

### 13.4 JTAG Interface

The PXA270 provides a JTAG interface for connecting to debuggers, emulators and boundary scan. The interface has its own reset controller (U8). The JTAG interface signals extend to the module's phyCORE-connector. Furthermore, there is an on-board JTAG connector (X2) located at the edge of the module, which has the standard ARM pinout but uses a 2.0 mm pin pitch instead of 2.54 mm. The connector is not populated on the standard version of the phyCORE-PXA270. You can order a specific debug version of the module (denoted by the -D part number extension) or populate a 2\* 10-pin header connector at space X2. The numbering scheme is depicted on the phyCORE-PXA270. The pinout of the JTAG interface at X2 is described in the following table.

Signal	Pin Row		Signal
	A	B	
VREF	1	2	VCC
/JTAG-RESET	3	4	GND
JTAG-TDI	5	6	GND
JTAG-TMS	7	8	GND
JTAG-TCK	9	10	GND
JTAG-RTCK	11	12	GND
JTAG-TDO	13	14	GND
RESET (System)	15	16	GND
N.C.	17	18	GND
N.C.	19	20	GND

Table 28: JTAG Interface





### 14 Technical Specifications

The physical dimensions of the phyCORE-PXA270 are represented in Figure 22.

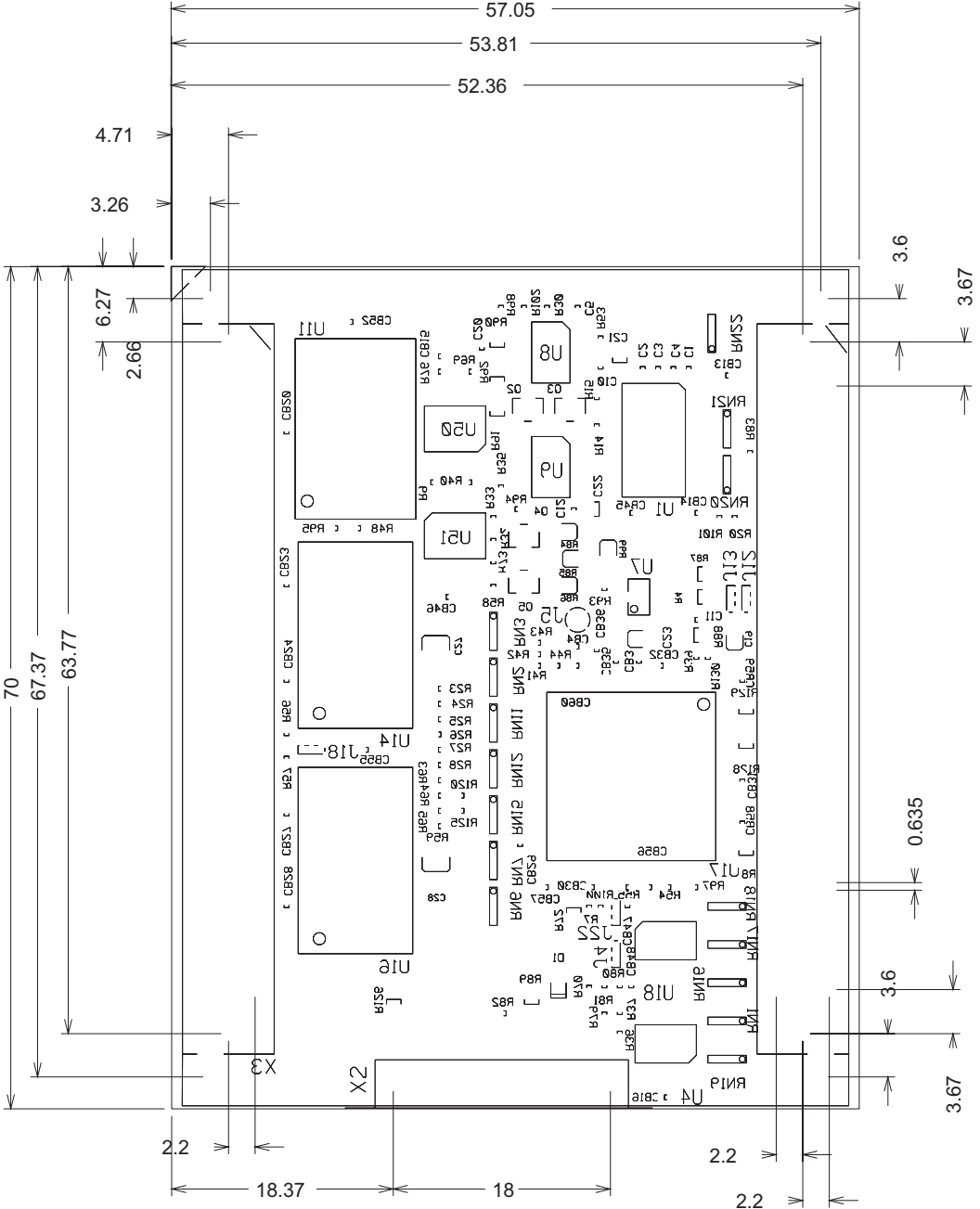


Figure 22: Physical Dimensions

The height of all components on the top side of the PCB is ca. 4.5 mm. The PCB itself is approximately 1.1 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 2 mm.

**Additional Technical Data:**

Parameter	Condition	Characteristics
Dimensions		72 mm x 57 mm
Weight		approximately 25 g with all optional components mounted on the circuit board
Storage Temp. Range		-40°C to +90°C
Operating Temp. Range:		
Extended		-25°C to +85°C
Humidity		max. 95 % r.F. non condensing
Operating voltages: Voltage 3.3V VCC 3.0V VBAT		3.3 V $\pm$ 5 % 3.0 V
Operating Power Consumption: Voltage 3.3 V	(depending on load)	Max. 2 watts

Table 29: Technical Data

*These specifications describe the standard configuration of the phyCORE-PXA270 as of the printing of this manual.*

**Connectors on the phyCORE-PXA270:**

Manufacturer	Molex
Number of pins per contact rows	160 (2 rows of 80 pins each)
Molex part number	52760-1609 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-PXA270. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2 mm) on the underside of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex type number	55091-1609 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex type number	53553-1609 (header)

*Please refer to the corresponding data sheets and mechanical specifications provided by Molex ([www.molex.com](http://www.molex.com)).*

## **15 Hints for Handling the Module**

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

**Caution!**

If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-PXA270 into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected

## 16 U-Boot Boot Loader

Upon delivery of the phyCORE-PXA270 there is a boot loader (U-Boot) stored in the Flash memory. The boot loader is 128 kB in size and is stored in the Flash starting at address 0x00000000. The boot loader performs the initial PXA270 processor configuration following a reset. Configuration includes initialization of the SDRAM, the Flash and the port pins depending on their function. The boot loader subsequently starts the operating system or carries out low level commands in its own monitor such as `tftpboot` for loading images to the SDRAM.

### 16.1 Initializing the phyCORE-PXA270

The boot loader initializes the /CS signals of the PXA270 after reset.

/CS Signal	Busb Width	Usage
/CS0	32-bit	2* 16-bit Flash memory 16 to 64 MByte async / sync
/CS1	16-bit	Free (16-bit asynchronous ROM/RAM)
/CS2	16-bit	Free (16-bit VLIO interface)
/CS3	16-bit	Not used PSKSEL PCMCIA
/CS4	16-bit	Free (16-bit VLIO interface)
/CS5	32-bit	Ethernet Chip 32-bit VLIO interface or free
/SDCS0	32-bit	64 MByte 2*16-bit SDRAM SA1111 mode
/SDCS1	32-bit	64 MByte 2*16-bit SDRAM SA1111 mode
/SDCS2	32-bit	Free
/SDCS3	32-bit	Free

Table 30: U-Boot Memory Configuration

The GPIO port initialization is listed in the following table.

Port	I/O	Configured as
GPIO0	I	GPIO 0 (INT RTC)
GPIO1	I	GPIO 1 (WAKE UP)
<i>GPIO2</i>	I	SYS_ENA
GPIO3	I	PWR_SCL
GPIO4	I	PWR_SDA
<i>GPIO5</i>	I	POWER_CAP0
<i>GPIO6</i>	I	POWER_CAP1
<i>GPIO7</i>	I	POWER_CAP2
<i>GPIO8</i>	I	POWER_CAP3
GPIO9	I	GPIO9
GPIO10	I	GPIO10
GPIO11	I	GPIO11
GPIO12	I	GPIO12
GPIO13	I	GPIO13
GPIO14	I	GPIO14 (L_VSYNC)
GPIO15	O	/CS1
GPIO16	O	PWM0
GPIO17	O	PWM1
GPIO18	I	READY input
GPIO19	I	GPIO19 (L_CS)
GPIO20	I	/SD_CS2
GPIO21	I	/SD_CS3
GPIO22	I	GPIO22
GPIO23	I	SCLK SPI clock
GPIO24	I	SFRM SPI frame signal
GPIO25	O	SPI TxD transmit line
GPIO26	I	SPI RxD receive line
GPIO27	I	SPI EXTCLK external master clock
GPIO28	O	AC97 BitCLK
GPIO29	I	AC97 SDATA_IN0
GPIO30	O	AC97 SDATA_OUT
GPIO31	O	AC97 SYNC
GPIO32	I	MMC_CLK
GPIO33	O	/CS5
GPIO34	I	FF-UART RxD
GPIO35	I	FF-UART CTS
GPIO36	I	FF-UART DCD
GPIO37	I	FF-UART DSR
GPIO38	I	FF-UART RI
GPIO39	O	FF-UART TxD

Table 31: Port Configuration GPIO0-39

Port	I/O	Configured as
GPIO40	O	FF-UART DTR
GPIO41	O	FF-UART RTS
GPIO42	I	BT-UART RxD
GPIO43	O	BT-UART TxD
GPIO44	I	BT-UART CTS
GPIO45	O	BT-UART RTS
GPIO46	I	STD-UART RxD
GPIO47	O	STD-UART TxD
GPIO48	O	/POE PCMCIA
GPIO49	O	/PWE PCMCIA
GPIO50	O	/PIOR PCMCIA
GPIO51	O	/PIOW PCMCIA
GPIO52	O	GPIO52 (INT ETHERNET)
GPIO53	I	GPIO53
GPIO54	O	/PCE_2
GPIO55	O	/PREG PCMCIA
GPIO56	I	/PWAIT PCMCIA
GPIO57	I	/IOIS16 PCMCIA
GPIO58	O	LDD0, data bus to LCD display
GPIO59	O	LDD1, data bus to LCD display
GPIO60	O	LDD2, data bus to LCD display
GPIO61	O	LDD3, data bus to LCD display
GPIO62	O	LDD4, data bus to LCD display
GPIO63	O	LDD5, data bus to LCD display
GPIO64	O	LDD6, data bus to LCD display
GPIO65	O	LDD7, data bus to LCD display
GPIO66	O	LDD8, data bus to LCD display
GPIO67	O	LDD9, data bus to LCD display
GPIO68	O	LDD10, data bus to LCD display
GPIO69	O	LDD11, data bus to LCD display
GPIO70	O	LDD12, data bus to LCD display
GPIO71	O	LDD13, data bus to LCD display
GPIO72	O	LDD14, data bus to LCD display
GPIO73	O	LDD15, data bus to LCD display
GPIO74	O	LCD_FCLK, frame clock
GPIO75	O	LCD_LCLK, line clock
GPIO76	O	LCD_PCLK, pixel clock
GPIO77	O	LCD_ACBIAS BIAS oder LCD_Enable
GPIO78	O	/CS2
GPIO79	O	/PSKSEL (/CS3)
GPIO80	O	/CS4

Table 32: Port Configuration GPIO40-80

Port	I/O	Configured as
GPIO81	I	GPIO 81
GPIO82	I	GPIO 82
GPIO83	I	GPIO 83
GPIO84	I	GPIO 84
GPIO85	O	/PCE_1
GPIO86	I	GPIO86
GPIO87	I	GPIO87
GPIO88	I	GPIO88
GPIO89	I	GPIO89
GPIO90	I	GPIO90
GPIO91	I	GPIO91
GPIO92	I/O	MMC_DAT0
GPIO93	I	GPIO93
GPIO94	I	GPIO94
GPIO95	I	GPIO95
GPIO96	I	GPIO96
GPIO97	I	GPIO97
GPIO98	I	GPIO98
GPIO99	I	GPIO99
GPIO100	I	GPIO100
GPIO101	I	GPIO101
GPIO102	I	GPIO102
GPIO103	I	GPIO103
GPIO104	I	GPIO104
GPIO105	I	GPIO105
GPIO106	I	GPIO106
GPIO107	I	GPIO107
GPIO108	I	GPIO108
GPIO109	I/O	MMC_DAT1
GPIO110	O	MMC_DAT2_CS0
GPIO111	O	MMC_DAT3_CS1
GPIO112	I/O	MMC_CMD
GPIO113	O	AC97_RESET
GPIO114	I	GPIO114
GPIO115	I	GPIO115
GPIO116	I	GPIO116
GPIO117	I/O	I <sup>2</sup> C SDA
GPIO118	O	I <sup>2</sup> C SCL
GPIO119	I	GPIO119
GPIO120	I	GPIO120
GPIO121	I	GPIO121

Table 33: Port Configuration GPIO81-121



## 16.2 Communication with U-Boot

The U-Boot boot loader communicates exclusively over FF\_UART with the user. It is required that at least the RS-232 signals RS\_TxD, RS\_RxD and GND of the phyCORE-PXA270 are connected to the PC's serial interface.

Signal on phyCORE	Signal on Host-PC
RS_TxD (Molex pin X3D23)	PC_RxD (pin 2 DB-9)
RS_RxD (Molex pin X3D22)	PC_TxD (pin 3 DB-9)
GND (e.g. Molex pin X3D24)	PC_GND (pin 5 DB-9)

Table 34: RS-232 Connection to Host-PC

A terminal program such as HyperTerminal (Windows) or miniCOM (Linux) can be used to display the output message of the U-Boot boot loader on the host-PC. The interface settings should be as follows.

- 115200 baud
- 8 data bits
- No priority
- 1 stop bit

Please note that the U-Boot boot loader only works line by line.

## 16.3 Important U-Boot Commands

The U-Boot boot loader provides a large number of commands that are available to the user. These are constantly being expanded and can be freely configured as well. Below are a few important commands of the U-Boot to get familiar.

- **help**

Lists all commands that are contained in the current U-Boot version and that have been configured.

*help*

- **Erase**

Erases a sector in the Flash. The boot loader is protected against accidental erasure by software. The following example erases the memory area of a Linux image.

*erase 4000 1FFFF*

- **tftpboot**

With this command an image can be loaded to the phyCORE from the >tftpboot directory (FTP must be running). The following example stores a binary image with the name "phyImage" starting at address 0xA2000000 in the SDRAM.

*tftpboot a3000000 phyImage*

- **cp**

This is a copy command that can write to the Flash as well. In this example the phyImage (*see tftpboot*) can be copied from the SDRAM to the Flash.

*cp.b a3000000 40000 1FFFFFF*

- **bootm**

This command loads an image from the Flash starting at address 0x00040000 (e.g. Linux) to the SDRAM and starts it there.

*Bootm 40000*

- **printenv**

This command returns the configuration data which was loaded from the I<sup>2</sup>C EEPROM to the SDRAM.

*printenv*

- **setenv**

This command writes a new configuration line to the SDRAM. In the example the IP address of the PC is set, from which the tftpboot acquires its image.

*setenv serverip 192.168.0.1*

- **saveenv**

This command writes the configuration data from the SDRAM to the I<sup>2</sup>C EEPROM. Thus the modifications are still present after power-off.

*saveenv*

## 17 Revision History

Date	Version numbers	Changes in this manual
01-June-2005	Manual L-667e_0 PCM-027 PCB# 1235.0	Preliminary edition.
14-March-2006	Manual L-667e_1 PCM-027 PCB# 1235.2	First release edition. Sections added for DeepSleep mode and reset configuration. Minor changes in Molex pinout supporting new functions. SDRAM supply options revised.

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**Dokumentnummer:** L-667e\_1, March 2006

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**How would you improve this manual?**

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**Did you find any mistakes in this manual?** page

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\_\_\_\_\_

**Return to:**

PHYTEC Technologie Holding AG  
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