PHYTEC

Carrier Board for phyCORE-PXA270

Hardware Manual

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

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Preface

This manual describes only the functions of the PHYTEC phyCORE-PXA270 Carrier Board. The controllers and relevant Single Board Computers for use with the Carrier Board are not described herein. Additional controller- and board-level information and technical descriptions can be found in appropriate Hardware Manual or User's Manual support documentation. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the phyCORE-PXA270 Carrier Board

PHYTEC Carrier Boards (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-PXA270 Carrier Board is one of a series of PHYTEC Carrier Boards supporting the phyCORE-PXA270 Single Board Computer module. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The Carrier Board phyCORE-PXA270 is a universal carrier board for start-up and programming of the PHYTEC phyCORE-PXA270 Single Board Computer module with two high density SMT (160 pins each, 0.63 mm pitch) pin header connectors. The Carrier Board is fully equipped with all mechanical and electrical components necessary for the speedy and secure insertion and subsequent programming of the high-density PHYTEC phyCORE module. These components include TFT display connection, touch screen interface, Ethernet transformer and connector, DB-9, USB and power socket connectors.

The phyCORE module can be plugged like a "big chip" onto the Carrier Board's mating Molex connectors. Once programmed, the phyCORE module can be removed from the Carrier Board and inserted like a "big chip" in a target hardware application. Given the compact nature of the Carrier Board use of the complete hardware platform as OEM part in human-machine-interface (HMI) applications is also possible.

The hardware manual for this Carrier Board does not describe the features and functions of the phyCORE-PXA270 SBC module, as this is not relevant for the basic functioning of the Carrier Board. For module and controller-specific features *please refer to the corresponding Hardware Manuals/User's Manuals*.

The Carrier Board offers the following features:

- Molex connectors for mating with phyCORE-PXA270 SBC module
- Connector for 8.4" Sharp TFT display with 640*480 pixel resolution, incl. adjustable inverter for background illumination
- AC97 controller WM9712L with touch and sound interface (Line-IN, Line-OUT, MIC-IN and 0.4 watts speaker)
- Two DB-9 sockets for RS-232 interface from FF-UART and BT-UART, 2*5 pin header for IR-UART
- One DB-9 plug for CAN interface, optical isolation
- RJ-45 Ethernet connector with transformer for 100/10 MBit/s
- USB host socket for PXA270 USB host interface
- USB client socket for PXA270 USB client interface
- Power supply for unregulated input voltage from 12 V (optional 24 V). It supplies regulated +3.3 V for the phyCORE-PXA270. Additional +5 V is created for the IDE and CF card and LCD/inverter circuitry.
- Optional battery charger circuitry for NiMH batteries
- Power magement for MMC, CF, IDE and LC display
- Two user programmable LEDs
- Optional IDE interface for two 2.5" hard disks (Master / Slave)
- Interface for matrix keyboards
- JTAG interface
- AC97 expansion port
- Reset and GPIO push button

Expansion Board with:

- 1* MultiMedia card
- 1* Compact Flash
- 1* Reset button
- 1* GPIO button
- 1* USB-OTG socket for PXA270 USB interface
- 4* LEDs via PLD GPIOs

1.1 Block Diagram

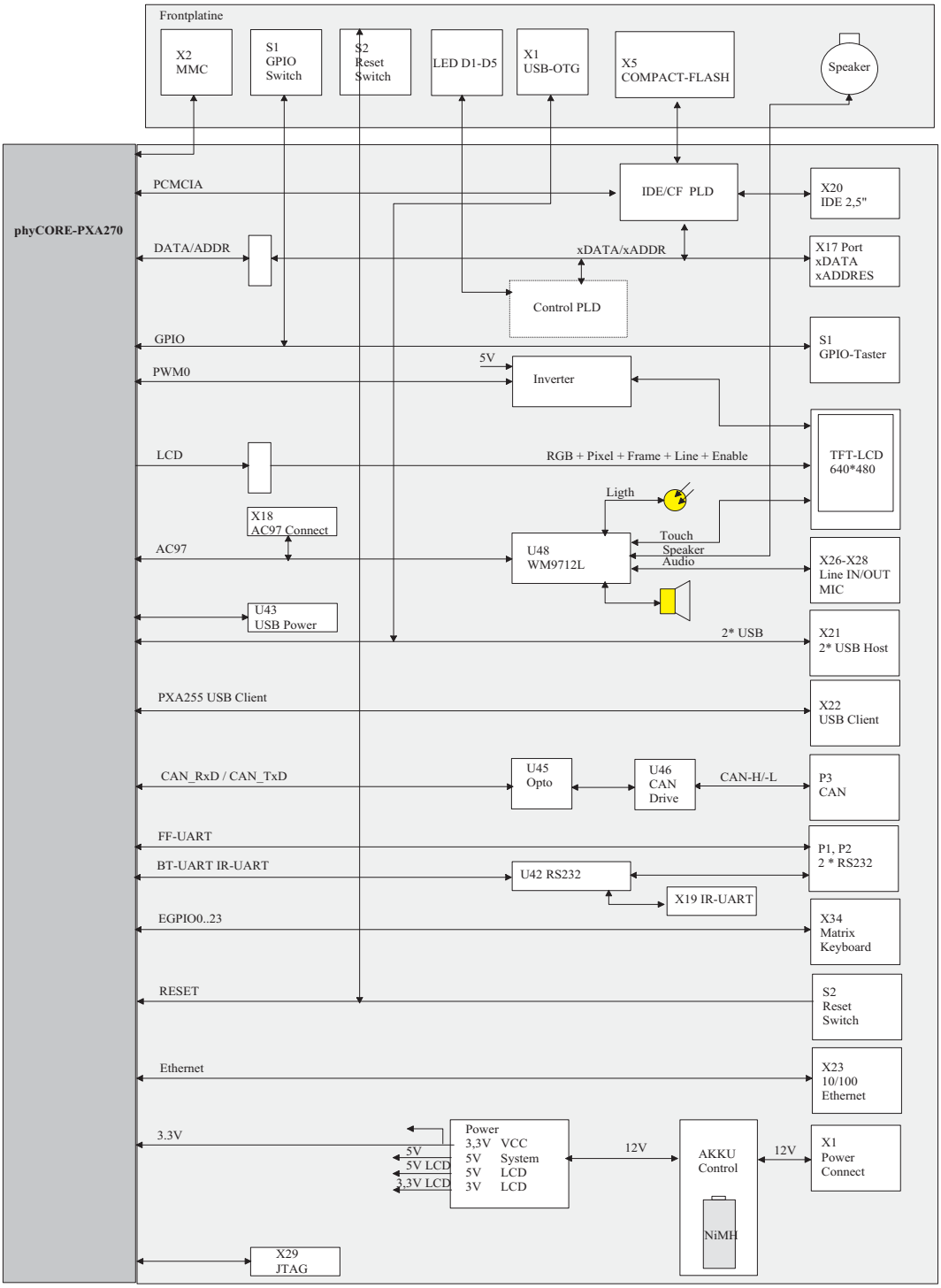


Figure 1: Block Diagram of the Carrier Board

1.2 Overview

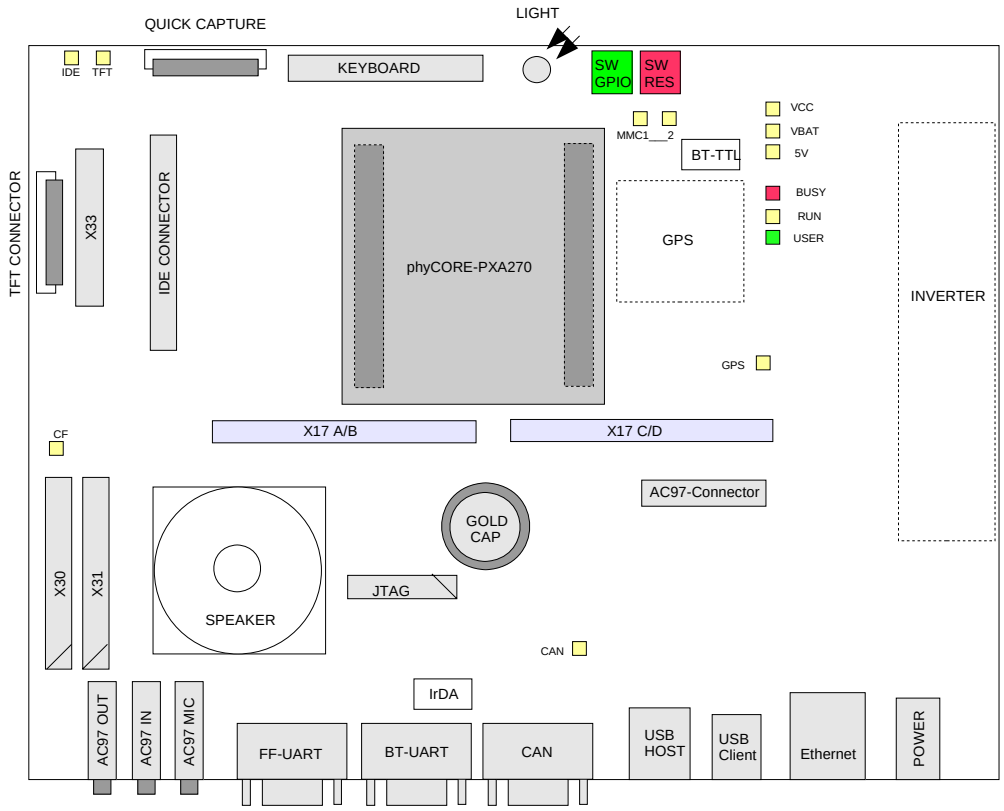


Figure 2: Carrier Board Overview (Top View)

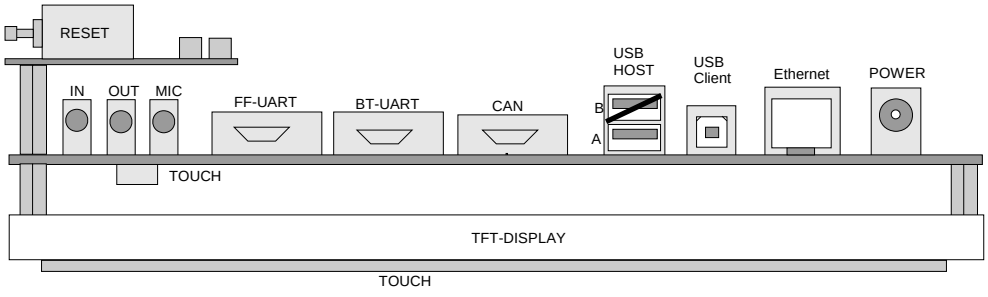


Figure 3: Carrier Board Overview (Connector Side View)

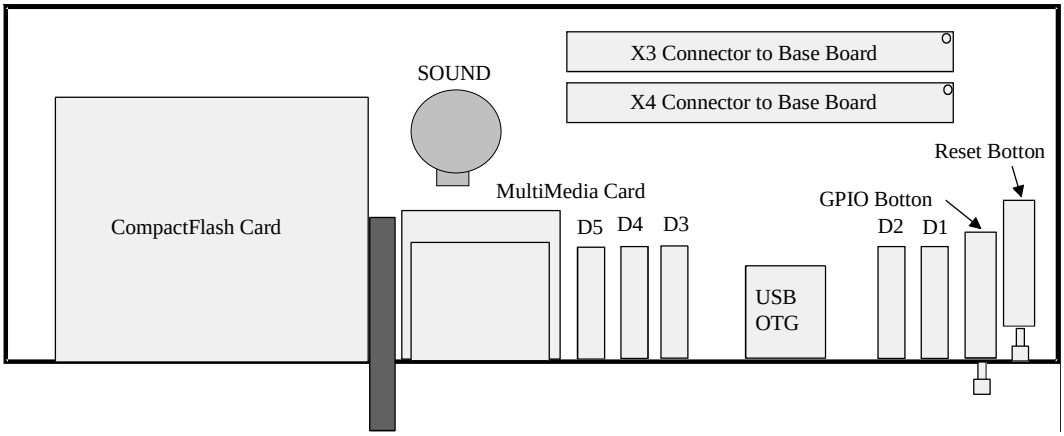


Figure 4: Expansion Board Overview (Top View)

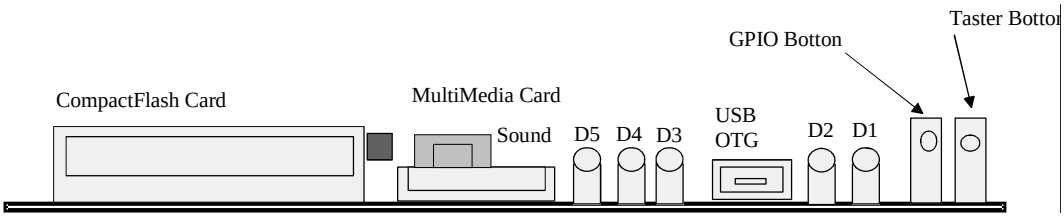


Figure 5: Expansion Board Overview (Side View)

2 Port Pin Initialization

The Intel PXA270 controller provides a wide variety of chip-level features that are routed to GPIO pins with alternative functions. The following functions are used on the phyCORE-PXA270 Carrier Board:

- MMC Card 0/1
- PCMCIA interface
- 16-bit LCD interface
- AC97 interface
- FF-UART, BT-UART and IR-UART
- SSP and NSSP
- I²C bus
- USB client and host

Either the operating system installed on the phyCORE-PXA270 or the boot loader (e.g. U-Boot) must initialize the GPIO port pins in questions as shown in the table below:

Port	I/O	Configured as
GPIO0	I	GPIO 0 (INT RTC)
GPIO1	I	GPIO 1 (WAKE UP)
GPIO2[1]	I	SYS_ENA
GPIO3	I	PWR_SCL
GPIO4	I	PWR_SDA
GPIO5	I	POWER_CAP0
GPIO6	I	POWER_CAP1
GPIO7	I	POWER_CAP2
GPIO8	I	POWER_CAP3
GPIO9	I	GPIO9
GPIO10	I	GPIO10
GPIO11	I	GPIO11
GPIO12	I	GPIO12
GPIO13	I	GPIO13
GPIO14	I	GPIO14 (L_VSYNC)
GPIO15	O	/CS1
GPIO16	O	PWM0
GPIO17	O	PWM1
GPIO18	I	READY input
GPIO19	I	GPIO19 (L_CS)
GPIO20	I	/SD_CS2
GPIO21	I	/SD_CS3
GPIO22	I	GPIO22
GPIO23	I	SCLK SPI clock
GPIO24	I	SFRM SPI frame signal
GPIO25	O	SPI TxD transmit line
GPIO26	I	SPI RxD receive line
GPIO27	I	SPI EXTCLK external master clock
GPIO28	O	AC97 BitCLK
GPIO29	I	AC97 SDATA_IN0
GPIO30	O	AC97 SDATA_OUT
GPIO31	O	AC97 SYNC
GPIO32	I	MMC_CLK
GPIO33	O	/CS5
GPIO34	I	FF-UART RxD
GPIO35	I	FF-UART CTS
GPIO36	I	FF-UART DCD
GPIO37	I	FF-UART DSR
GPIO38	I	FF-UART RI
GPIO39	O	FF-UART TxD

Table 1: Port Configuration GPIO0-39

[1] : Ports shown in *italic style* have special function on the phyCORE-PXA270 and can not be used externally.

Port	I/O	Configured as
GPIO40	O	FF-UART DTR
GPIO41	O	FF-UART RTS
GPIO42	I	BT-UART RxD
GPIO43	O	BT-UART TxD
GPIO44	I	BT-UART CTS
GPIO45	O	BT-UART RTS
GPIO46	I	STD-UART RxD
GPIO47	O	STD-UART TxD
GPIO48	O	/POE PCMCIA
GPIO49	O	/PWE PCMCIA
GPIO50	O	/PIOR PCMCIA
GPIO51	O	/PIOW PCMCIA
GPIO52	O	GPIO52 (INT ETHERNET)
GPIO53	I	GPIO53
GPIO54	O	/PCE_2
GPIO55	O	/PREG PCMCIA
GPIO56	I	/PWAIT PCMCIA
GPIO57	I	/IOIS16 PCMCIA
GPIO58	O	LDD0, data bus to LCD display
GPIO59	O	LDD1, data bus to LCD display
GPIO60	O	LDD2, data bus to LCD display
GPIO61	O	LDD3, data bus to LCD display
GPIO62	O	LDD4, data bus to LCD display
GPIO63	O	LDD5, data bus to LCD display
GPIO64	O	LDD6, data bus to LCD display
GPIO65	O	LDD7, data bus to LCD display
GPIO66	O	LDD8, data bus to LCD display
GPIO67	O	LDD9, data bus to LCD display
GPIO68	O	LDD10, data bus to LCD display
GPIO69	O	LDD11, data bus to LCD display
GPIO70	O	LDD12, data bus to LCD display
GPIO71	O	LDD13, data bus to LCD display
GPIO72	O	LDD14, data bus to LCD display
GPIO73	O	LDD15, data bus to LCD display
GPIO74	O	LCD_FCLK, frame clock
GPIO75	O	LCD_LCLK, line clock
GPIO76	O	LCD_PCLK, pixel clock
GPIO77	O	LCD_ACBIAS BIAS or LCD_Enable
GPIO78	O	/CS2
GPIO79	O	/PSKSEL (/CS3)
GPIO80	O	/CS4

Table 2: Port Configuration GPIO40-80

Port	I/O	Configured as
GPIO81	I	GPIO 81
GPIO82	I	GPIO 82
GPIO83	I	GPIO 83
GPIO84	I	GPIO 84
GPIO85	O	/PCE_1
GPIO86	I	GPIO86
GPIO87	I	GPIO87
GPIO88	I	GPIO88
GPIO89	I	GPIO89
GPIO90	I	GPIO90
GPIO91	I	GPIO91
GPIO92	I/O	MMC_DAT0
GPIO93	I	GPIO93
GPIO94	I	GPIO94
GPIO95	I	GPIO95
GPIO96	I	GPIO96
GPIO97	I	GPIO97
GPIO98	I	GPIO98
GPIO99	I	GPIO99
GPIO100	I	GPIO100
GPIO101	I	GPIO101
GPIO102	I	GPIO102
GPIO103	I	GPIO103
GPIO104	I	GPIO104
GPIO105	I	GPIO105
GPIO106	I	GPIO106
GPIO107	I	GPIO107
GPIO108	I	GPIO108
GPIO109	I/O	MMC_DAT1
GPIO110	O	MMC_DAT2_CS0
GPIO111	O	MMC_DAT3_CS1
GPIO112	I/O	MMC_CMD
GPIO113	O	AC97_RESET
GPIO114	I	GPIO114
GPIO115	I	GPIO115
GPIO116	I	GPIO116
GPIO117	I/O	I²C SDA
GPIO118	O	I²C SCL
GPIO119	I	GPIO119
GPIO120	I	GPIO120
GPIO121	I	GPIO121

Table 3: Port Configuration GPIO80-121

3 Jumpers

For configuration purposes, the phyCORE-PXA270 Carrier Board has 10 removable and 32 solder jumpers, most of which have been installed prior to delivery depending on the board's configuration. Solder jumpers should not be changed by the user. *Figure 6* illustrates the numbering of the jumper pads, while *Figure 7* indicates the location of the jumpers on the board.

Figure 6: Numbering of the Jumper Pads

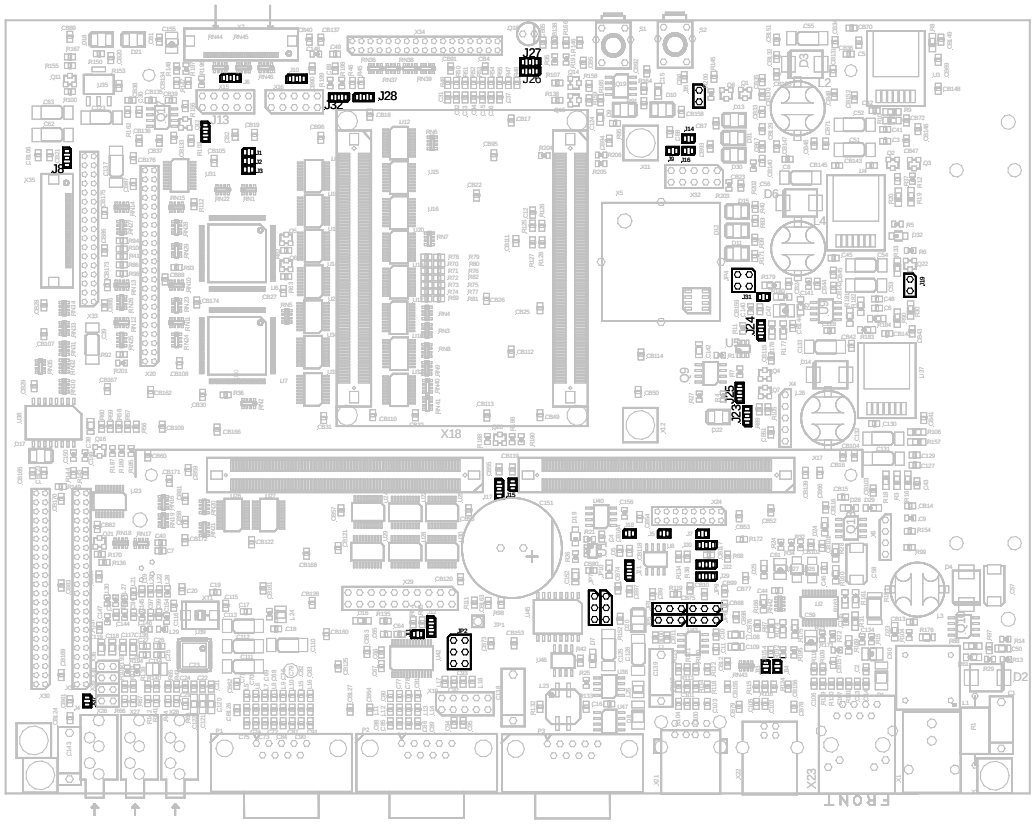


Figure 7: Location of the Jumpers (Carrier Board)

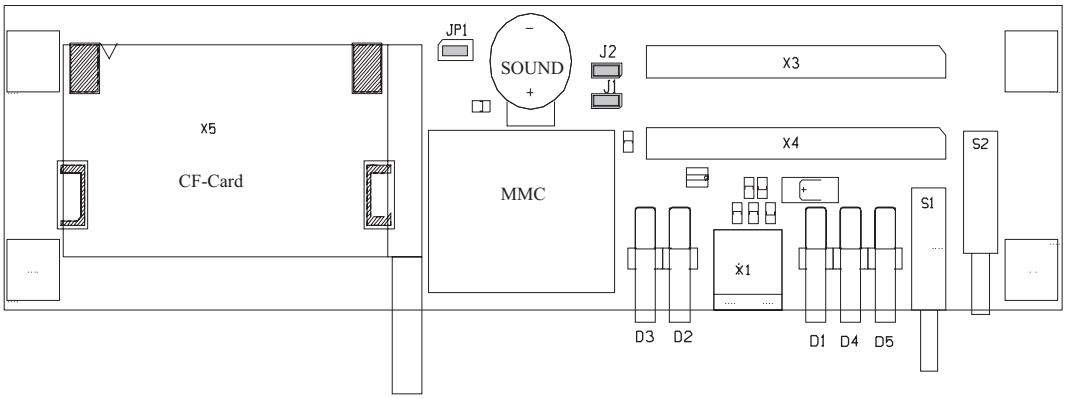


Figure 8: Location of the Jumpers (Expansion Board)

Description of the jumper functions is provided in the following manual sections. The jumpers are grouped by function as follows:

Jumper	**Function/Section**
JP3, JP5, JP6, JP9	USB host interface, *refer to section 7.*
JP7, JP10	CAN Interface, *refer to section 11.*
JP2	RS-232 transceiver BT-UART and IR-UART, *refer to section 10.2.*

Table 4: Jumper Functions and Section Reference

4 Power Supply System

The Carrier Board operates with a supply voltage of 12 VDC (optional 24 VDC). The on-board voltage converters generate all supply voltages required for the components on the Carrier Board, the Expansion Board and the phyCORE-PXA270. The supply voltage can also be used for the optional battery charger circuitry.

Supply voltage 1: +3.3 V (VCC)
Supply voltage 2: +5 V (IDE and CF card)
Supply voltage 3: +5 V (LCD and inverter)

The controller signal SYS_ENA can be used to switch all three suplly voltages. This requires closing jumper JP19 on the Carrier Board.

Supply voltage 1: +3.3 V (VCC)

Nearly all of the components on the Carrier Board, the Expansion Board and the phyCORE-PXA270 are powered by VCC (+3.3 V). The supply voltages for the CompactFlash Card and the Multimedia Card on the Expansion Board can be switched with the help of transistors. The voltage converter allows for a maximum current draw of 2 amps at 3.3 V (+/-5 %). The efficiency of the converter is over 80 %.

Supply voltage 2: +5 V (IDE and CF card)

The 5 V supply voltage is intended only for the 2.5" hard drive and the CF card. It can be switched on or off during operation. The voltage converter allows for a maximum current draw of 2 amps at 5 V (+/- 5 %). The efficiency of the regulator is over 80 %.

Supply voltage 3: +5 V (LCD and inverter)

The inverter for the LCD background lighting is powered by this 5 V supply voltage. The PXA270 switches the background lighting on and off or dims it over its PWM0 signal. A linear voltage regulator is used to generate the 3.3 V LCD logic supply voltage from the 5 V LCD. The voltage converter allows for a maximum current draw of 1.5 amps at 5 V (+/- 5%). The efficiency of the regulator is over 80 %.

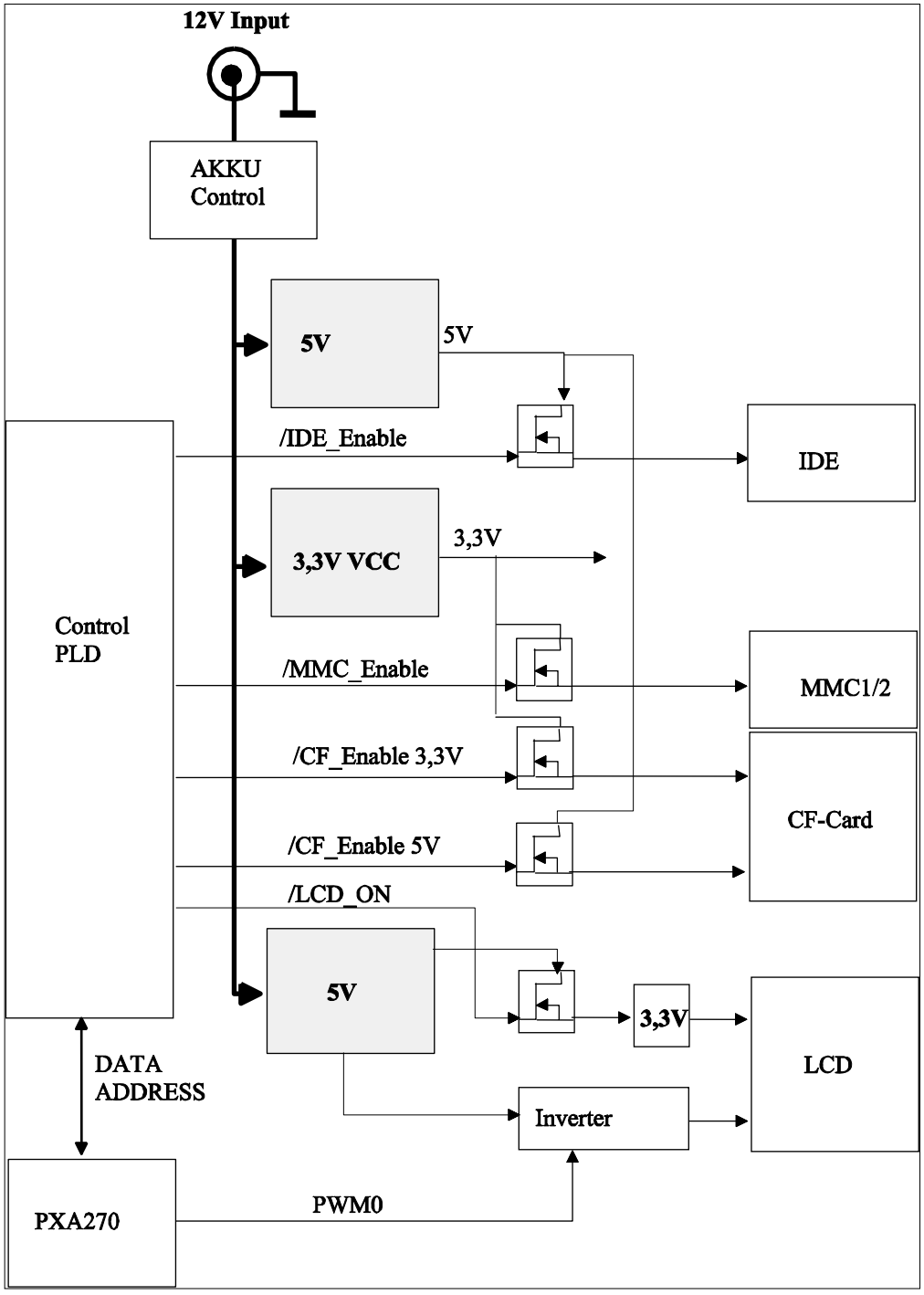


Figure 9: Power Supply Block Diagram

Battery Charger Circuitry for 6 NiMH Batteries

The Carrier Board can be populated with an optional battery charger circuit for six (when using a 12 V input voltage, up to 12 possible, requires different hardware configuration and 24 V input voltage) NiMH batteries. In this case the BQ24703 battery charge controller switches the voltage from the power adapter to battery operation. It will charge the batteries when the Carrier Board is supplied with power through a wall adapter.

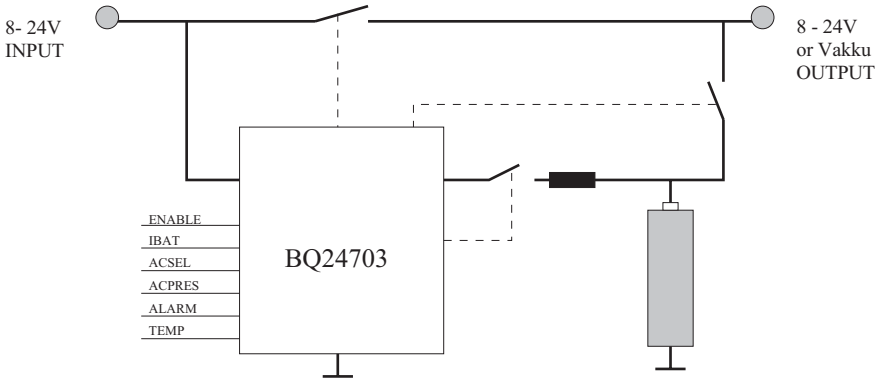


Figure 10: Battery Charger Circuitry

Note:
The battery charger register (Control PLD register 11, *refer to section 5.2.1*) is only available with PCB revision 1220.2 and higher.

VBAT Supply and DeepSleep

The PXA270 controller can enter a so-called DeepSleep mode. In this mode only the battery supply VBAT is required for powering the controller. All other voltages can be turned off in this mode. For this purpose the controller signal SYS_ENA is available. This feature is activate via Jumper J19 on the Carrier Board. If SYS_ENA = "0" all three supply voltages are turned off.

Before entering DeepSleep Mode is it important to render the SDRAM into self-refresh mode and to ensure that VBAT is available to supply the device internally. If the system "wakes up" and resumes full operation it will continue to excecute at the same stage where it was before going into DeepSleep Mode. Power consumption during this mode is in the lower milliampere range.

For better support of this function improvements in the board's VBAT support circuitry were made on PCB revision 1220.3. VBAT is now created by a 3.1 V linear regulator. Power can be supplied from three different sources. If the DC input voltage is supplied from a wall adapter it will first be converted down by a 5 V linear regulator and a gold cap is charged simultaneoulsy. This voltage then supplies the 3.1 V linear voltage regulator for VBAT. In the absense of the DC input voltage power is supplied by the battery. If neither the DC input nor the battery voltage are available then the gold cap can buffer the VBAT supply for 20 minutes while the battery is changed or the DC input is restored. Jumper J35 can be used to monitor VBAT via LED D31. If VBAT is present the LED will illuminate. It is recommended to leave J35 open (disconnect the LED) because power consumption of the LED is relatively high.

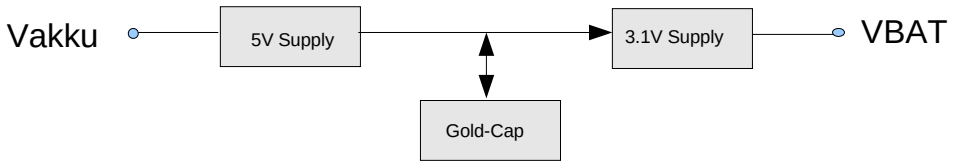


Figure 11: VBAT Supply

5 Memory Configuration

The Carrier Board for the phyCORE-PXA270 uses the module's /CS1 and /CS2 signals as well as the PCMCIA interface for controlling the components on the data bus. All other /CS and /SDCS signals from the phyCORE-PXA270 are routed to and can be controlled by the address decoder (control PLD U7) in order to connect the external data bus drivers and allow for custom-specific modification options. The PCMCIA interface is managed by the second address decoder (Control PLD U6), which generates all necessary signals for the CF card and the IDE interface.

/CS0	2 * 16-bit Flash memory 16 to 64 MByte asynchronous / synchronous (optional 16-bit Flash memory 8 MByte asynchronous)
/CS1	16-bit VLIO interface, address decoder U7 on the Carrier Board
/CS2	16-bit VLIO interface, expansion connector X17 on the Carrier Board
/CS3	Used for PSKSEL (PC Card Socket Select)
/CS4	free 16-bit VLIO interface
/CS5	Ethernet chip with 32-bit VLIO interface on the phyCORE-PXA270 module

The SDRAM /CS signals extend to the Carrier Board's X-Bus connector X17. Depending on the phyCORE-PXA270 configuration option, these /CS signals /SDCS_0 through /SDCS_3 are connected with the chips of both SDRAM banks.

/SDCS_0	64 MB 2*16-bit SDRAM on the phyCORE-PXA270
/SDCS_1	optional 64 MB 2*16-bit SDRAM on the phyCORE-PXA270
/SDCS0/1	optional 128 MB 2*16-bit SDRAM on the phyCORE-PXA270 (applicable when using SDRAM with two /CS signals per chip)
/SDCS2/3	optional 128 MB 2*16-bit SDRAM on the phyCORE-PXA270 (applicable when using SDRAM with two /CS signals per chip)

5.1 Interrupts

The interrupt signals for components on the phyCORE-PXA270 are configured on the phyCORE module itself. Because of the limited number of available GPIOs, the signals /MMC_DET and MMC-WP cannot be connected to GPIO9 and GPIO10 on the phyCORE module, hence these functions are not available. These GPIO signals are instead used for the interrupt inputs /PLD_INT for power management functions and AC_INT from the AC97 Codec (*refer to Table 6*). This is implemented on the Carrier Board.

GPIO	Signal	Jumper	Description
GPIO_0	/RTC_INT	J29	Low active interrupt RTC-8564
GPIO_52	LAN_IRQ	J20	High active interrupt for LAN91C11 Ethernet controller
GPIO_114	/CAN_INT	J23	Low active interrupt for SJA1000 CAN controller
GPIO27 (SSP_EXT CLK)	EGPIO27	J9	Low active interrupt for MAX7301 matrix keyboard

Table 5: Interrupt Assignment phyCORE-PXA270

On the Carrier Board interrupts are used for the CF card, IDE interface, AC97, touch and power management circuits. These are either hard-wired over solder jumpers or managed in the two address decoders.

GPIO	Signal	Jumper / PLD	Description
GPIO_1	/SW_ON	J15	Low active interrupt for User Switch
GPIO_9	/PLD_INT		Low active interrupt for power management
GPIO_10	AC_INT	J18	High active interrupt for WML9712 AC97 controller
GPIO_13	xIDE_IRQ	J1	High active interrupt for IDE drive
GPIO_12	/CF_CDINT (internal)	U6	Low active interrupt /CD1 and /CD2 CF card. Support of hot-plugging CF cards; an interrupt is released each time a card is inserted ot removed, only available with PCB revision 1220.2 and higher.
GPIO_11	CF_IRQ	J2	High active interrupt CF card. The active level of an interrupt depends on the card type (memory, TrueIDE, etc.) With TrueIDE cards the level is active high.

Table 6: Interrupt Assignment Carrier Board

5.2 Control PLD (U7)

Control PLD U7 controls the drivers for the buffered data and the address bus. Furthermore, all power management, control and interrupt functions, except for the CF card and the IDE interface, are integrated in this device. The individual functions will be explained in greater detail in the register description.

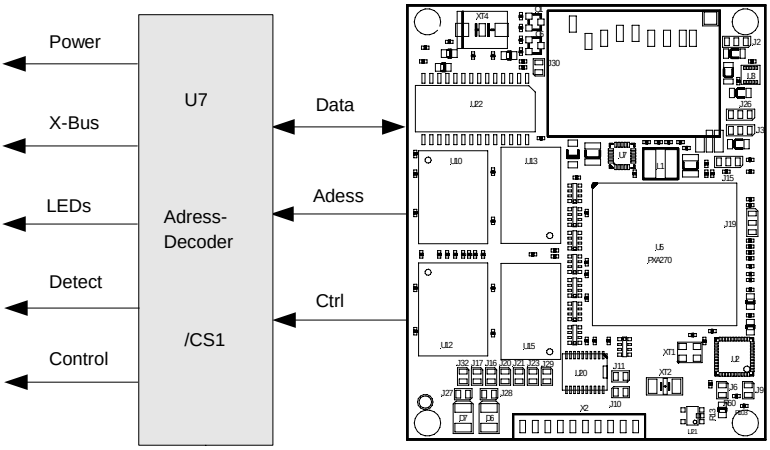


Figure 12: Control PLD U7

5.2.1 Control PLD (U7) Registers

Control PLD U7 is addressed over the PXA270's Chip Select signal /CS_1 The bus width is set to 16-bit as a VLIO interface. The registers of the Control PLD are listed in the following table. The register's reset value after the system start is shown below the description.

REG	ADDR.	D7-D4	D3	D2	D1	D0
CTRL0	0x04000000	Res	Res	GPIO0	RESOUT	SRES
RESET				0	0	0
CTRL 1	0x04000002	Res	PM_5V	CANPWR	Res	Res
RESET			1	0	0	0
CTRL 2	0x04000004	Res	Res	LEDUSER	LEDBUSY	LEDRUN
RESET			0	0	0	0
CTRL 3	0x04000006	Res	POS1	POS2	LCDON	LCDPWR
RESET			0	0	0	0
CTRL 4	0x04000008	Res	Res	Res	Res	MMC1PWR
RESET			0	0	0	0
CTRL 5	0x0400000A	Res	WP	DET	LED	MMC2PWR
RESET			0	X	0	0
CTRL 6	0x0400000C	Res	INT3	INT2	INT1	INT0
RESET			0	0	0	0
CTRL 7	0x0400000E	Res	INT PM_5V	INT MMCDET	INT FF_RI	INT BT_DET
RESET			0	0	0	0
CTRL 8	0x04000010	Res	BT_Rx	FF_RI	BT_SD	FF_SD
RESET					0	0
CTRL 9	0x04000012	Res	Res	AC97 ENA	/FL_DIS	FL_WP
RESET			0	0	0	1
CTRL 10	0x04000014	Res	GPS_ENA	GPS_PWR	Res	Res
RESET			0	0	0	0
CTRL 11	0x04000016	Res	ALARM	ACPRES	ACSEL	ACENA
RESET			0	X	1	1

Table 7: Control PLD U7 Overview and Reset Values

The reset properties for SRES on the Carrier Board are set in control register 0.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL0	0x04000000	Res	Res	GPIO0	RESOUT	SRES
RW		R/W=0	R/W=0	R/W	R/W	R/W
Signal Name				GPIO_0	/RESET_OUT	/RES_X /RESIN

Table 8: PLD U7 Control Register 0

SRES Setting this bit generates a system reset.
RESOUT This bit is **not** used on the PXA270 controller.
GPIO0 This bit is **not** used on the PXA270 controller.

PLD U7 control register 1 is used for switching and controlling various supply voltages. The bit PM_5V displays whether the 5 V voltage is still active or if it was shut off due to a wall adapter output voltage drop to less than 8 V. If 5V_OFF is set, the 5 V supply can be shut off independently of the input voltage level. The external CAN supply voltage can be switched on with the CANPWR bit.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL1	0x04000002	Res	PM_5V	CANPWR	Res	Res
RW		R/W=0	R	R/W	R/W=0	R/W=0
Signal Name			PM_5V	CAN_VE		

Table 9: PLD U7 Control Register 1

CANPWR Turns on the external CAN supply voltage (bit set).
PM_5V Indicates that 5 V supply voltage is active.

The registers for controlling the Carrier Board's user LEDs D11, D12 and D15 are in U7 control register 2. The register values are negated by the PLD so that the LEDs can be switched with a high-active level. The LEDs are located on the Carrier Board between the phyCORE module and the backlight inverter board (*refer to Figure 2*).

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL2 RW	0x04000004	Res R/W=0	Res R/W=0	LEDUSER R/W	LEDBUSY R/W	LEDRUN R/W
Signal Name				x/LED_USER	x/LED_BUSY	x/LED_RUN

Table 10: PLD U7 Control Register 2

LEDRUN Setting this bit will turn on user LED D12.
LEDBUSY Setting this bit will turn on user LED D15.
LEDUSER Setting this bit will turn on user LED D11.

The voltage settings and the adjustment of the TFT display can be carried out in control register 3. The bit POS1 is connected to the R/L signal of the display while POS2 is connected to the display's U/D signal. The data line drivers can be switched to active with LCD_ON. The supply voltage of the LCD is switched on with LCDPWR.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 3 RW	0x04000006	Res R/W=0	POS1 R/W	POS2 R/W	LCDON R/W	LCDPWR R/W
Signal Name			L_POS1	L_POS2	/LCD_ON	LCD_P_ON

Table 11: PLD U7 Control Register 3

POS1/POS2 The display adjustment is set here. The display can be mirrored in the X direction as well as the Y direction with these two bits. If both bits are changed at the same time, then the image will be rotated in an 180 degree angle.
LCDON With a "1" (high level) the driver circuits for the LCD data and control bus are turned on.
LCDPWR Setting this bit turns on the supply voltage for the TFT display.

Control register 4 controls the external supply voltage for MultiMedia Card #1 of the phyCORE-PXA270.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 4 RW	0x04000008	Res R/W=0	Res R/W=0	Res R/W=0	Res R/W=0	MMC1PWR R/W
Signal Name						/MMC1_3V

Table 12: PLD U7 Control Register 4

MMC1PWR Setting this bit turns on the supply voltage for MMC card #1.

Control register 5 is reserved for MultiMedia Card #2. Here the supply voltage can be switched on and the access LED can be activated. The register bits WP and DET return the card status.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 5 RW	0x0400000A	Res R/W=0	WP R	DET R	LED R/W	MMC2PWR R/W
Signal Name			MMC_WP2	MMC_DET2	xMMC_LED	/MMC2_3V

Table 13: PLD U7 Control Register 5

MMC2PWR Setting this bit turns on the supply voltage for the MMC card 2.

LED Setting this bit turns on the access indication LED for then MMC card on the Expansion Board.

DET If an MMC card is inserted in the socket then reading this bit returns "0", otherwise it is "1".

WP If a MMC card is inserted in the socket that is write protected then reading this bit returns a "0", otherwise it is set to "1".

Control registers 6 and 7 contain the interrupt sources for the controller's interrupt input GPIO_9. In control register 6 the register bits are cleared when one of the external interrupt sources becomes active. If one of the 4 bits in this register is 0, then a high-active interrupt is generated on GPIO_9. The value 0xFF has to be written to this control register after the interrupt has been serviced in order to allow new interrupts to occur. The interrupt control register 7 is used to mask individual interrupt inputs. Only if the corresponding bit is set to 1, an external interrupt will clear the bit in control register 6. The interrupt sources correspond to the bit name in control register 7.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 6	0x0400000C	Res	INT3	INT2	INT1	INT0
RW		R/W=0	R/W	R/W	R/W	R/W
CTRL 7	0x0400000E	Res	INT PM_5V	INT MMCDET	INT FF_RI	INT BT_DET
RW		R/W=0	R/W	R/W	R/W	R/W
Signal Name			5V_OFF	MMC_DET 2	FF_RI_DETECT	BT_RXD_DETECT

Table 14: PLD U7 Control Registers 6 and 7

INT0 IRQ status bit for BT-UART detect
INT1 IRQ status bit for FF-UART detect
INT2 IRQ status bit for MMC-Card 2 detect
INT3 IRQ status bit for 5 V power not present

Clear bit = interrrupt active if one of the four bits = 0 => /INT0-BIT

INT_BT_DET Enable bit for BT-UART detect
INT_FF_DET Enable bit for FF-UART detect
INT_MMCDET Enable bit for MMC card 2 detect
INT_PM5V Enable bit for 5 V power not present

Only if the corresponding bit is set to "1", then an interrupt will clear the matching bit in control register 6 and hence release an interrupt.

Control register 8 controls the RS-232 transceiver for the BT/IR UART and the FF-UART.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 8	0x04000010	Res	BT_Rx	FF_RI	BT_SD	FF_SD
RW		R/W=0	R/W	R/W	R/W	R/W
Signal Name			BT_RX_DETECT	FF_RI_DETECT	BT_/SHDN	FF_/SHDN

Table 15: PLD U7 Control Register 8

FF-SD Setting this bit shuts down the RS-232 transceiver for the FF-UART.

BT-SD Setting this bit shuts down the RS-232 transceiver for the BT-UART and IR-UART.

FF_RI If the RS-232 transceiver for the FF-UART is in power down mode then this bit returns an active RI signal.

BT_Rx If the RS-232 transceiver for the BT-UART or IR-UART is in power down mode then this bit returns an active RxD signal.

The Flash device on the phyCORE module and the AC97 expansion interface can be configured in control register 9. If /FL_DIS is set to 0, then it is possible to boot from an external Flash (not the Flash populating the phyCORE-PXA270).

However it is important to be aware of the bus configuration on the phyCORE module. When setting the bit FL_WP the Flash will be write-protected with WP.

AC97ENA is an output that extends to the expansion socket of the AC97 interface. This is provided so that the expansion circuitry supply voltage can be turned off or switched to power down mode. The connections have to be made on the AC97 expansion board. *Refer to section 12 for more details on this AC97 expansion connector.*

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 9	0x04000012	Res	Res	AC97 ENA	/FL_DIS	FL_WP
RW		R/W=0	R/W=0	R/W	R/W	R
Signal Name				/ENA_AC97	FL_DIS	FL_/WP_PEN

Table 16: PLD U7 Control Register 9

FL_WP **NOTE**: When using the J3D Flash type on the phyCORE-PXA270 this signal is hard wired to VCC (logic high). This bit has no function in this case.

FL_DIS This bit can be used to disable the on-board Flash on the phyCORE-PXA270.

AC97_ENA This bit controls an output signal routed to the AC97 expansion connector. It can be used to turn the supply voltage for an AC97 module connected to X24 on or off.

Control register 10 configures the supply voltage and enable pin for the optional GPS module on the Carrier Board.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 10 RW	0x04000014	Res R/W=0	GPS_ENA R/W	GPS_PWR R/W	Res R/W=0	Res R/W=0
Signal Name			IR_GPIO	IR_PWR		

Table 17: PLD U7 Control Register 10

GPS_PWR Setting this bit turns on the supply voltage for the GPS module.

GPS_ENA Setting this bit enables the GPS module.

The optional battery charger circuitry is configured with control register 11.

Note:
The battery charger register is only available with PCB revision 1220.2 and higher.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 11 RW	0x04000016	Res R/W=0	ALARM R	ACPRES R	ACSEL R/W	ACENA R/W
Signal Name			AKKU_ALARM	AKKU_ACPRES	AKKU_ACSEL	AKKU_ENABLE

Table 18: PLD U7 Control Register 11

ACENA Setting this bit turns on the battery charger controller.

ACSEL This bit selects the source of the board's power supply, "1" specifies supply via DC adapter, "0" via battery.

ACPRES Reading a "1" from this input indicates that a DC adapter is currently connected to the board.

ALARM This bit returns the alarm status information of the battery charger controller.

5.2.2 External Data and Address Bus

The data and address bus on the phyCORE-PXA270 operates with a clock frequency of 100 MHz, therefore it must be decoupled for external use. All components on the Carrier Board except the Control PLD are connected to the decoupled data and address bus. The driver ICs are controlled by the PLD at U7 depending on the state of the corresponding Chip Select signal.

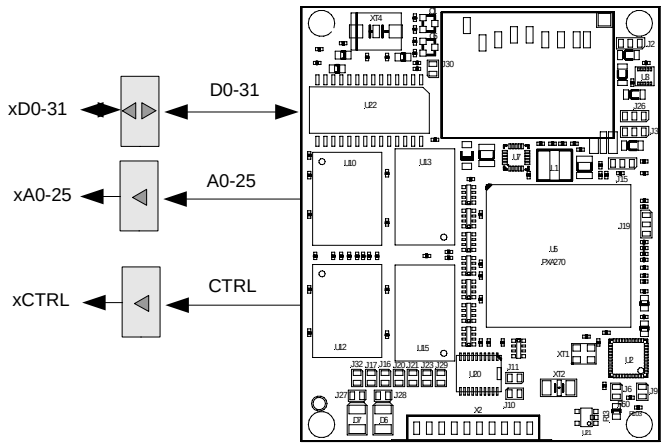


Figure 13: Decoupling the Data and Address Bus

5.3 IDE Interface and CF Card PLD (U6)

The phyCORE-PXA270 provides a PCMCIA interface that supports two independent PCMCIA sockets. The first socket is available on the Carrier Board as an IDE interface, the second interface extends as a CF card socket to the Expansion Board. PLD U6 is provided for controlling the additional functions such as TrueIDE mode, power and others.

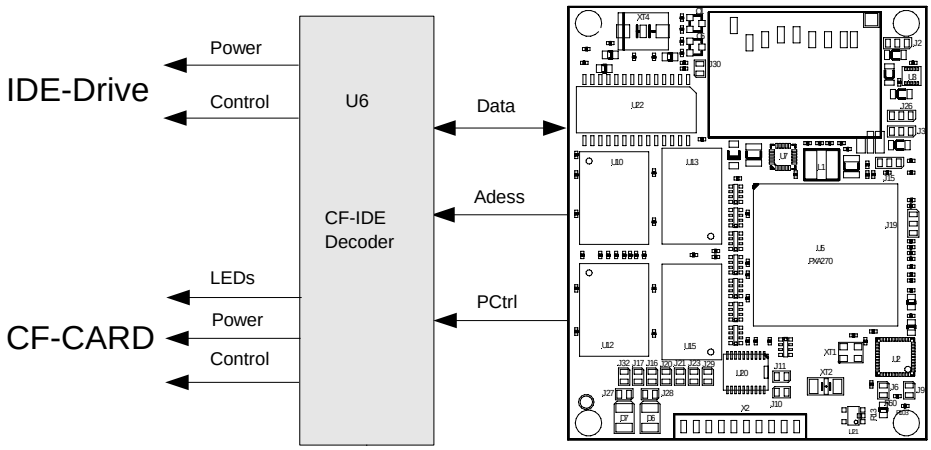


Figure 14: CF Card and IDE Control PLD U6

5.3.1 IDE Interface

The PXA270 controller's first PCMCIA interface is used on the Carrier Board to realize an IDE socket for 2.5" hard drives. PLD U6 provides all the control logic to operate the IDE interface. The 2.0 mm header connector is located at X20 on the Carrier Board. Mounting holes for attaching the hard drive are located on the Carrier Board as well. The hard disk will be attached to the board using spacers on top of the phyCORE-PXA270 module *(refer to Figure 15 for details)*.

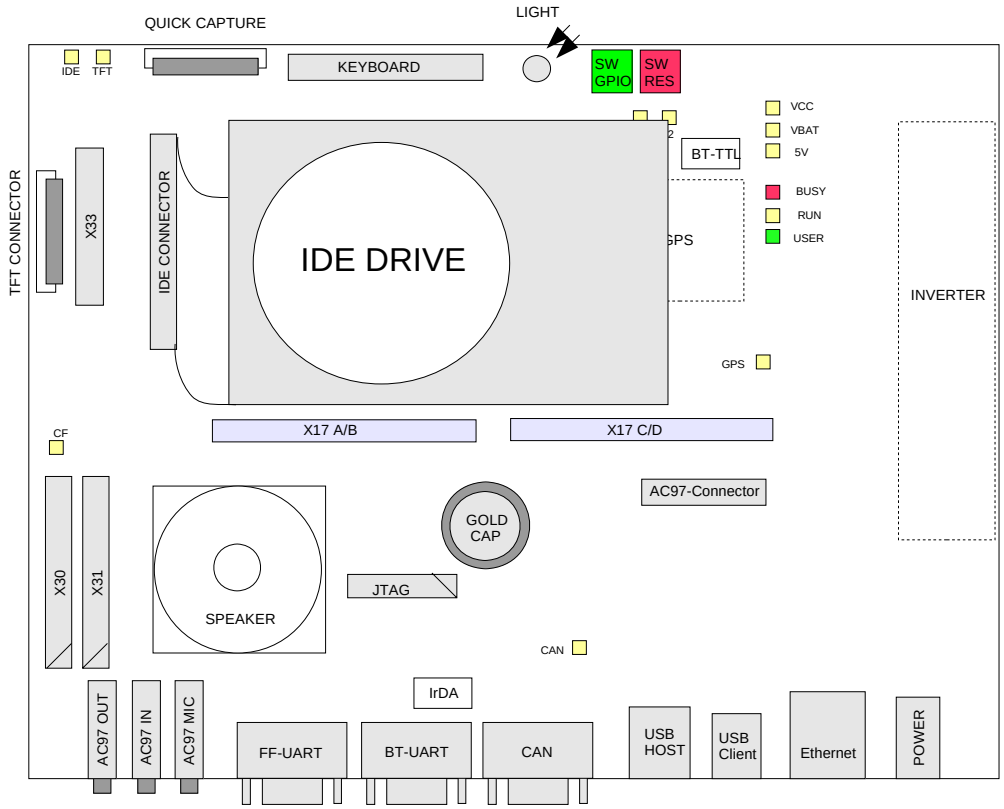


Figure 15: IDE Hard Drive Mounting Location

The hard drive, running at 5 V, is decoupled from the buffered data and address bus on the Carrier Board via 74LVC245 line driver ICs.

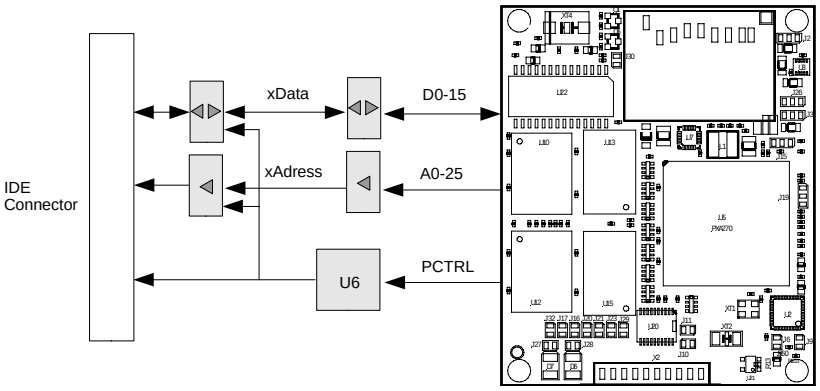


Figure 16: IDE Circuitry

The PCMCIA interface settings are made in the PXA270 controller. The IDE registers within PLD U6 along with their reset values are given in the following table.

REG	ADDR	D7	D3	D2	D1	D0
IDE 0	0x20001000	Res	Res	PM_5V	RES	RES
Reset			0	X	0	0
IDE 1	0x20001002	Res	DMA0/1	DMAEN	RES	IDE/MEM
Reset			0	0	0	1
IDE 2	0x20001004	Res	RDY	Res	IDE_RES	RES
Reset			0	0	0	1
IDE 3	0x20001006	Res	Res	IDEIN	IDEON	IDEOE
Reset			0	0	0	0
IDE 4	0x20001008	Res	IDE5V	RES	5V/3V	IDEPWR
Reset			x	0	1	0

Table 19: IDE Control Register with Reset Values

The operating states of the 5 V supply voltage can be read in the IDE control register 0. If the Carrier Board's input voltage drops below 8 V, the 5 V supply voltage will be shut off.

REG	ADDR	D7	D3	D2	D1	D0
IDE 0	0x20001000	Res	Res	PM_5V	RES	RES
RW		R/W=0	R/W=0	R	R/W=0	R/W=0
Signal Name				PM_5V		

Table 20: IDE Control Register 0

PM_5V Reading a "1" from this bit indicates that the 5 V system supply voltage as well as the LCD voltatge are active.

IDE control register 1 is used to set the memory interface and the DMA access. Since a hard drive only supports the TruIDE mode of a CF card interface, this has a fixed setting in register bit 0. The PXA270 controller's PCMCIA interface does not support TrueIDE mode. Therefore the /IDE_PCE1 signal is activated with A11='0' and the /IDE_PCE2 signal is activated with A11='1'. Both signals are active during 8-bit as well as 16-bit accesses. As an option the IDE interface can also run in DMA mode. The DMA mode is activated by setting bit DMAENA. The free DMA channel can be selected in register DMA0/1. The DACK signal is generated if A21=1 and A13=0.

REG	ADDR	D7	D3	D2	D1	D0
IDE 1	0x20001002	Res	DMA0	DMAEN	RES	IDE/MEM
RW		R/W=0	R=0/W=0	R/W	R/W=0	R=1/W=1
Signal Name			XDREQ_0	xIDE_DREQ		internal

Table 21: IDE Control Register 1

IDE/MEM Setting this bit to "1" selects the TrueIDE mode. In this mode address line A11 is used to switch the PCE1 and PCE2 memory areas. It is not possible to use the memory mode.

DMAEN This bit enables the optional DMA mode.

DMA0 This bit configures the available DMA channel (only channel 0 is possible in conjunction phyCORE-PXA270).

IDE control register 2 includes the control signals for reset and ready. The hard drive reset can be controlled via software. Bit 1 of the IDE control register 2 will generate a reset if set to "0" while setting this bit to "1" will end the reset cycle. Reading bit 3 returns the status of the hard drive's RDY signal.

REG	ADDR	D7	D3	D2	D1	D0
IDE 2	0x20001004	Res	RDY	Res	IDE_RES	RES
RW		R/W=0	R	R/W=0	R/W=0	R=1
			xIDE_RDY		x/IDE_RES	

Table 22: IDE Control Register 2

IDE_RES High active reset signal for the hard drive.

/RDY Shows current state of the hard drive's ready signal.

The IDE interface is separated from the data, address and control bus by line driver circuits. The drivers for the data bus can be activated with the signal IDEOE. IDEON activates the drivers for the address and control signal outputs and IDEIN activates the drivers for the input signals such as IRQ.

REG	ADDR	D7	D3	D2	D1	D0
IDE 3	0x20001006	Res	Res	IDEIN	IDEON	IDEOE
RW		R/W=0	R/W=0	R/W	R/W	R/W
Signal Name				x/IDE_IN	X/IDE_ON	x/IDE_OE

Table 23: IDE Control Register 3

IDEOE Setting this bit turns on the data bus line drivers.

IDEON Setting this bit turns on the control and address lines.

IDEIN Setting this bit turns on the input signals.

The IDE control register 4 is responsible for the supply voltage to the IDE hard drive. The register bit 5 V/3 V is always set to 1 because the hard drive runs with 5 V. If IDEPWR is set, then the 5 V supply is connected to the hard drive. The IDE5V bit is set in response.

REG	ADDR	D7	D3	D2	D1	D0
IDE 4	0x20001008	Res	IDE5V	RES	5V/3V	IDEPWR
RW		R/W=0	R	R/W=0	R=1/W=1	R/W
Signal Name			Internal		internal	/IDE_5V

Table 24: IDE Control Register 4

IDEPWR Setting this bit turns on the 5 V supply voltage for the IDE drive.

3V/5V This bit will always retunr a "1" because only a 5 V supply voltage is permissible.

IDE5V Indicates that the 5 V supply voltage has been turned on.

The PXA270 PCMCIA interface does not support TrueIDE mode. When operating in TrueIDE mode signals /IDE_PCE1 and /IDE_PCE2 don't control the LowByte and HighByte but two different memory areas. LowByte or HighByte are selected via address line A0 in TrueIDE mode. PLD U6 allows access to the two separate memory areas (control register 1 - bit 0 = 1) by using address line A11 in order to decide which of the two Chip Select signals is active.

A11	**/IDE_PCE1 and /IDE_PCE2 Level**
0	/IDE_PCE1 = active, /IDE_PCE2 = not active
1	/IDE_PCE2 = active, /IDE_PCE1 = not active

Table 25: TrueIDE Memory Area Assignment

Based on the above assignment scheme the following memory areas are used in conjunction with the physical address range of the PXA270 controller. It should be noted that operating systems, such as Linux and WinCE, use virtual addresses. This means that physical addresses can also be mapped to other memory areas.

Active Address Range	**Corresponding Chip Select Signal**
0x2000 0000	/IDE_PCE1
0x2000 0800	/IDE_PCE2

Table 26: Physical Address Range of the IDE Interface

For more information refer to the applicable IDE data sheet.

5.3.2 Compact Flash Interface

The PXA270 controller supports two PCMCIA interfaces. The second interface is used on the Carrier Board as a CompactFlash socket. PLD U6 provides all the control logic to operate the CompactFlash interface. The connector is located on the corresponding Expansion Board.

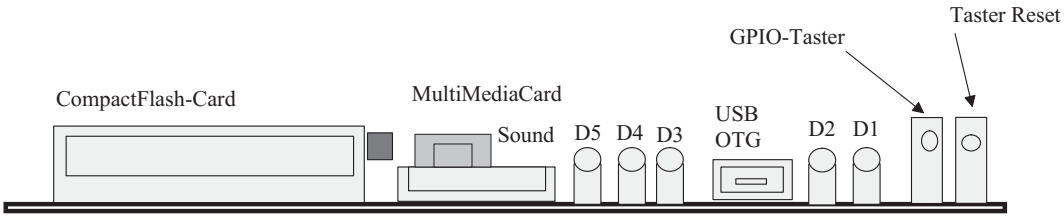


Figure 17: Compact Flash Interface on the Expansion Board

The CompactFlash card is operated in TrueIDE mode. The interface is decoupled from the buffered data and address bus on the Carrier Board via 74LVC245 line driver ICs.

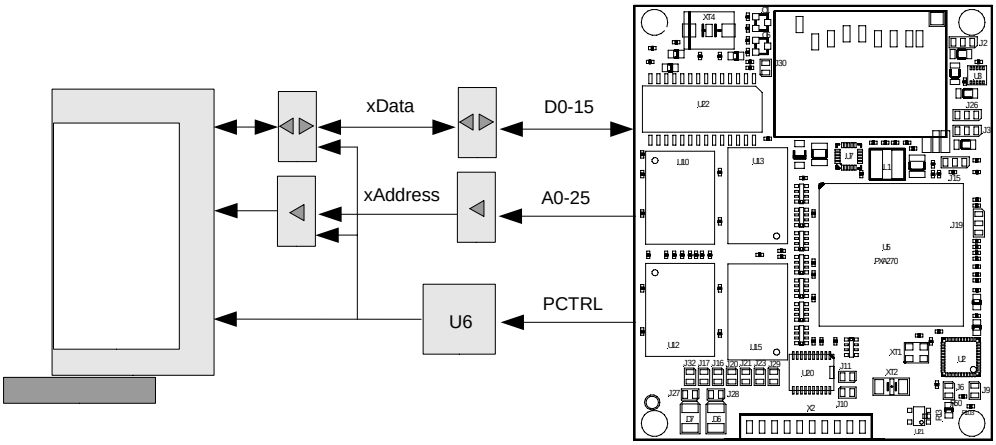


Figure 18: Compact Flash Circuitry

The settings for the PCMCIA interface are made in the PXA270 controller. The CF card registers of the PLD U6 along with their reset values are given in the following table.

REG	ADDR	D7	D3	D2	D1	D0
CF0	0x30001000	Res	Res	PM_5V	Res	LED
Reset			0	X	0	0
CF1	0x30001002	Res	Res	Res	Res	IDE/MEM
Reset			0	0	0	0
CF2	0x30001004	Res	RDY	RDYEN	RES_CF	RESEN
Reset			0	0	0	1
CF3	0x30001006	Res	CFCD	IDEIN	IDEON	IDEOE
Reset			0	0	0	0
CF4	0x30001008	Res	CF5V	CF3V	5V/3V	CFPWR
Reset			0	0	0	0
CF5	0x3000100A	Res	/VS2	/VS1	/BVD2	/BVD1
Reset			X	X	X	X
CF6	0x3000100C	Res	WP	Res	/CD2	/CD1
Reset			X	X	X	X

Table 27: CF Card Control Register with Reset Values

The operating states of the 5 V supply voltages can be read in the CF control register 0. If the Carrier Board's input voltage drops below 8 V, the 5 V supply voltage will be shut off. The CF LED is located at register bit 0. The LED is switched on by setting the bit and can be used as an access display for the CF card socket.

REG	ADDR	D7	D3	D2	D1	D0
CF0	0x30001000	Res	Res	PM_5V	Res	LED
RW			R/W=0	R	R/W=0	RW
Signal Name				PM_5V		x/CF_LED

Table 28: CF Card Control Register 0

LED Controls the CF card access LED.

PM_5V This bit indicates that the 5 V supply voltage is active.

CF control register 1 is used to set the memory interface. The CF card interface can operate in TruIDE mode if the register bit is set to 0. The PXA270 controller's PCMCIA interface does not support TruIDE mode. Therefore the /CF_PCE1 signal is linked with A11='0' and the /CF_PCE2 signal is linked with A11='1'. Both signals are active during 8-bit as well as 16-bit accesses. If register bit 0 is set to '0' then the memory mode of the CF card is configured. This memory interface is supported directly by the PXA270.

REG	ADDR	D7	D3	D2	D1	D0
CF1	0x30001002	Res	Res	Res	Res	IDE/MEM
RW		R/W=0	R/W=0	R/W=0	R/W=0	R=1/W=1
Signal Name						internal

Table 29: CF Card Control Register 1

IDE/MEM Setting this bit to "1" turns on the TrueIDE mode, writing a "0" selects the memory mode.

The CF card settings for reset and RDY are made in CF control register 2. With RESENA the reset can be activated. RDYENA connects the RDY signal of the CF card to the controller signal PWAIT. The RDY signal can be read on the RDY bit.

REG	ADDR	D7	D3	D2	D1	D0
CF2	0x30001004	Res	RDY	RDYENA	RES_CF	RESENA
RW		R/W=0	R/W	R/W	R/W	R=1
Signal Name			xCF_RDY	internal	X/CF_RESET	internal

Table 30: CF Card Control Register 2

RESENA Enables CF card reset (bit is always "1").
RES_CF Activates the CF card reset.
RDYEN Connects the RDY input with PWAIT.
RDY Returns the state of the RDY signal.

The CF interface is separated from the data, address and control bus by line driver circuits. The drivers for the data bus can be activated with the signal CFOE. CFON activates the drivers for the address and control signal outputs and CFIN activates the drivers for the input signals such as IRQ.

REG	ADDR	D7	D3	D2	D1	D0
CF3	0x30001006	Res	CFCD	CFIN	CFON	CFOE
RW		R/W=0	R/W	R/W	R/W	R/W
Signal Name			x/CF_CD	x/CF_IN	x/CF_ON	x/CF_OE

Table 31: CF Card Control Register 3

CFOE Turns on the data bus line driver.
CFON Turns on the address bus and contol line driver.
CFIN Turns on the line driver for input signals.
CFCD Turns on the line driver with the CF card control output signals such as CD1/2 etc.

CF control register 4 configures the supply voltage for the CF card interface. The register bit 5 V/3 V is used to configure the CF card voltage. If the bit is set to "1" the CF card is supplied with 5 V, if the bit is set to '0' then the CF card is supplied with 3.3 V. If CFPWR is set then the configured voltage (5 V or 3.3 V) is connected to the CF card. In response the CF5V bit will be set for a 5 V supply voltage or CF3V if a 3.3 V supply is used.

REG	ADDR	D7	D3	D2	D1	D0
CF4	0x30001008	Res	CF5V	CF3V	5V/3V	CFPWR
RW		R/W=0	R	R	R/W	R/W
Signal Name			internal	internal	xCF_5V xCF_3V	xCF_5V xCF_3V

Table 32: CF Card Control Register 4

CFPWR Turns on the selected CF card voltage.
5V/3V Selects the CF card voltage; 1 = 5 V, 0 = 3.3 V
CF3V Indicates 3.3 V supply active.
CF5V Indicates 5 V supply active.

Control register 5 displays the CF card signals /VS1, /VS2, /BVD1 and /BVD2. /VS1 and /VS2 should be read in order to set the correct CF card supply voltage in CF card control register 4.

REG	ADDR	D7	D3	D2	D1	D0
CF5	0x3000100A	Res	/VS2	/VS1	/BVD2	/BVD1
RW		R/W=0	R	R	R	R
Signal Name			x/CF_VS2	x/CF_VS1	x/CF_BVD2	x/CF_BVD1

Table 33: CF Card Control Register 5

/BVD1 Returns the CF card /BVD1 signal.
/BVD2 Returns the CF card /BVD2 signal.
/VS1 Returns the CF card /VS1 signal.
/VS2 Returns the CF card /VS2 signal.

The CF card CD signals can be read via control register 6. If a CR card is inserted correctly in the socket both signals should read back the value "0".

REG	ADDR	D7	D3	D2	D1	D0
CF6	0x3000100C	Res	WP	Res	/CD2	/CD1
RW		R/W=0	R/W=0	R/W=0	R	R
Signal Name					x/CF_CD2	x/CF_CD1

Table 34: CF Card Control Register 6

/CD1 Returns the Card Detect1 signal, active low.
/CD2 Returns the Card Detect2 signal, active low.

6 Ethernet Interface

The Ethernet interface of the phyCORE-PXA270 is supplemented on the Carrier Board by the Ethernet transformer and the RJ45 connector.

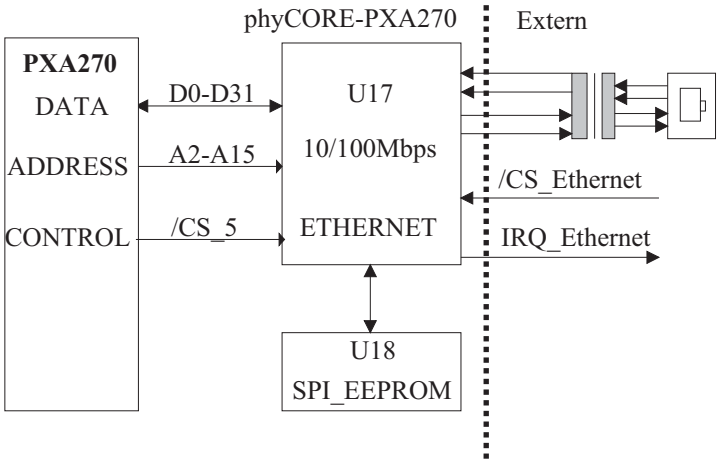


Figure 19: Ethernet Circuitry

The Ethernet interface is accessible on the RJ45 socket at X23. The yellow LED extends to the /LAN_LED_A signal and the green LED extends to /LAN_LED_B. The organization of the LED functions is freely programmable in the LAN91C111 Ethernet chip and is therefore operating system dependent.

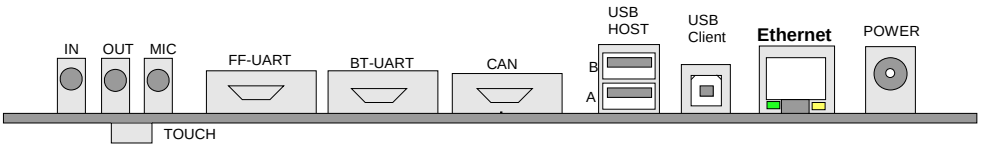


Figure 20: Location of the Ethernet Socket

The Ethernet chip's physical memory area is given in the following table. The address decoder generates the Ethernet /CS at address 0x14000000. In addition an offset of 0x00000300 has to be added.

Ethernet	**Start Address**
/CS_ETH + OFFSET	0x 1400 0000 + 0x 0000 0300 = 0x 1400 0300

Table 35: Address Space for Ethernet Controller

7 USB Host

The PXA270 controller lacks support of controlling input devices such as keyboard or mouse. The PXA270 on-chip USB host controller supports one USB host interface which can also function as an OTG interface. On the Carrier Board the USB host interfaces are connected to a double USB host socket. Note that socked B is inactiv and must **not** be used in conjunction with the phyCORE-PXA270 given the fact that only one USB host is available. Since the USB host interface can also operate in OTG mode it is connected to the OTG socket on the Expansion Board as well.

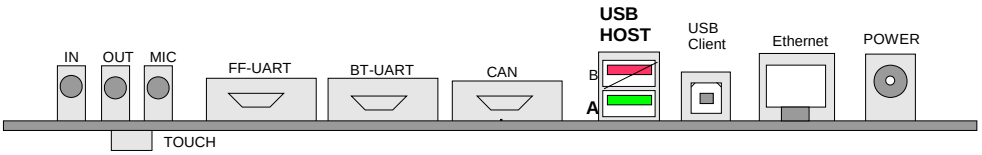


Figure 21: USB Host Connector

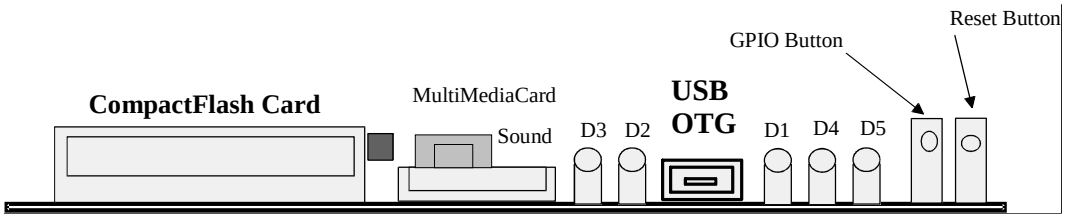


Figure 22: Location of the USB OTG Socket

The following table gives an overview of jumpers relevant for configuring the USB interface:

Jumper	Default	Comment
JP3		This jumper configures the USB controller OTG ID input. *Refer to PXA270 controller data sheet and user's manual for details.*
1 + 2	-	OTG ID = 10 kOhm pull-up,for external OTG ID signal
2 + 3	X	OTG ID tied to Ground.
JP5		This jumper should not be changed.
1 + 2	X	OTG_5V connected to 3.3 V
2 + 3		Must not be used!
JP6		This jumper configures the routing of the first USB channel supply voltage. *Refer to PXA270 controller data sheet and user's manual for details.*
1 + 2	-	USB 5 V routed to OTG interface on expansion board.
2 + 3	X	USB 5V routed to USB host interface on Carrier Board.
JP9		This jumper should not be changed.
1 + 2	-	Must not be used!
2 + 3	X	OTG_VBUS open

Table 36: USB Host Jumpers

Due to the lack of a second USB host interface on the phyCORE-PXA270 solder jumpers J33 and J34 on the Carrier Board are not populated.

8 USB Client

The PXA270 controller is equipped with a USB client interface for communication with a PC. The interface extends to the USB client socket X22 on the Carrier Board.

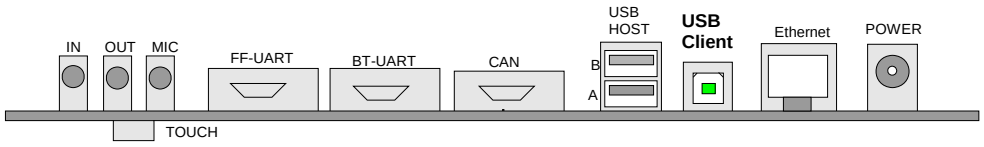


Figure 23: USB Client Connector

9 LCD Interface

There is an active TFT-LCD interface on the Carrier Board for controlling displays with 18-bit color depth (6 each for red, green and blue). The LCD signals are decoupled from the PXA270 controller with 74LVC254 line driver circuits. The controller supports 18-bit and 16-bit color information. The circuitry on the Carrier Board only uses 16-bit color information. The least significant bits for decoding the blue and red color signal are connected to GND.

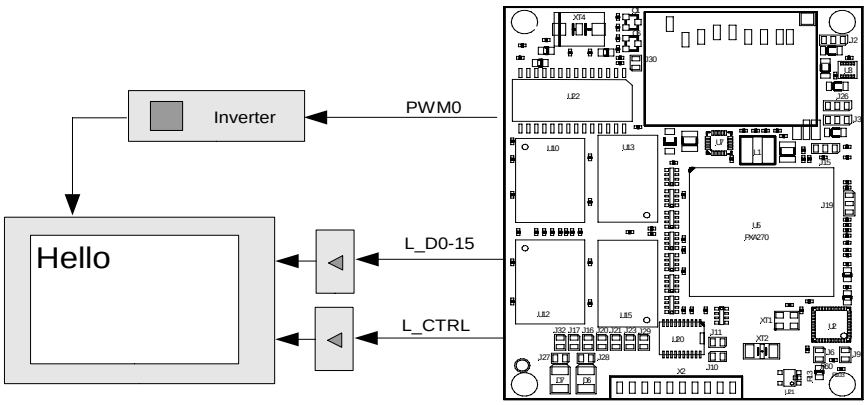


Figure 24: Active TFT LCD Connection

The Sharp display used on the Carrier Board offers the possibility of adjusting the display size and position via two inputs. The control PLD U7 enables configuration of these inputs over internal registers.

A TFT display can be connected to the Carrier Board with the help of a 33-pin ribbon cable at header connector X35. An LCD-001 adapter board is necessary when using the Sharp TFT display in order to convert the Hirose connector plug to a ribbon cable connector plug. Furthermore, there is a 2.0 mm universal connector plug on the board at X33, where other display types can be adapted to the PXA270's LCD port.

Jumper	Default	Comment
J8		LCD position 3 signal at connector X35
1 + 2	X	LCD_POS3 = VCC
2 + 3		LCD_POS3 = GND
J13		This jumper configures the input voltage for LCDVCC.
1 + 2	-	LCDVCC connect with VCC_5VLCD power supply
2 + 3	X	LCDVCC connect with VCC_5V power supply
J20		This jumper is note used.
1 + 2	-	Leave unconnected.
2 + 3		Leave unconnected.
J23		This jumper configures the inverter enable input which can be used to control the LCD brightness.
1 + 2	X	Inverter is controlled by the PWM0 signal from PXA270.
2 + 3		Inverter is always on.
J24		This jumper should not be changed.
1 + 2	X	Signal always tied to GND.
2 + 3		Note used.

Table 37: LCD Jumpers

Signal		A	B		Signal
GND		**1**	**1**		PCLK
GND		**2**	**2**		LCLK
GND		**3**	**3**		FCLK
GND		**4**	**4**		R0
R1		**5**	**5**		R2
R3		**6**	**6**		R4
R5		**7**	**7**		GND
G0		**8**	**8**		G1
G2		**9**	**9**		G3
G4		**10**	**10**		G5
GND		**11**	**11**		B0
B1		**12**	**12**		B2
B3		**13**	**13**		B4
B5		**14**	**14**		GND
LCD_ENAB		**15**	**15**		3.3V VCC
3.3 V VCC		**16**	**16**		LCD_POS1
LCD_POS2		**17**	**17**		LCD_POS3

Table 38: LCD Connector at X33

The supply voltage for the TFT display and the inverter can be turned on with the help of a register in control PLD U7. The brightness of the background illumination can be set using the controller's PWM0 signal. The inverter is located on the Carrier Board near the LCD inverter cable.

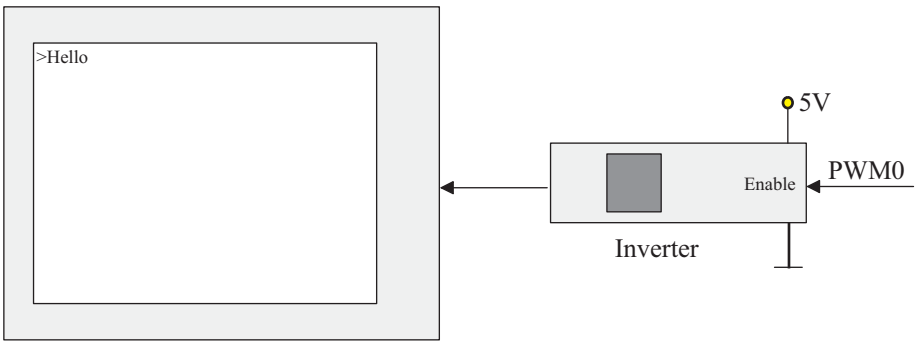


Figure 25: LCD Inverter Circuitry

10 RS-232 Interface

The PXA270 controller has four internal UARTS. Three of these are supported in the current version of the phyCORE-PXA270. Two of the interfaces are accessible in the standard RS-232 level over DB-9 sockets at P1 (FF-UART) and P2 (BT-UART).

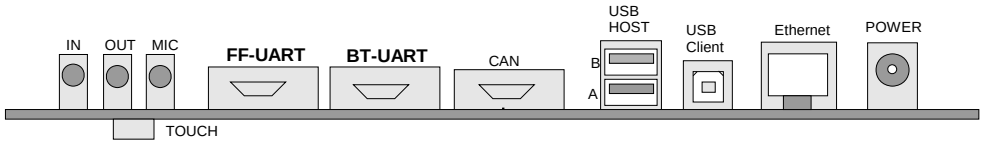


Figure 26: RS-232 Connectors (FF-UART, BT-UART)

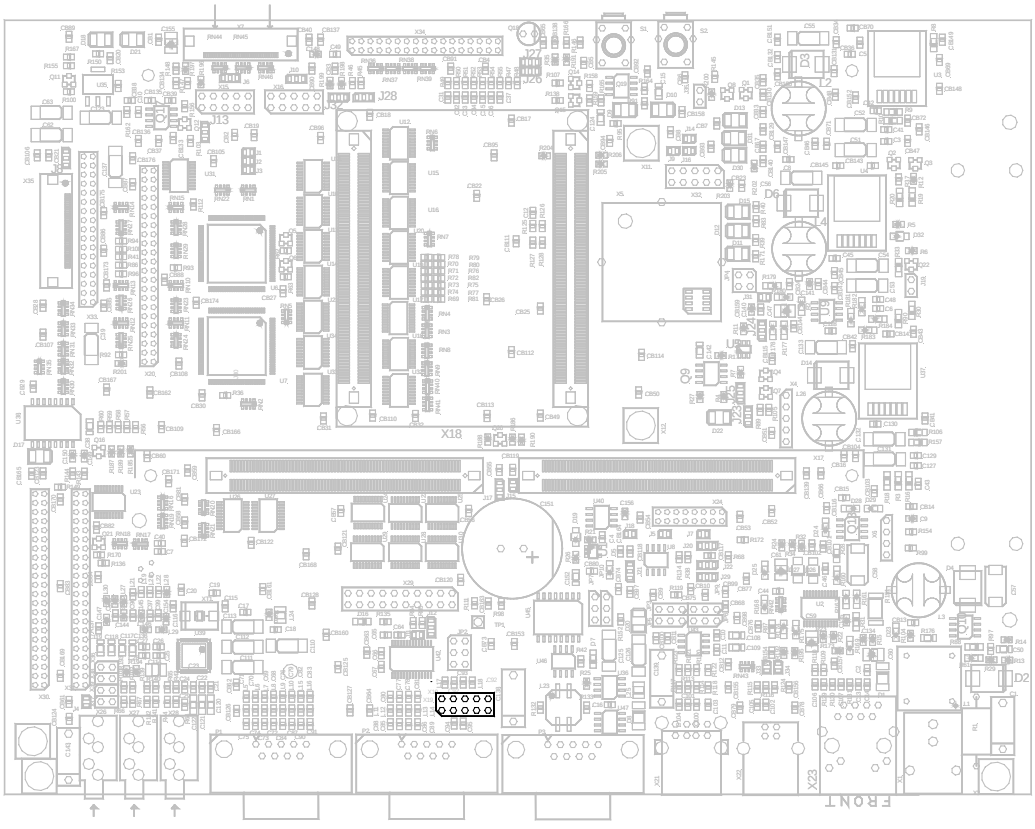
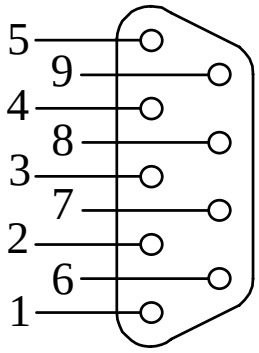


Figure 27: IR-UART Connector

10.1 FF-UART

The FF-UART (**F**ull **F**eature UART) is a UART with all modem and control signals and a maximum transfer rate of 921.5 kBaud. This interface is used on the phyCORE-PXA270 for communication with the host-PC. The RS-232 transceiver device is located on the phyCORE module at U1. The RS-232 transceiver is configured for auto shutdown, which means that the driver shuts off automatically after a few seconds in order to conserve power. The RS-232 transceiver can be made inactive over the PowerLatch (data bit D1). The interface extends to socket P1 on the Carrier Board.

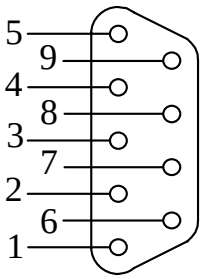


Pin 5:	GND
Pin 9:	FF_RI
Pin 4:	FF_DTR
Pin 8:	FF_CTS
Pin 3:	FF_TxD
Pin 7:	FF_RTS
Pin 2:	FF_RxD
Pin 6:	FF_DSR
Pin 1:	FF_DCD

Figure 28: P1 Pin Assignment, FF-UART

10.2 BT-UART

The BT-UART has the same properties as the FF-UART, however only the signals BT_RxD, BT_TxD, BT_CTS and BT_RTS are supported. The TTL signals RxD and CTS can be separated from the RS-232 transceiver at U42 with Jumper JP2 removed from pins 3+4 and 5+6. The RS-232 transceiver for the BT-UART is located on the Carrier Board.



Pin 5: GND
Pin 9: N.C.
Pin 4: N.C.
Pin 8: BT_CTS
Pin 3: BT_TxD
Pin 7: BT_RTS
Pin 2: BT_RxD
Pin 6: N.C.
Pin 1: N.C.

Figure 29: P2 Pin Assignment, BT-UART

Jumper	Default	Comment
JP2		This jumper connects the BT-UART to the RS-232 transceiver.
1 + 2	-	*IR_RxD connected to RS-232 transceiver.*
3 + 4	closed	BT_RxD connected to RS-232 transceiver.
5 + 6	closed	BT_CTS connected to RS-232 transceiver.

Table 39: BT-UART Jumper Configuration

10.3 IR-UART

The IR-UART has the same properties as the FF-UART, however only the signals IR_RxD and IR_TxD are supported. The TTL level signal RxD can be separated from the RS-232 transceiver U42 with Jumper JP2 removed from position 1+2. The RS-232 transceiver for the IR-UART is located on the Carrier Board. The IR-UART extends to a 10-pin header connector at X19, to which an optional flat band cable with a DB 9 socket can be connected.

Signal		A	B		Signal
n.c.		**1**	**1**		n.c.
STD_RxD		**2**	**2**		n.c.
STD_TxD		**3**	**3**		n.c.
n.c.		**4**	**4**		n.c.
GND		**5**	**5**		VCC via J20

Table 40: IR-UART Connector at X19

Jumper	Default	Comment
JP2		This jumper connects the IR-UART's RxD signal to the RS-232 transceiver.
1 + 2	Closed	IR_RxD connected to RS-232 transceiver.
3 + 4	-	*BT_RxD connected to RS-232 transceiver.*
5 + 6	-	*BT_CTS connected to RS-232 transceiver.*

Table 41: IR-UART Jumper Configuration

Jumper JP4 can be used to connect an optional GPS module with the IrDA UART (TTL level) of the PXA270. Make sure Jumper JP2 position 1+2 remains open.

Jumper	Default	Comment
JP4		This jumper connects the IR-UART to the GPS module.
1 + 2	closed	IR_RxD connected to GPS module
3 + 4	closed-	IR_TxD connected to GPS module

Table 42: GPS Module Jumper Configuration

Jumper	Default	Comment
JP2		This jumper connects the IR-UART to the RS-232 transceiver.
1 + 2	open	IR_RxD connected to RS-232 transceiver.
3 + 4	-	*BT_RxD connected to RS-232 transceiver.*
5 + 6	-	*BT_CTS connected to RS-232 transceiver.*

Table 43: IR-UART Jumper Configuration for GPS Modul

11 CAN Interface

An industry-standard CAN interface is populated on the PXA270 Carrier Board for integration into networked machines and systems. The CAN controller (SJA1000) is located on the phyCORE module.

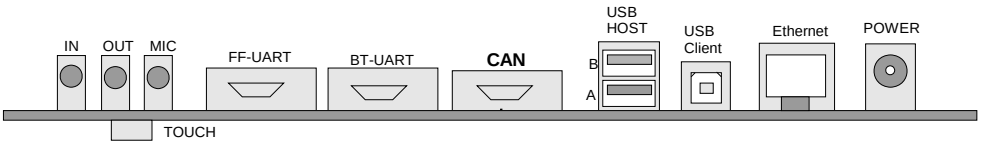


Figure 30: CAN Connector

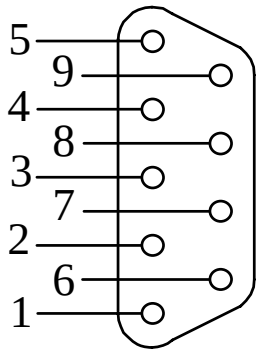
The signals CAN-RxD and CAN-TxD are optically isolated from the phyCORE module over an ADU1402 opto-coupler (U45) and are converted to CANH and CANL using an 82C251 CAN transceiver (U46). A switching voltage regulator converts the exernal CAN supply voltage in a range from 8 – 24 V to a 5 V/0.5 A CANVCC. This enables galvanic separation of the CAN circuitry from the potential of the Carrier Board. Jumpers JP7 and JP10 must be closed at position 2+3 in order to support galvanic separation, when closed at position 1+2 the CAN interface is powered by the internal 5 V supply from the Carrier Board.

Jumper	Default	Comment
JP7		This jumper configures the CAN circuitry supply voltage.
1 + 2	X	CAN supply voltage derived from on-board supply voltage
2 + 3	-	CAN supply voltage from external source for optical isolation
JP10		This jumper configures the CAN circuitry supply voltage.
1 + 2	X	CAN Ground from external source for optical isolation.
2 + 3	-	CAN Ground connected to on-board Ground potential.

Table 44: CAN Interface Jumper Configuration

Note:
Support of the external CAN supply voltage is only available with PCB revision 1220.2 or higher.

The following figure depicts the CAN connector pin assignment:



Pin 9: CANV+

Pin 3: CANV-
Pin 7: CAN-H (optically isolated)
Pin 2: CAN-L (optically isolated)
Pin 6: CANV-

Figure 31: CAN Connector P3 Pinout

12 AC97 Interface and Touch Controller

The PXA270 controller feataures an AC97 interface for controlling sound decoders such as the WM9712L from Wolfson. The WM9712L also has an integrated touch controller.

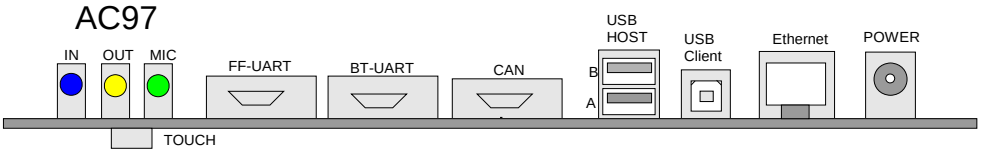


Figure 32: Sound and Touch Controller Interfaces

The sound decoder WM9712L is controlled via the controller's AC97 interface. The SDATA_IN0 is used as the input channel. The second channel (SDATA_IN1) is available on the AC97 expansion socket at X24. Connection to other AC97 devices such as modems is possible via this socket.

Signal		A	B		Signal
VCC (3.3V)		**1**	**2**		VCC (3.3V)
/ENA_AC97		**3**	**4**		/ACRESET
SYNC		**5**	**6**		GND
BITCLK		**7**	**8**		GND
SDATA_OUT		**9**	**10**		GND
SDATA_IN0		**11**	**12**		GND
SDATA_IN1		**13**	**14**		GND
AC_INT		**15**	**16**		GND

Table 45: AC97 Expansion Socket at X24

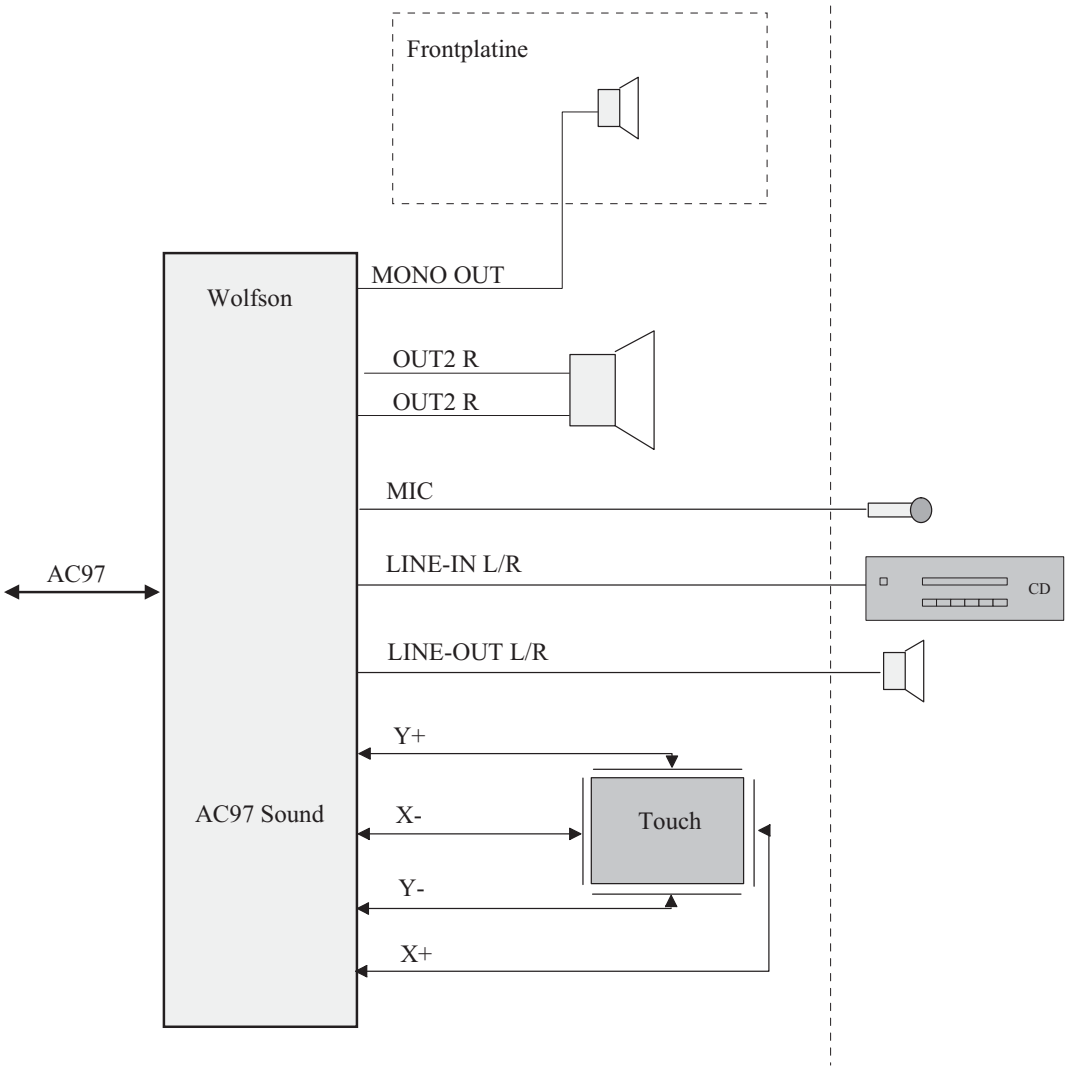


Figure 33: AC97 with WM9712L

The signals from the integrated touch controller are routed to connector X25 on the Carrier Board.

The WM9712L IC also provides four analog inputs that can be used for voltage monitoring purposes.

ADC	**Function**
AUX 0	AKKU_COMP, battery voltage
AUX 1	AKKU_IBAT, battery current draw
AUX 2	AKKU_TEMP, battery temperature
AUX 3	Light sensor

Table 46: Voltage Supervision with WM9712L

The sound portion of the WM9712L supports microphone (mono), stereo input und stereo output.

Sound Jack	**Functions**
X28	Microphone input (mono)
X27	Stereo input
X26	Stereo output

Table 47: Sound Jacks

Another functional block of the WM9712L allows for controlling of loudspeakers. A miniature loudspeaker connected to MonoOut is implemented on the Expansion Board. A larger 0.4 W loudspeaker is located on the Carrier Board at X36 and is connected to signals LOUT2 and ROUT2.

13 Quick Capture Interface

The Quick Capture Interface of the PXA270 controller is supported on the Carrier Board starting with PCB revision 1220.3. This requires use of a special phyCORE-PXA270 module configuration without the MAX7301 or the MAX6957 GPIO Expander chip. A PHYTEC camera module with a KAC-9638 CMOS image sensor can be connected to X7 on the Carrier Board. This monochrome sensor supports 1288*1032 pixels with up to 1024 gray shades. A color sensor version of this camera module is in preparation.

Image data from the sensor can be copied into the frame buffer of the PXA270 via DMA transfer or can be saved into a file.

The camera module connects via 33-pin ZIF connector using a flat band cable. The pinout of the connector is shown in the table below:

Pin #	Signal Name	Description
1	VCC	Power supply
2	VCC	Power supply
3	GND	Ground
4	GND	Ground
5	CAM_MCLK	Clock output
6	GND	Ground
7	CAM_PCLK	Pixel clock input
8	GND	Ground
9	CAM-D0	Data 0
10	CAM-D1	Data 1
11	GND	Ground
12	CAM-D2	Data 2
13	CAM-D3	Data 3
14	GND	Ground
15	CAM-D4	Data 4
16	CAM-D5	Data 5
17	GND	Ground
18	CAM-D6	Data 6
19	CAM-D7	Data 7
20	GND	Ground

Pin #	Signal Name	Description
21	CAM-D8	Data 8
22	CAM-D9	Data 9
23	GND	Ground
24	CAM-LV	Line start
25	CAM-FV	Frame start
26	GND	Ground
27	CAM_GPIO	I²C address config
28	CAM_SCL	SCL Quick Capture
29	CAM_SDA	SDA Quick Capture
30	GND	Ground
31	/CAM_RES	/Reset Quick Capture
32	VCC	Power supply
33	VCC	Power supply

Table 48: Quick Capture Interface Connector

Jumpers J26, J27, J28 and J32 can be used to configure the Quick Capture interface.

Jumper	Default	Comment
J26		This jumper configures CAM_GPIO for address select.
1 + 2	X	CAM_GPIO = GPIO14
2 + 3		CAM_GPIO = High
open		CAM_GPIO = Low
J27		This jumper configures the SDA signal.
1 + 2	X	CAM_SDA = PXA270 SDA
2 + 3	-	CAM_SDA = GPIO19
J28		This jumper configures the SCL signal.
1 + 2	X	CAM_SCL = PXA270 SCL
2 + 3	-	CAM_SCL = GPIO22
J32		This jumper configures the Quick Capture reset signal.
1 + 2	-	Reset comes from Carrier Board
2 + 3	X	Reset comes from GPIO86 (phyCORE-PXA270)

Table 49: Quick Capture Interface Jumpers

14 MultiMedia Card

The second PCMCIA interface of the PXA270 controller is available on the Expansion Board and supports MultiMedia cards. MultiMedia cards are available as memory devices with capacities of 8 to 512 MByte that can be easily removed by the user. Access to the MMC connector is controlled via MMC-CS0.

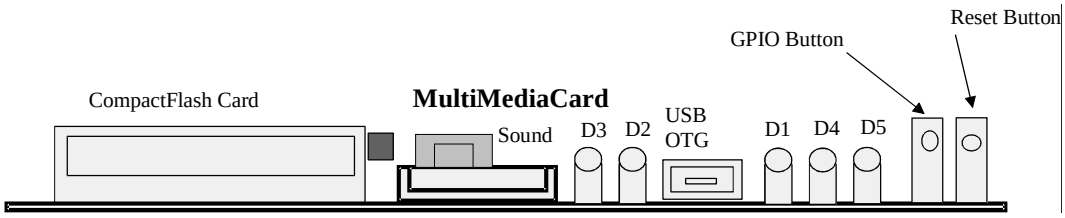


Figure 34: MultiMedia Card

15 Expansion Board

The LCD is mounted on the backside of the Carrier Board to enable easy installation of the Carrier Board inside an enclosure. All important interfaces and sockets that require easy or frequent user access are populated on an Expansion Board. The Expansion Board can be mounted in the housing at a 90° angle to the display, whereby easy access to the MultiMedia Card, CompactFlash Card, USB OTG and push buttons is provided.

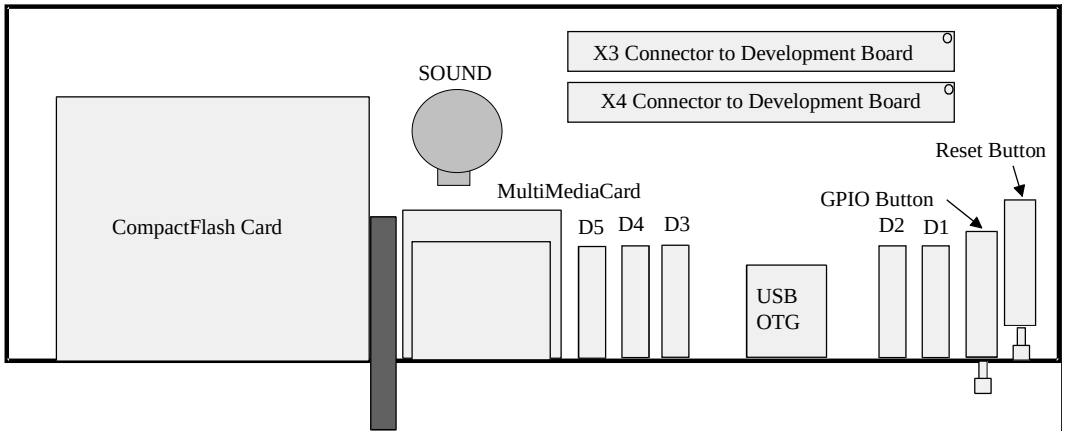


Figure 35: Expansion Board, Top View

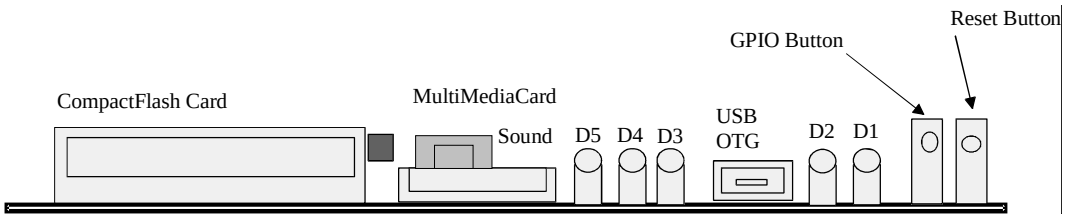


Figure 36: Expansion Board, Side View

The Expansion Board is connected over two 2.0 mm, 44-pin flat band cables. The pinout of the Carrier Board header connectors X30 and X31 is given in the following table. Using a customer-specific Expansion Board instead of the standard Expansion Board is also possible given the removable connection via flat band cables. The connector X30 contains the signals for the CompactFlash card. The voltage pin CF_VCC can only be used for the CF card because it is switched on or off depending on the operating status of the socket.

Signal		X30			Signal
CF_VCC		**1**	**2**		CF_VCC
GND		**3**	**4**		GND
CF_D0		**5**	**6**		CF_D1
CF_D2		**7**	**8**		CF_D3
CF_D4		**9**	**10**		CF_D5
CF_D6		**11**	**12**		CF_D7
GND		**13**	**14**		GND
CF_D8		**15**	**16**		CF_D9
CF_D10		**17**	**18**		CF_D11
CF_D12		**19**	**20**		CF_D13
CF_D14		**21**	**22**		CF_D15
GND		**23**	**24**		GND
CF_A0		**25**	**26**		CF_A4
CF_A1		**27**	**28**		CF_A5
CF_A2		**29**	**30**		CF_A6
CF_A3		**31**	**32**		CF_A7
GND		**33**	**34**		GND
CF_A8		**35**	**36**		/CF_CS1
CF_A9		**37**	**38**		/CF_CS2
CF_A10		**39**	**40**		/CF_WE
/CF_PREG		**41**	**42**		/CF_OE
GND		**43**	**44**		GND

Table 50: Expansion Board Connector X30 Pinout

Connector X31 contains the signals for controlling the CF card, the LEDs, push buttons, USB OTG and MMC. The 3.3 V supply voltage is routed to the Expansion Board at pins 1 and 2.

Signal	X31		Signal
VCC	**1**	**2**	VCC
GND	**3**	**4**	GND
/CF_IORD	**5**	**6**	/CF_CD1
/CF_IOWR	**7**	**8**	/CF_CD2
CF_IRQ	**9**	**10**	/CF_RDY
/CF_RESET	**11**	**12**	/CF_IOIS16
GND	**13**	**14**	GND
OTG_ID	**15**	**16**	/CF_BVD1
OTG_DP1	**17**	**18**	/CF_BVD2
OTG_DM1	**19**	**20**	/CF_LED
OTG_VCC	**21**	**22**	/CF_VS1
GND	**23**	**24**	GND
/CF_VS2	**25**	**26**	/CF_INPACK
/RESIN	**27**	**28**	/OTG_LED
/SW_ON	**29**	**30**	AUDIO_P
/LED_USR	**31**	**32**	AUDIO_N
GND	**33**	**34**	GND
/LED_PWR	**35**	**36**	MMC_WP2
/MMC_LED	**37**	**38**	MMC_CS1
MMCDET2	**39**	**40**	MMC_CLK
MMCDAT	**41**	**42**	MMC_CMD
GND	**43**	**44**	GND

Table 51: Expansion Board Connector X31 Pinout

16 Push Buttons and LEDs

Two push buttons and four LEDs are integrated on the Carrier Board serving as user input and display elements. The corresponding Expansion Board features two additional push buttons and 5 user and status LEDs. Push Button S2 on both the Expansion Board and the Carrier Board serves as a reset button, push button S1 is connected with the GPIO1 (via J15) signal on both boards and can be used freely in the application code. The 4 programmable LEDs are controlled with a low level over PLDs U6 and U7.

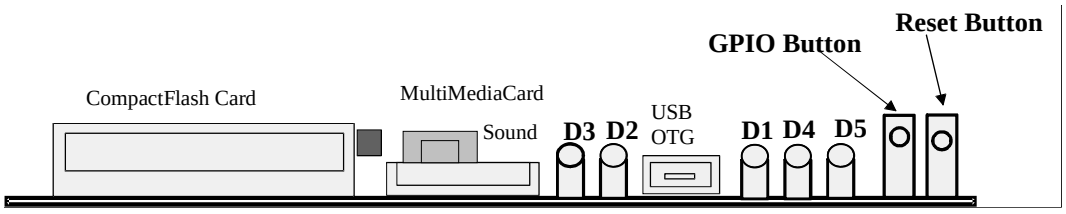


Figure 37: Location of Push Buttons and LEDs (Expansion Board)

LED	Name	Description
D1	*OTG_LED*	*Only in conjunction with phyCORE-PXA255!*
D2	MMC_LED	Bit 1 of control register 5 in PLD U7.
D3	CF_LED	Bit 0 of CF control register 0 in PLD U6.
D4	USER_LED	Bit 1 of control register 2 in PLD U7.
D5	POWER_LED	Bit 0 of control register 2 in PLD U7.

Table 52: Expansion Board LED Functions

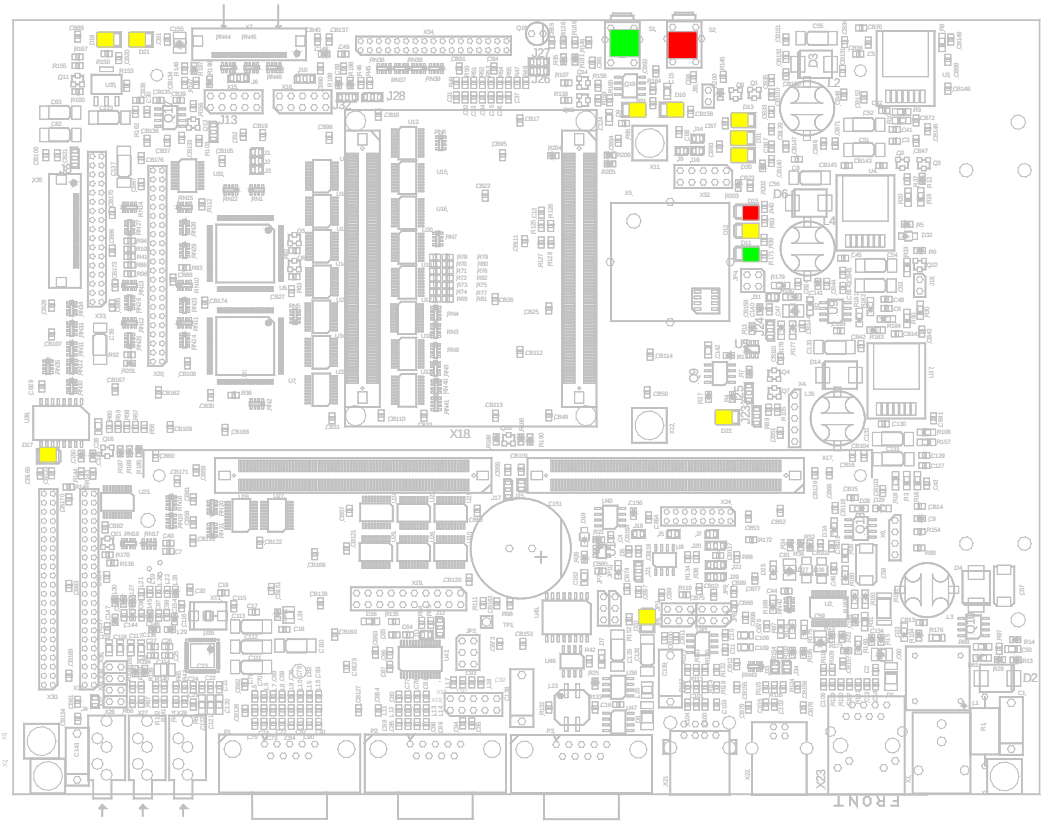


Figure 38: Location of Push Buttons and LEDs (Top View)

17 Matrix Keyboard

The phyCORE-PXA270 features an optional GPIO expander IC which can be used for connecting to a matrix keyboard. The signal lines extend to connector X34 and are arranged in columns and rows. The column outputs have an in-line resistance of 33R and the row inputs have an RC combination with R=1 kOhm against VCC and C = 100 nF against GND to prevent a possible signal bouncing.

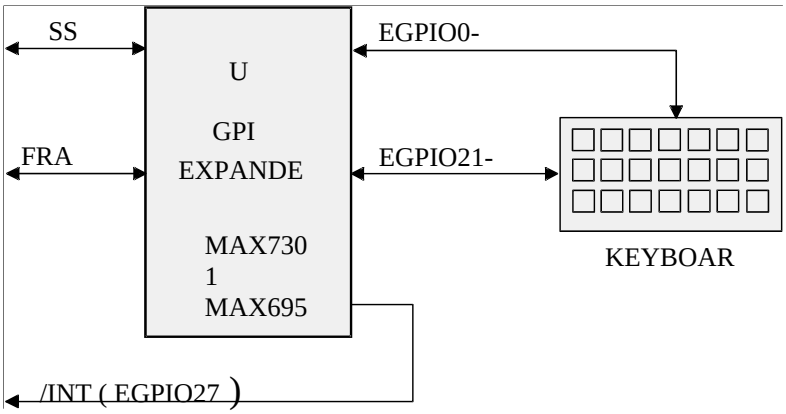


Figure 39: Matrix Keyboard Connection

18 GPIO Expansion Board Interface

The Carrier Board also provides a socket for standardized PHYTEC Expansion Boards. All signals except the data, address and control bus of the phyCORE-PXA270 extend from phyCORE connector X18 to the expansion connector X17 in a strict 1:1 arrangement. The data, address and control bus is buffered on the Carrier Board over line driver circuits before being routed to X17. The Ethernet signals do not extend to the expansion connector.

Similar to the numbering scheme of the phyCORE connector, the expansion connector also uses a two-dimensional matrix.

Please refer to the following figure for the arrangement of the number matrix for the expansion connector:

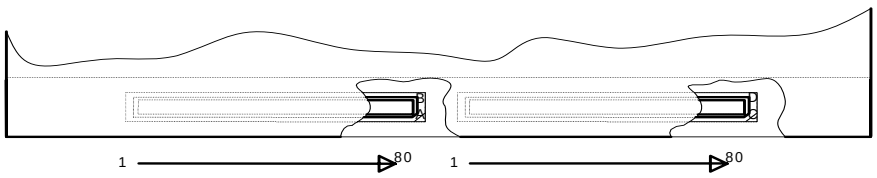


Figure 40: GPIO Expansion Bus Numbering Scheme

In the current version of the address decoder there is no memory area provided for the expansion card receptacle, because all /CS signals of the PXA270 are already used for other functions. The following tables give the signal assignments for the signals of the GPIO expansion bus connector X17. Signals that are in bold are buffered on the Carrier Board.

Pin Number	Signal	I/O	Comments
Pin Row X17A			
1A	CLKIN	I	Optional external clock input of the processor
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	CLK_REQ	I/O	Indicates Clocksource
4A	GPIO0	I/O	Processor I/O port, *alternative: interrupt*
5A	**x/CS_2**	I/O	Freely available /CS signal of the processor, *alternative: GPIO78*
6A	**x/CS_4**	I/O	Chip Select signal of the processor, *alternative: GPIO80*
8A	**x/WE**	O	Write-enable signal for SDRAM, SRAM and Flash devices. Please note that the /PWE signal must be used for I/O components.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A, 36A	**xA1, xA2, xA4, xA7, xA9, xA10, xA12, xA15, xA17, xA18, xA20, xA23, xA24**	I/O	Address lines
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	**xD1, xD2, xD4, xD7, xD9, xD10, xD12, xD15, xD18, xD19, xD20, xD22, xD25, xD27, xD28, xD30**	I/O	Data lines
34A, 35A	**xDQM_1, xDQM_2**	O	Byte enable signals
48A	**xRDY**	I/O	Ready signal of the processor, *alternative: GPIO 18*
49A	**xRDnWR**	O	Bus control singal of the processor

Pin Number	Signal	I/O	Comments
Pin Row X17A			
50A, 51A	**xDREQ_0** **xDVAL_0**	O	DMA request singal DREQ0 *alternative: GPIO 115* DVAL0 *alternative: GPIO 116*
53A,	**x/SDCKE_0**	O	Clock enable for synchronous memory
55A, 56A	**x/SDCLK_0** **x/SDCLK_1**	O	Clock signal for synchronous memory
58A, 59A	**x/PCE_1** **x/PCE_2**	I/O	PCMCIA Chip Select resp. byte control signal, *alternative: GPIO85/54*
60A	**x/PWAIT**	I/O	PCMCIA wait signal, *alternative: GPIO56*
61A	**x/IOIS16**	I/O	PCMCIA 16-bit access *alternative: GPIO57*
63A	**x/PREG**	I/O	PCMCIA register control signal *alternative: GPIO55*
64A	/LAN_CS	I	I/O Chip Select for LAN controller
65A	/LAN_DATA	I	DATA Chip Select for LAN controller
66A	L_VSYNC	O	Refresh sync signal from the LCD panel with internal frame buffer *alternative: GPIO14*
68A	L_PCLK	I/O	LCD pixel clock *alternative: GPIO76*
69A	L_LCLK	I/O	LCD line clock *alternative: GPIO75*
70A	L_FCLK	I/O	LCD frame clock *alternative: GPIO74*
71A	L_BIAS	I/O	LCD enable *alternative: GPIO77*
73A, 74A, 75A, 76A, 78A, 79A, 80A	L_DD3, L_DD5 L_DD6, L_DD8, L_DD11, L_DD13 L_DD14	I/O	LCD data *alternative: GPIO61, GPIO63, GPIO64, GPIO66, GPIO69, GPIO71, GPIO72*

Pin Number	Signal	I/O	Comments
Pin Row X17B			
1B	STBY	I	STBY = 1 /SDRAM buffered by VBAT
2B	SYS_ENA	O	System Power Switch signal
3B	GPIO_1	I/O	Processor I/O port, *alternative: interrupt*
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND	-	Ground 0 V
5B	**x/CS_1x**		If J19 = 1+2 on the phyCORE-PXA270 then x/CS_1x is not available because it is used as /CS Signal for the second on-board 16-bit Flash, *alternative: GPIO15*
6B	**x/CS_5**	I/O	Chip Select signal of the processor, can be used to access the LAN controller, *alternative: GPIO33*
7B	**x/OE**	O	Output-enable signal of the processor
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B 36B	**xA0, xA3, xA5, xA6, xA8, xA11, xA13, xA14, xA16, xA19, xA21, xA22, xA25**	I/O	Address lines
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	**xD0, xD3, xD5, xD6, xD8, xD11, xD13, xD14, xD16, xD17, xD21, xD23, xD24, xD26, xD29, xD31**	I/O	Data lines
33B, 35B	**xDQM_0, xDQM_3**	O	Byte enable signals
47B	**x/CS_0**	O	Chip Select for on-board Flash
48B	**x/CS_1y**	I/O	If J19 = 2+3 on the phyCORE-PXA270 then x/CS_1y is not available because it is used as /CS Signal for the second on-board 16-bit Flash, *alternative: GPIO15*
50B 51B 52B 53B	**x/SDCS_0** **x/SDCS_1** **x/SDCS_2,** **x/SDCS_3**	O O IO IO	/CS SDRAM bank #0 /CS SDRAM bank #1 /CS SDRAM bank #2 *alternative: GPIO20* /CS SDRAM bank #3 *alternative: GPIO21*
55B	**x/SDCLK_2**	O	Clock signal for synchronous memory
56B	**x/SDRAS**	O	/SDRAS control signal for SDRAM

Pin Number	Signal	I/O	Comments
Pin Row X17B			
57B	**x/SDCAS**	O	/SDCAS control signal for SDRAM
58B	**x/PSKSEL**	I/O	Card0/1 select *alternative: GPIO 79*
60B	**x/PWE**	I/O	PCMCIA memory write signal and I/O write signal *alternative: GPIO 49*
61B	**x/POE**	I/O	PCMCIA memory read signal *alternative: GPIO 48*
62B	**x/PIOR**	I/O	PCMCIA I/O read signal *alternative: GPIO 50*
63B	**x/PIOW**	I/O	PCMCIA I/O write signal *alternative: GPIO 51*
65B	/LAN_IRQ	I/O	Interrupt LAN controller
66B	L_CS	O	LCD CS *alternative: GPIO 19*
67B	L_DD16	O	LCD data *alternative: GPIO 86*
68B	L_DD17	O	LCD data *alternative: GPIO 87*
70B, 71B, 72B, 73B, 75B, 76B 77B, 78B 80B	L_DD0, L_DD1, L_DD2, L_DD4, L_DD7, L_DD9, L_DD10, L_DD12, L_DD15	I/O	LCD data bus *alternative: GPIO 58, GPIO 59, GPIO 60, GPIO 65, GPIO 67, GPIO 68, GPIO 70, GPIO 73*
Pin Row X17C			
1C, 2C	+3V3	P	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C 72C, 77C	GND	P	Ground 0 V
4C	VMMC	P	Optional supply voltage for internal MMC card
5C	VBAT	P	Input for external battery
6C	VCC_LCD	P	VCC for LCD Port
8C	USB_H_PWR	P	Over-current indicator from ports 3, 2 and 1
9C	USIM_VCC	P	VCC (3.0 V or 1.8 V) USIM
10C	/RESIN	I/O	/Reset input for reset controller at U9
11C	/RESET_OUT	I/O	/Reset output of the PXA270 processor
13C	NSSP_TxD	I/O	Network SPI TxD signal, used for CAN Controller *Alternative: GPIO 81*

Pin Number	Signal	I/O	Comments
Pin Row X17C			
14C	NSSP_CLK	I/O	Network SPI Clock signal *Alternative: GPIO 84*
15C	NSSP_RxD	I/O	Network SPI RxD signal *Alternative: GPIO 82*
16C	NSSP_FRM	I/O	Network SPI Frame signal, used for CAN Controller *alternative: GPIO 83*
18C	IR_TXD	O	IrDA TxD *Alternative: GPIO 47*
19C	IR_RXD	I	IrDA RxD *Alternative: GPIO 46*
20C	FF_RI_DETECT	O	RI-Detect FF-UART (for interrupt)
21C	FF_/INVALID	O	Invalid level FF_UART
23C	/ACRESET	O	/RESET AC97 *Alternative: GPIO 113*
24C	SYNC	I/O	SYNC AC97 *Alternative: GPIO 31*
25C	BITCLK	I/O	BITCLK *Alternative: GPIO 28*
26C	nc		No connect
28C	SDATA_IN_0	I/O	SDATA_IN0 (AC97 interface) *Alternative: GPIO 29*
29C	SDATA_OUT	I/O	SDATAOUT *Alternative: GPIO 30*
30C	SDA	I/O	I^2C data from processor *Alternative: GPIO 118*
31C	SCL	I	I^2C clock from processor *Alternative: GPIO 117*
33C	EXP0	O	General purpose output from PLD U7.
34C	EXP1	O	General purpose output from PLD U7.
35C	EXP2	O	General purpose output from PLD U7.
36C	EXP3	O	General purpose output from PLD U7.
38C	OTG_ID	I	OTD ID Input USB Controller
39C	PWM0	O	PWM output #0 *Alternative: GPIO 16*
40C	PWM1	O	PWM output #1 *Alternative: GPIO 17*
41C	/TRST	O	JTAG reset
43C	USIM_IO	IO	USIM I/O Data. Receive and transmit data connection

Pin Number	Signal	I/O	Comments
Pin Row X17C			
44C	nc		No connect
45C	MMC_DAT2_CS0	O	MMC_C0 for external MMC card *Alternative: GPIO 110*
46C	MMC_DAT3_CS1	O	MMC_C1 for internal MMC card *Alternative: GPIO 111*
48C, 49C, 50C, 51C, 53C	GPIO114, GPIO9 GPIO10, GPIO12, GPIO90	I/O	GPIOs *Alternative: interrupt signals*
54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C	EGPIO0, EGPIO1, EGPIO3, EGPIO6, EGPIO8, EGPIO9, EGPIO11, EGPIO14, EGPIO16, EGPIO17 EGPIO18, EGPIO22, EGPIO24 EGPIO25, EGPIO27	I/O	Additional GPIOs generated by the MAX7301 IC
73C	SSP_RXD	I	SPI RxD signal *Alternative: GPIO 26*
74C	SSP_TXD	O	SPI TxD signal *Alternative: GPIO 25*
75C	/CS_EGPIO	I	SSP /CS1 signal for MAX7301 (EGPIO)
76C	/CAN_CS	I	/CS signal for SJA1000 (CAN)
78C	/CAN_INT	O	CAN Interrupt
79C	CANRXD	I/O	CAN RxD signal
80C	CANTXD	I/O	CAN TxD signal
Pin Row X17D			
1D, 2D	VCC	P	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	-	Ground 0 V
4D, 5D	VCC1	P	Optional external supply voltage VCORE for processor, 3 - 5.0 V
6D	VCC_BB	P	VCC Baseband
7D	USB_H_ENA	O	USB Controller Power Switch signal
8D	SYS_ENAB	O	System Power Switch signal
10D	/RESET	O	Reset output from reset controller
11D	/BATT_FAULT	I	Low battery voltage indication

Pin Number	Signal	I/O	Comments
Pin Row X17D			
12D	/VCC_FAULT	I	Low supply voltage indication
13D	PWR_ENAB	O	PXA-Core Power Signal
15D	BT_CTS	I	CTS Bluetooth UART *Alternative: GPIO 44*
16D	BT_RXD	I	RXD Bluetooth UART *Alternative: GPIO 42*
17D	BT_TXD	O	TXD Bluetooth UART *Alternative: GPIO 43*
18D	BT_RTS	O	RTS Bluetooth UART *Alternative: GPIO 45*
20D	FF_/SHDN	I	FF-UART power on
21D	FL_WP_PEN	I	Flash Write Protect
22D	RS_RXD	I	FF-UART RxD signal (RS-232)
23D	RS_TXD	O	FF-UART TxD signal (RS-232)
25D	RS_RTS	I	FF-UART RTS signal (RS-232)
26D	RS_CTS	I	FF-UART CTS signal (RS-232)
27D	RS_DSR	I	FF-UART DSR signal (RS-232)
28D	RS_DTR	O	FF-UART DTR signal (RS-232)
30D	RS_RI	I	FF-UART RI signal (RS-232)
31D	RS_DCD	I	FF-UART DCD signal (RS-232)
32D	USB_C_P	I/O	USB Client positive, from processor
33D	USB_C_N	I/O	USB Client negative, from processor
35D	-	-	Not connected
36D	-	-	Not connected
37D	USB_H _P	I/O	USB Host Controller positive, from processor
38D	USB_H_N	I/O	USB Host Controller negative, from processor
40D	TDI	I	JTAG TDI signal
41D	TDO	O	JTAG TDO signal
42D	TMS	I	JTAG TMS signal
43D	TCK	I	JTAG TCK signal
45D	MMC_CLK	I/O	MMC_CLK signal
46D	MMC_DAT0	I/O	MMC_DAT signal
47D	MMC_CMD	I/O	MMC_CMD signal
48D	MMC_DAT1	I/O	MMC_DAT1 signal
50D, 51D, 52D, 53D	GPIO11, GPIO13, GPIO52, GPIO91,	I/O	GPIOs, *alternative: interrupt signals*

Pin Number	Signal	I/O	Comments
Pin Row X17D			
55D, 56D, 57D, 58D, 60D, 61D, 62D, 63D, 65D, 66D, 67D, 68D, 70D	EGPIO2, EGPIO4, EGPIO5, EGPIO7 EGPIO10, EGPIO12, EGPIO13, EGPIO15, EGPIO19, EGPIO20, EGPIO21, EGPIO23, EGPIO26	I/O	Additional GPIOs generated by the MAX7301 IC with 7 interrupt-capable inputs for connection to a matrix keyboard
71D	SSP_EXTCLK	I	SPI external clock *alternative: GPIO 27*
72D	SSP_CLK	O	SPI clock signal *alternative: GPIO 23*
73D	SSP_SFRM	I/O	SPI frame signal *alternative: GPIO 24*
75D	FL_DIS	I	Signal to disable internal Flash
76D	SSP_SYSCLK	I/O	SYSCLOCK SSP *Alternative: GPIO 53*
77D	PWR_SDA	I/O	Power I2C Serial Data/Address signal *Alternative: GPIO 4*
78D	PWR_SCL	O	Power I2C Serial Clock Line signal *Alternative: GPIO 3*
80D	/INT_RTC	O	Interrupt output RTC

Table 53: GPIO Expansion Bus X17 Pin Assignment

The pin assignment on the phyCORE-PXA270, in conjunction with the expansion bus (X17) on the Carrier Board and the patch field on an expansion board, is as follows:

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
1A	CLKIN	1A	CLKIN	BUS0	28A	BUS0
2A	GND	2A	GND	GND	3C	GND
3A	CLKIN_OE	3A	CLKIN_OE	BUS3	28B	BUS3
4A	GPIO_0	4A	GPIO_0	BUS5	29A	BUS5
5A	**/CS_2**	5A	**/CS_2**	BUS6	29E	BUS6
6A	**/CS_4**	6A	**/CS_4**	BUS8	29D	BUS8
7A	GND	7A	GND	GND	4C	GND
8A	**/WE**	8A	**/WE**	BUS11	30E	BUS11
9A	**A1**	9A	**A1**	BUS13	30D	BUS13
10A	**A2**	10A	**A2**	BUS14	30F	BUS14
11A	**A4**	11A	**A4**	BUS16	31E	BUS16
12A	GND	12A	GND	GND	7C	GND
13A	**A7**	13A	**A7**	BUS19	32A	BUS19
14A	**A9**	14A	**A9**	BUS21	32E	BUS21
15A	**A10**	15A	**A10**	BUS22	32B	BUS22
16A	**A12**	16A	**A12**	BUS24	33A	BUS24
17A	GND	17A	GND	GND	8C	GND
18A	**A15**	18A	**A15**	BUS27	33B	BUS27
19A	**D1**	19A	**D1**	BUS29	34A	BUS29
20A	**D2**	20A	**D2**	BUS30	34E	BUS30
21A	**D4**	21A	**D4**	BUS32	34D	BUS32
22A	GND	22A	GND	GND	9C	GND
23A	**D7**	23A	**D7**	BUS35	35E	BUS35
24A	**A17**	24A	**A17**	BUS37	35D	BUS37
25A	**A18**	25A	**A18**	BUS38	35F	BUS38
26A	**A20**	26A	**A20**	BUS40	36E	BUS40
27A	GND	27A	GND	GND	12C	GND
28A	**A23**	28A	**A23**	BUS43	37A	BUS43
29A	**D9**	29A	**D9**	BUS45	37E	BUS45
30A	**D10**	30A	**D10**	BUS46	37B	BUS46
31A	**D12**	31A	**D12**	BUS48	38A	BUS48
32A	GND	32A	GND	GND	13C	GND
33A	**D15**	33A	**D15**	BUS51	38B	BUS51
34A	**DQM1**	34A	**DQM1**	BUS53	39A	BUS53
35A	**DQM2**	35A	**DQM2**	BUS54	39E	BUS54
36A	**A24**	36A	**A24**	BUS56	39D	BUS56
37A	GND	37A	GND	GND	14C	GND
38A	**D18**	38A	**D18**	BUS59	40E	BUS59
39A	**D19**	39A	**D19**	BUS61	40D	BUS61
40A	**D20**	40A	**D20**	BUS62	40F	BUS62

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
41A	**D22**	41A	**D22**	BUS64	41E	BUS64
42A	GND	42A	GND	GND	17C	GND
43A	**D25**	43A	**D25**	BUS67	42A	BUS67
44A	**D27**	44A	**D27**	BUS69	42E	BUS69
45A	**D28**	45A	**D28**	BUS70	42B	BUS70
46A	**D30**	46A	**D30**	BUS72	43A	BUS72
47A	GND	47A	GND	GND	18C	GND
48A	**RDY**	48A	**RDY**	BUS75	43B	BUS75
49A	**RDnWR**	49A	**RDnWR**	BUS77	44A	BUS77
50A	**DREQ_0**	50A	**DREQ_0**	BUS78	44E	BUS78
51A	**DVAL_0**	51A	**DVAL_0**	BUS80	44D	BUS80
52A	GND	52A	GND	GND	19C	GND
53A	**/SDCKE_0**	53A	**/SDCKE_0**	BUS83	45E	BUS83
54A		54A		BUS85	45D	BUS85
55A	**/SDCLK_0**	55A	**/SDCLK_0**	BUS86	45F	BUS86
56A	**/SDCLK_1**	56A	**/SDCLK_1**	BUS88	46E	BUS88
57A	GND	57A	GND	GND	22C	GND
58A	**/PCE_1**	58A	**/PCE_1**	BUS91	47A	BUS91
59A	**/PCE_2**	59A	**/PCE_2**	BUS93	47E	BUS93
60A	**/PWAIT**	60A	**/PWAIT**	BUS94	47B	BUS94
61A	**/IOIS16**	61A	**/IOIS16**	BUS96	48A	BUS96
62A	GND	62A	GND	GND	23C	GND
63A	**/PREG**	63A	**/PREG**	BUS99	48B	BUS99
64A	/LAN_CS	64A	/LAN_CS	BUS101	49A	BUS101
65A	/LAN_DATA	65A	/LAN_DATA	BUS102	49E	BUS102
66A	L_VSYNC	66A	L_VSYNC	BUS104	49D	BUS104
67A	GND	67A	GND	GND	24C	GND
68A	L_PCLK	68A	L_PCLK	BUS107	50E	BUS107
69A	L_LCLK	69A	L_LCLK	BUS109	50D	BUS109
70A	L_FCLK	70A	L_FCLK	BUS110	50F	BUS110
71A	L_BIAS	71A	L_BIAS	BUS112	51E	BUS112
72A	GND	72A	GND	GND	29C	GND
73A	L_DD3	73A	L_DD3	BUS115	52A	BUS115
74A	L_DD5	74A	L_DD5	BUS117	52E	BUS117
75A	L_DD6	75A	L_DD6	BUS118	52B	BUS118
76A	L_DD8	76A	L_DD8	BUS120	53A	BUS120
77A	GND	77A	GND	GND	30C	GND
78A	L_DD11	78A	L_DD11	BUS123	53B	BUS123
79A	L_DD13	79A	L_DD13	BUS125	54A	BUS125
80A	L_DD14	80A	L_DD14	BUS126	54E	BUS126

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
1B		1B		BUS1	28C	BUS1
2B		2B		BUS2	28E	BUS2
3B	GPIO_1	3B	GPIO_1	BUS4	28F	BUS4
4B	GND	4B	GND	GND	31C	GND
5B		5B		BUS7	29B	BUS7
6B	**/CS_5**	6B	**/CS_5**	BUS9	29F	BUS9
7B	**/OE**	7B	**/OE**	BUS10	30A	BUS10
8B	**A0**	8B	**A0**	BUS12	30B	BUS12
9B	GND	9B	GND	GND	34C	GND
10B	**A3**	10B	**A3**	BUS15	31A	BUS15
11B	**A5**	11B	**A5**	BUS17	31B	BUS17
12B	**A6**	12B	**A6**	BUS18	31F	BUS18
13B	**A8**	13B	**A8**	BUS20	32C	BUS20
14B	GND	14B	GND	GND	35C	GND
15B	**A11**	15B	**A11**	BUS23	32F	BUS23
16B	**A13**	16B	**A13**	BUS25	33C	BUS25
17B	**A14**	17B	**A14**	BUS26	33E	BUS26
18B	**D0**	18B	**D0**	BUS28	33F	BUS28
19B	GND	19B	GND	GND	36C	GND
20B	**D3**	20B	**D3**	BUS31	34B	BUS31
21B	**D5**	21B	**D5**	BUS33	34F	BUS33
22B	**D6**	22B	**D6**	BUS34	35A	BUS34
23B	**A16**	23B	**A16**	BUS36	35B	BUS36
24B	GND	24B	GND	GND	39C	GND
25B	**A19**	25B	**A19**	BUS39	36A	BUS39
26B	**A21**	26B	**A21**	BUS41	36B	BUS41
27B	**A22**	27B	**A22**	BUS42	36F	BUS42
28B	**D8**	28B	**D8**	BUS44	37C	BUS44
29B	GND	29B	GND	GND	40C	GND
30B	**D11**	30B	**D11**	BUS47	37F	BUS47
31B	**D13**	31B	**D13**	BUS49	38C	BUS49
32B	**D14**	32B	**D14**	BUS50	38E	BUS50
33B	**DQM_0**	33B	**DQM_0**	BUS52	38F	BUS52
34B	GND	34B	GND	GND	41C	GND
35B	**DQM_3**	35B	**DQM_3**	BUS55	39B	BUS55
36B	**A25**	36B	**A25**	BUS57	39F	BUS57
37B	**D16**	37B	**D16**	BUS58	40A	BUS58
38B	**D17**	38B	**D17**	BUS60	40B	BUS60
39B	GND	39B	GND	GND	44C	GND
40B	**D21**	40B	**D21**	BUS63	41A	BUS63

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
41B	**D23**	41B	**D23**	BUS65	41B	BUS65
42B	**D24**	42B	**D24**	BUS66	41F	BUS66
43B	**D26**	43B	**D26**	BUS68	42C	BUS68
44B	GND	44B	GND	GND	45C	GND
45B	**D29**	45B	**D29**	BUS71	42F	BUS71
46B	**D31**	46B	**D31**	BUS73	43C	BUS73
47B	**/CS_0**	47B	**/CS_0**	BUS74	43E	BUS74
48B	**/CS_1**	48B	**/CS_1**	BUS76	43F	BUS76
49B	GND	49B	GND	GND	46C	GND
50B	**/SDCS_0**	50B	**/SDCS_0**	BUS79	44B	BUS79
51B	**/SDCS_1**	51B	**/SDCS_1**	BUS81	44F	BUS81
52B	**/SDCS_2**	52B	**/SDCS_2**	BUS82	45A	BUS82
53B	**/SDCS_3**	53B	**/SDCS_3**	BUS84	45B	BUS84
54B	GND	54B	GND	GND	49C	GND
55B	**/SDCLK_2**	55B	**/SDCLK_2**	BUS87	46A	BUS87
56B	**/SDRAS**	56B	**/SDRAS**	BUS89	46B	BUS89
57B	**/SDCAS**	57B	**/SDCAS**	BUS90	46F	BUS90
58B	**/PSKSEL**	58B	**/PSKSEL**	BUS92	47C	BUS92
59B	GND	59B	GND	GND	50C	GND
60B	**/PWE**	60B	**/PWE**	BUS95	47F	BUS95
61B	**/POE**	61B	**/POE**	BUS97	48C	BUS97
62B	**/PIOR**	62B	**/PIOR**	BUS98	48E	BUS98
63B	**/PIOW**	63B	**/PIOW**	BUS100	48F	BUS100
64B	GND	64B	GND	GND	51C	GND
65B	LAN_IRQ	65B	LAN_IRQ	BUS103	49B	BUS103
66B	L_CS	66B	L_CS	BUS105	49F	BUS105
67B	L_DD16	67B	L_DD16	BUS106	50A	BUS106
68B	L_DD17	68B	L_DD17	BUS108	50B	BUS108
69B	GND	69B	GND	GND	54C	GND
70B	L_DD0	70B	L_DD0	BUS111	51A	BUS111
71B	L_DD1	71B	L_DD1	BUS113	51B	BUS113
72B	L_DD2	72B	L_DD2	BUS114	51F	BUS114
73B	L_DD4	73B	L_DD4	BUS116	52C	BUS116
74B	GND	74B	GND	GND	4D	GND
75B	L_DD7	75B	L_DD7	BUS119	52F	BUS119
76B	L_DD9	76B	L_DD9	BUS121	53C	BUS121
77B	L_DD10	77B	L_DD10	BUS122	53E	BUS122
78B	L_DD12	78B	L_DD12	BUS124	53F	BUS124
79B	GND	79B	GND	GND	5D	GND
80B	L_DD15	80B	L_DD15	BUS127	54B	BUS127

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
1C	VCC	1C	VCC	*VCC1*	1A	*VCC1*
2C	VCC	2C	VCC	*VCC1*	1C	*VCC1*
3C	GND	3C	GND	GND	6D	GND
4C	VMMC	4C	VMMC	*VCC2*	1B	*VCC2*
5C	VBAT	5C	VBAT	*VCC2*	2A	*VCC2*
6C	VCC_LCD	6C	VCC_LCD	*VBAT*	2B	*VBAT*
7C	GND	7C	GND	GND	9D	GND
8C	USB_H_PWR	8C	USB_H_PWR	*PFO*	3E	*PFO*
9C		9C		*BOOT*	3B	*BOOT*
10C	/RESIN	10C	/RESIN	*/RESET*	3D	*/RESET*
11C	/RESET_OUT	11C	/RESET_OUT	*/RESETOUT*	4E	*/RESETOUT*
12C	GND	12C	GND	GND	10D	GND
13C	NSSP_TxD	13C	NSSP_TxD	GPIO2	4F	GPIO2
14C	NSSP_CLK	14C	NSSP_CLK	GPIO4	5C	GPIO4
15C	NSSP_RxD	15C	NSSP_RXD	GPIO5	5E	GPIO5
16C	NSSP_FRAM	16C	NSSP_FRAM	GPIO7	5F	GPIO7
17C	GND	17C	GND	GND	11D	GND
18C	IR_TxD	18C	IR_TxD	GPIO10	6E	GPIO10
19C	IR_RxD	19C	IR_RxD	GPIO12	6F	GPIO12
20C	FF_RI_DETECT	20C	FF_RI_DETECT	GPIO13	7A	GPIO13
21C	FF_/INVALID	21C	FF_/INVALID	GPIO15	7B	GPIO15
22C	GND	22C	GND	GND	14D	GND
23C	/ACRESET	23C	/ACRESET	GPIO18	8A	GPIO18
24C	SYNC	24C	SYNC	GPIO20	8B	GPIO20
25C	BITCLK	25C	BITCLK	GPIO21	8D	GPIO21
26C		26C		GPIO23	9A	GPIO23
27C	GND	27C	GND	GND	15D	GND
28C	SDATA_IN_0	28C	SDATA_IN_0	GPIO26	9F	GPIO26
29C	SDATA_OUT	29C	SDATA_OUT	GPIO28	10C	GPIO28
30C	SDA	30C	SDA	GPIO29	10E	GPIO29
31C	SCL	31C	SCL	GPIO31	10F	GPIO31
32C	GND	32C	GND	GND	16D	GND
33C	*/LAN_LED_A*	*33C*	*EXP0*	GPIO34	11E	GPIO34
34C	*/LAN_LED_B*	*34C*	*EXP1*	GPIO36	11F	GPIO36
35C	*LAN_TPI-*	*35C*	*EXP2*	GPIO37	12A	GPIO37
36C	*LAN_TPO-*	*36C*	*EXP3*	GPIO39	12B	GPIO39
37C	GND	37C	GND	GND	19D	GND
38C	OTG_ID	38C	OTG_ID	GPIO42	13A	GPIO42
39C	PWM0	39C	PWM0	GPIO44	13B	GPIO44
40C	PWM1	40C	PWM1	GPIO45	13D	GPIO45

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
41C	/TRST	41C	/TRST	GPIO47	14A	GPIO47
42C	GND	42C	GND	GND	20D	GND
43C	USIM_UIO	43C	USIM_UIO	GPIO50	14F	GPIO50
44C		44C		GPIO52	15C	GPIO52
45C	MMC_DAT2_CS0	45C	MMC_DAT2_CS0	GPIO53	15E	GPIO53
46C	MMC_DAT3_CS1	46C	MMC_DAT3_CS1	GPIO55	15F	GPIO55
47C	GND	47C	GND	GND	21D	GND
48C	GPIO_114	48C	GPIO_114	GPIO58	16E	GPIO58
49C	GPIO_9	49C	GPIO_9	GPIO60	16F	GPIO60
50C	GPIO_10	50C	GPIO_10	GPIO61	17A	GPIO61
51C	GPIO_12	51C	GPIO_12	GPIO63	17B	GPIO63
52C	GND	52C	GND	GND	24D	GND
53C	GPIO_90	53C	GPIO_90	GPIO66	18A	GPIO66
54C	EGPIO_0	54C	EGPIO_0	GPIO68	18B	GPIO68
55C	EGPIO_1	55C	EGPIO_1	GPIO69	18D	GPIO69
56C	EGPIO_3	56C	EGPIO_3	GPIO71	19A	GPIO71
57C	GND	57C	GND	GND	25D	GND
58C	EGPIO_6	58C	EGPIO_6	GPIO74	19F	GPIO74
59C	EGPIO_8	59C	EGPIO_8	GPIO76	20C	GPIO76
60C	EGPIO_9	60C	EGPIO_9	GPIO77	20E	GPIO77
61C	EGPIO_11	61C	EGPIO_11	GPIO79	20F	GPIO79
62C	GND	62C	GND	GND	26D	GND
63C	EGPIO_14	63C	EGPIO_14	GPIO82	21E	GPIO82
64C	EGPIO_16	64C	EGPIO_16	GPIO84	21F	GPIO84
65C	EGPIO_17	65C	EGPIO_17	GPIO85	22A	GPIO85
66C	EGPIO_18	66C	EGPIO_18	GPIO87	22B	GPIO87
67C	GND	67C	GND	GND	31D	GND
68C	EGPIO_22	68C	EGPIO_22	GPIO90	23A	GPIO90
69C	EGPIO_24	69C	EGPIO_24	GPIO92	23B	GPIO92
70C	EGPIO_25	70C	EGPIO_25	GPIO93	23D	GPIO93
71C	EGPIO_27	71C	EGPIO_27	GPIO95	24A	GPIO95
72C	GND	72C	GND	GND	32D	GND
73C	SSP_RxD	73C	SSP_RxD	GPIO98	24F	GPIO98
74C	SSP_TxD	74C	SSP_TxD	GPIO100	25C	GPIO100
75C	/CS_EGPIO	75C	/CS_EGPIO	GPIO101	25E	GPIO101
76C	/CAN_CS0	76C	/CAN_CS0	GPIO103	25F	GPIO103
77C	GND	77C	GND	GND	33D	GND
78C	/CAN_INT	78C	/CAN_INT	GPIO106	26E	GPIO106
79C	CANRxD	79C	CANRxD	GPIO108	26F	GPIO108
80C	CANTxD	80C	CANTxD	GPIO109	27A	GPIO109

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
1D	VCC	1D	VCC	*VCC1*	1A	*VCC1*
2D	VCC	2D	VCC	*VCC1*	1C	*VCC1*
3D	GND	3D	GND	GND	36D	GND
4D	VCC1	4D	VCC1	*VCC3*	1D	*VCC3*
5D	VCC1	5D	VCC1	*VCC3*	2C	*VCC3*
6D	VCC_BB	6D	VCC_BB	*VPD*	2D	*VPD*
7D	USB_H_ENA	7D	USB_H_ENA	*PFI*	2F	*PFI*
8D	SYS_ENAB	8D	SYS_ENAB	*WDI*	3A	*WDI*
9D	GND	9D	GND	GND	37D	GND
10D	/RESET	10D	/RESET	*/RESIN*	3F	*/RESIN*
11D	/BATT_FAULT	11D	/BATT_FAULT	GPIO0	4A	GPIO0
12D	/VCC_FAULT	12D	/VCC_FAULT	GPIO1	4B	GPIO1
13D	PWR_ENAB	13D	PWR_ENAB	GPIO3	5A	GPIO3
14D	GND	14D	GND	GND	38D	GND
15D	BT_CTS	15D	BT_CTS	GPIO6	5B	GPIO6
16D	BT_RxD	16D	BT_RxD	GPIO8	6A	GPIO8
17D	BT_TxD	17D	BT_TxD	GPIO9	6C	GPIO9
18D	BT_RTS	18D	BT_RTS	GPIO11	6B	GPIO11
19D	GND	19D	GND	GND	41D	GND
20D	FF_/SHDN	20D	FF_/SHDN	GPIO14	7E	GPIO14
21D	FL_/WP_PEN	21D	FL_/WP_PEN	GPIO16	7D	GPIO16
22D	RS_RxD	22D	RS_RxD	GPIO17	7F	GPIO17
23D	RS_TxD	23D	RS_TxD	GPIO19	8E	GPIO19
24D	GND	24D	GND	GND	42D	GND
25D	RS_RST	25D	RS_RST	GPIO22	8F	GPIO22
26D	RS_CTS	26D	RS_CTS	GPIO24	9E	GPIO24
27D	RS_DSR	27D	RS_DSR	GPIO25	9B	GPIO25
28D	RS_DTR	28D	RS_DTR	GPIO27	10A	GPIO27
29D	GND	29D	GND	GND	43D	GND
30D	RS_RI	30D	RS_RI	GPIO30	10B	GPIO30
31D	RS_DCD	31D	RS_DCD	GPIO32	11A	GPIO32
32D	USB_C_P	32D	USB_C_P	GPIO33	11C	GPIO33
33D	USB_C_N	33D	USB_C_N	GPIO35	11B	GPIO35
34D	GND	34D	GND	GND	46D	GND
35D	LAN_TPI+	35D	N.C.	GPIO38	12E	GPIO38
36D	LAN_TPO+	36D	N.C.	GPIO40	12D	GPIO40
37D	USB_H_P	37D	USB_H_P	GPIO41	12F	GPIO41
38D	USB_H_N	38D	USB_H_N	GPIO43	13E	GPIO43
39D	GND	39D	GND	GND	47D	GND
40D	TDI	40D	TDI	GPIO46	13F	GPIO46

phyCORE-PXA270 X18		**Carrier Board X17**			**Expansion Board Patch Field**	
41D	TDO	41D	TDO	GPIO48	14E	GPIO48
42D	TMS	42D	TMS	GPIO49	14B	GPIO49
43D	TCK	43D	TCK	GPIO51	15A	GPIO51
44D	GND	44D	GND	GND	48D	GND
45D	MMC_CLK	45D	MMC_CLK	GPIO54	15B	GPIO54
46D	MMC_DAT0	46D	MMC_DAT0	GPIO56	16A	GPIO56
47D	MMC_CMD	47D	MMC_CMD	GPIO57	16C	GPIO57
48D	MMC_DAT1	48D	MMC_DAT1	GPIO59	16B	GPIO59
49D	GND	49D	GND	GND	51D	GND
50D	GPIO_11	50D	GPIO_11	GPIO62	17E	GPIO62
51D	GPIO_13	51D	GPIO_13	GPIO64	17D	GPIO64
52D	GPIO_52	52D	GPIO_52	GPIO65	17F	GPIO65
53D	GPIO_91	53D	GPIO_91	GPIO67	18E	GPIO67
54D	GND	54D	GND	GND	52D	GND
55D	EGPIO2	55D	EGPIO2	GPIO70	18F	GPIO70
56D	EGPIO4	56D	EGPIO4	GPIO72	19E	GPIO72
57D	EGPIO5	57D	EGPIO5	GPIO73	19B	GPIO73
58D	EGPIO7	58D	EGPIO7	GPIO75	20A	GPIO75
59D	GND	59D	GND	GND	53D	GND
60D	EGPIO10	60D	EGPIO10	GPIO78	20B	GPIO78
61D	EGPIO12	61D	EGPIO12	GPIO80	21A	GPIO80
62D	EGPIO12	62D	EGPIO12	GPIO81	21C	GPIO81
63D	EGPIO15	63D	EGPIO15	GPIO83	21B	GPIO83
64D	GND	64D	GND	GND	1E	GND
65D	EGPIO19	65D	EGPIO19	GPIO86	22E	GPIO86
66D	EGPIO20	66D	EGPIO20	GPIO88	22D	GPIO88
67D	EGPIO21	67D	EGPIO21	GPIO89	22F	GPIO89
68D	EGPIO23	68D	EGPIO23	GPIO91	23E	GPIO91
69D	GND	69D	GND	GND	2E	GND
70D	EGPIO26	70D	EGPIO26	GPIO94	23F	GPIO94
71D	SSP_EXTCLK	71D	SSP_EXTCLK	GPIO96	24E	GPIO96
72D	SSP_CLK	72D	SSP_CLK	GPIO97	24B	GPIO97
73D	SSP_FRM	73D	SSP_FRM	GPIO99	25A	GPIO99
74D	GND	74D	GND	GND	1F	GND
75D	FL_DIS	75D	FL_DIS	GPIO102	25B	GPIO102
76D	SSP_SYSCLK	76D	SSP_SYSCLK	GPIO104	26A	GPIO104
77D	PWR_SDA	77D	PWR_SDA	GPIO105	26C	GPIO105
78D	PWR_SCL	78D	PWR_SCL	GPIO107	26B	GPIO107
79D	GND	79D	GND	GND	1F	GND
80D	/INT_RTC	80D	/INT_RTC	GPIO110	27E	GPIO110

Table 54: Signal Pin Assignment for the phyCORE-PXA270 / Carrier Board / Expansion Board

19 JTAG Interface (X29)

The PXA270 provides a JTAG interface for debuggers, emulators and boundary scan devices. All JTAG interface signals extend from the phyCORE-connector to an ARM-compatible, dual row, 20-pin connector at X29. The location of this JTAG connector can be found in *Figure 2*.

The following table describes the pin assignment for the JTAG interface.

Signal	X29		Signal
VREF	**1**	**2**	VCC
/JTAG-RESET	**3**	**4**	GND
JTAG-TDI	**5**	**6**	GND
JTAG-TMS	**7**	**8**	GND
JTAG-TCK	**9**	**10**	GND
JTAG-RTCK	**11**	**12**	GND
JTAG-TDO	**13**	**14**	GND
/RESIN (System)	**15**	**16**	GND
N.C.	**17**	**18**	GND
N.C.	**19**	**20**	GND

Table 55: JTAG Connector X29 Pinout

20 Technical Specifications

The physical dimensions of the Carrier Board are represented in *Figure 41*.

PHYTEC is currently working on an enclosure for this Carrier Board with Expansion Board. The dimensions shown below are subject to change. The maximum height of all components, the inserted phyCORE module and with a display mounted on the PCB is ca. 40 mm.

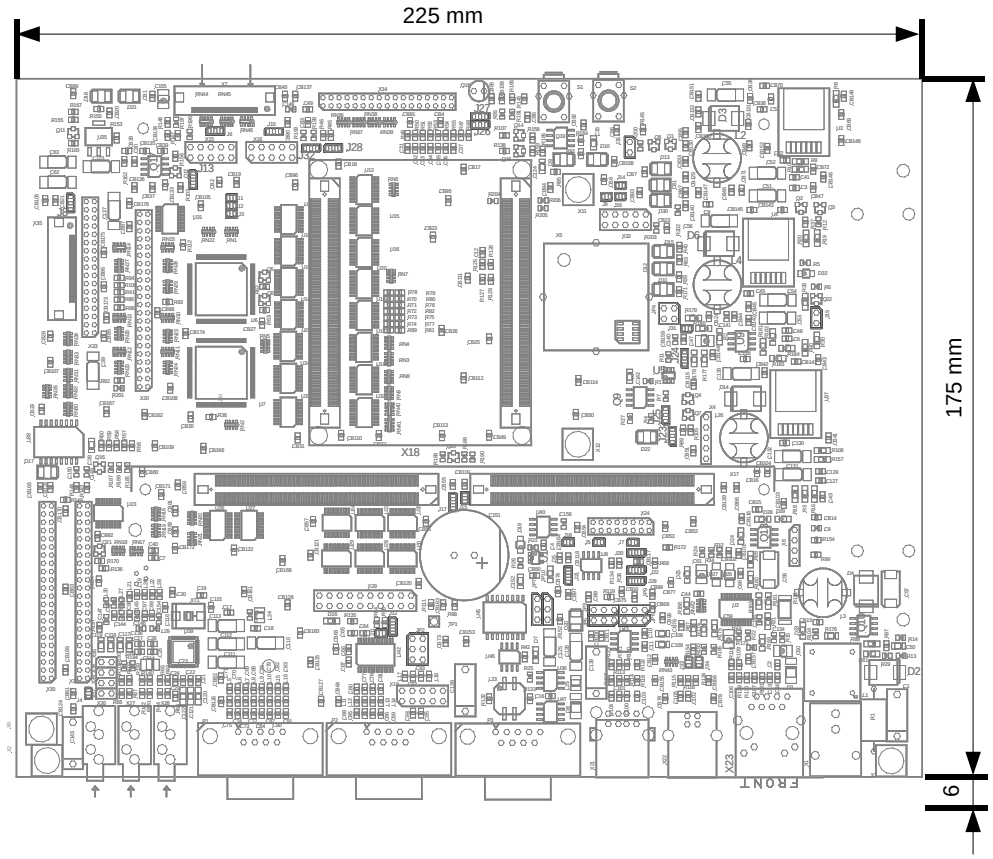


Figure 41: Physical Dimensions (Carrier Board)

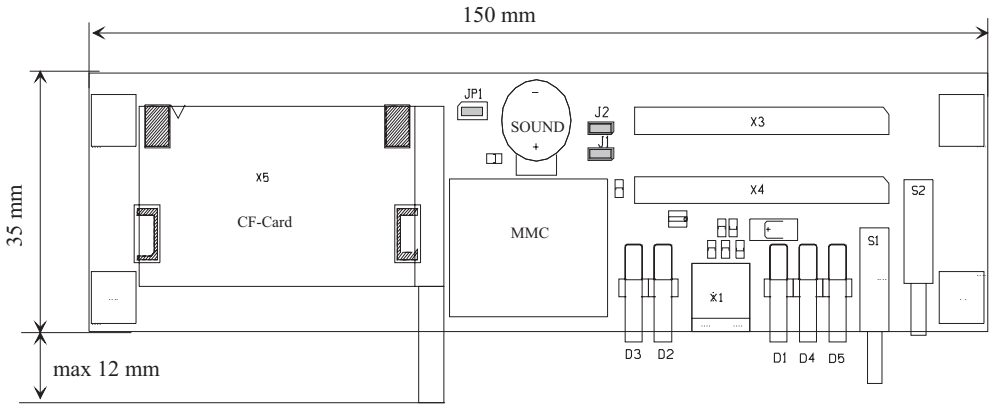


Figure 42: Physical Dimensions (Expansion Board)

Additional specifications:

- Dimensions (Carrier Board): 225 mm x 170 mm
- Dimensions (Expansion Board): 35 mm x 150 mm
- Weight: approximately 1000 grams
- Storage temperature: 0°C to +85°C
- Operating temperature: 0°C to +70°C
- Humidity: 95 % r.F. not condensed
- Operating voltage: 12 VDC ±5 %
  supplied via power jack

- Power consumption:
  operating with peripheral components
  incl. LCD and hard disk min. 8.5 W, max 15 W

These specifications describe the standard configuration of the Carrier Board as of printing of this manual.

21 Hints for Handling the Module

- **Modifications on the phyCORE-PXA270 Carrier Board and Expansion Board**

Removal of various components is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-PXA270 into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected.

22 Component Placement Diagram

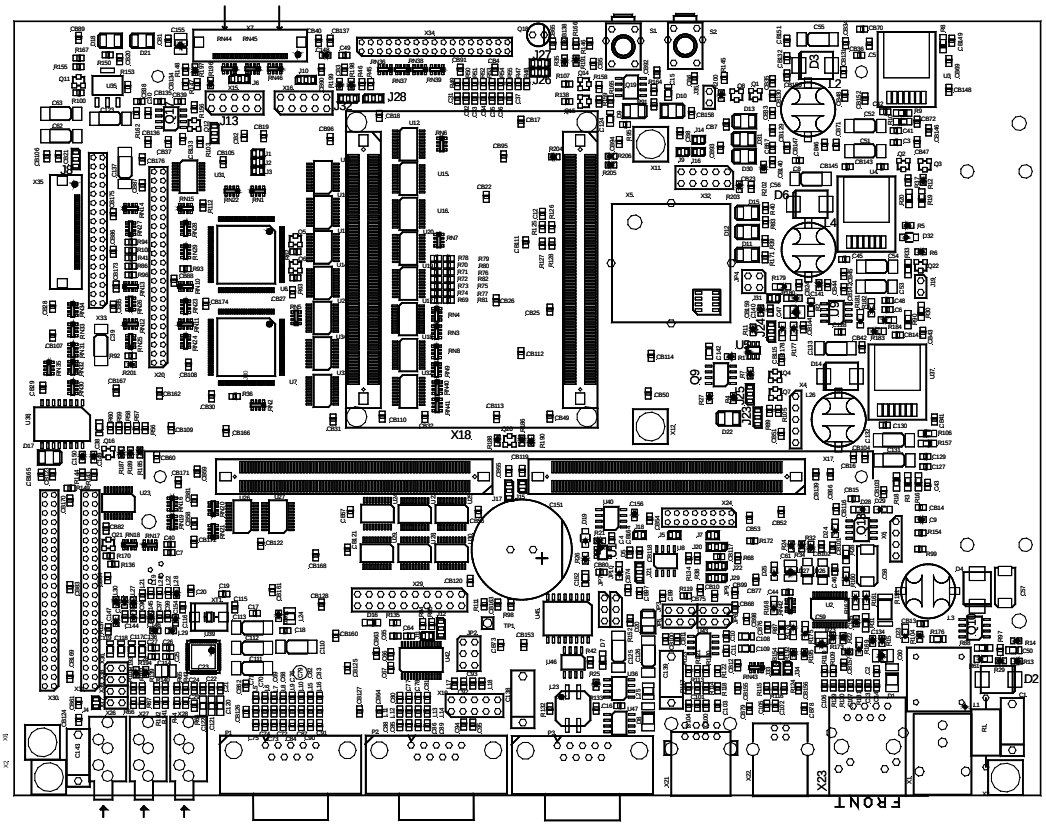


Figure 43: Component Placement Diagram Carrier Board (PCB Revision 1220.3)

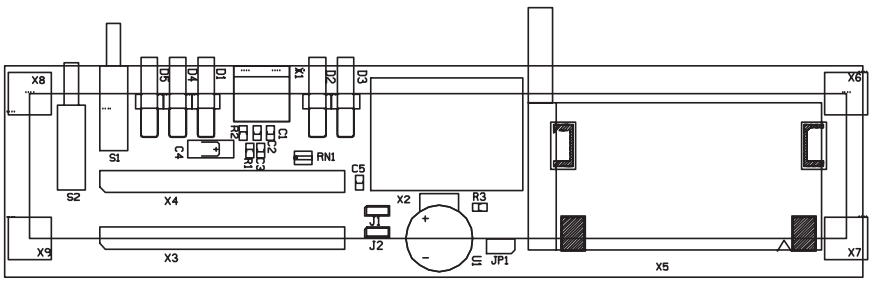


Figure 44: Component Placement Diagram Expansion Board

23 Revision History

Date	Version numbers	Changes in this manual
June 2005	Manual L-668e_0 PCM-990 PCB# 1220.2 PCM-985 PCB# 1222.1	First preliminary edition.
February-2006	Manual L-668e_1 PCM-990 PCB# 1220.3 PCM-985 PCB# 1222.1	Revision due to PCB revision change. *Section Quick Capture Interface* added.

Index

Document: Carrier Board for phyCORE-PXA270
Document number: L-668e_1, February 2006

How would you improve this manual?

Did you find any mistakes in this manual? page

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Return to: PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

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