Development Board for phyCORE-PXA255

Hardware Manual

PCB# 1220.1 and 1220.2

Edition November 2004

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Preface

This manual describes only the functions of the PHYTEC phyCORE-PXA255 Development Board. The controllers and relevant Single Board Computers for use with the Development Board are not described herein. Additional controller- and board-level information and technical descriptions can be found in appropriate Hardware Manual or User's Manual support documentation. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the phyCORE-PXA255 Development Board

CE

PHYTEC Development Boards (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

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The phyCORE-PXA255 Development Board is one of a series of PHYTEC Development Boards supporting the phyCORE-PXA255 Single Board Computer module. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The Development Board phyCORE-PXA255 is a universal carrier board for start-up and programming of the PHYTEC phyCORE-PXA255 Single Board Computer module with two high density SMT (160 pins each, 0.63 mm pitch) pin header connectors. The Development Board is fully equipped with all mechanical and electrical components necessary for the speedy and secure insertion and subsequent programming of the high-density PHYTEC phyCORE module. These components include TFT display connection, touch screen interface, Ethernet transformer and connector, DB-9, USB and power socket connectors.

The phyCORE module can be plugged like a "big chip" onto the Development Board's mating Molex connectors. Once programmed, the phyCORE module can be removed from the Development Board and inserted like a "big chip" in a target hardware application. Given the compact nature of the Development Board use of the complete hardware platform as OEM part in human-machine-interface (HMI) applications is also possible.

The hardware manual for this Development Board does not describe the features and functions of the phyCORE-PXA255 SBC module, as this is not relevant for the basic functioning of the Development Board. For module and controller-specific features *please refer to the corresponding Hardware Manuals/User's Manuals*.

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The Development Board offers the following features:

- Molex connectors for mating with phyCORE-PXA255 SBC module
- Connector for 8.4" Sharp TFT display with 640*480 pixel resolution, incl. adjustable inverter for background illumination
- AC97 controller WM9712L with touch and sound interface (Line-IN, Line-OUT, MIC-IN and 0.4 watts speaker)
- Two DB-9 sockets for RS-232 interface from FF-UART and BT-UART, 2*5 pin header for IR-UART
- One DB-9 plug for CAN interface, optical isolation
- RJ-45 Ethernet connector with transformer for 100/10 MBit/s
- USB host interface circuitry supporting the USB-OTG controller on the phyCORE-PXA255
- USB client socket for PXA255 USB client interface
- Power supply for unregulated input voltage from 8 V to 24 V (standard 12V). It supplies regulated +3.3 V for the phyCORE-PXA255. Additional +5 V is created for the IDE and CF card and LCD/inverter circuitry.
- Optional battery charger circuitry for NiMH batteries
- Power magement for MMC, CF, IDE and LC display
- Two user programmable LEDs
- Optional IDE interface for two 2.5" hard disks (Master / Slave)
- Interface for Matrix keyboards
- JTAG interface
- AC97 expansion port
- Reset and GPIO push button

Expansion Board with:

- 1* MultiMedia card
- 1* Compact Flash
- 1* Reset button
- 1* GPIO button
- 1* USB-OTG socket for ISP1362 USB interface
- 4* LEDs via PLD GPIOs

- **PXA255 Operating Systems Kits:**

- Linux
- WinCE

- **phyCORE-PXA255 Debugging Systems:**

- iSYSTEM iC3000 Active Emulator™

1.1 Block Diagram

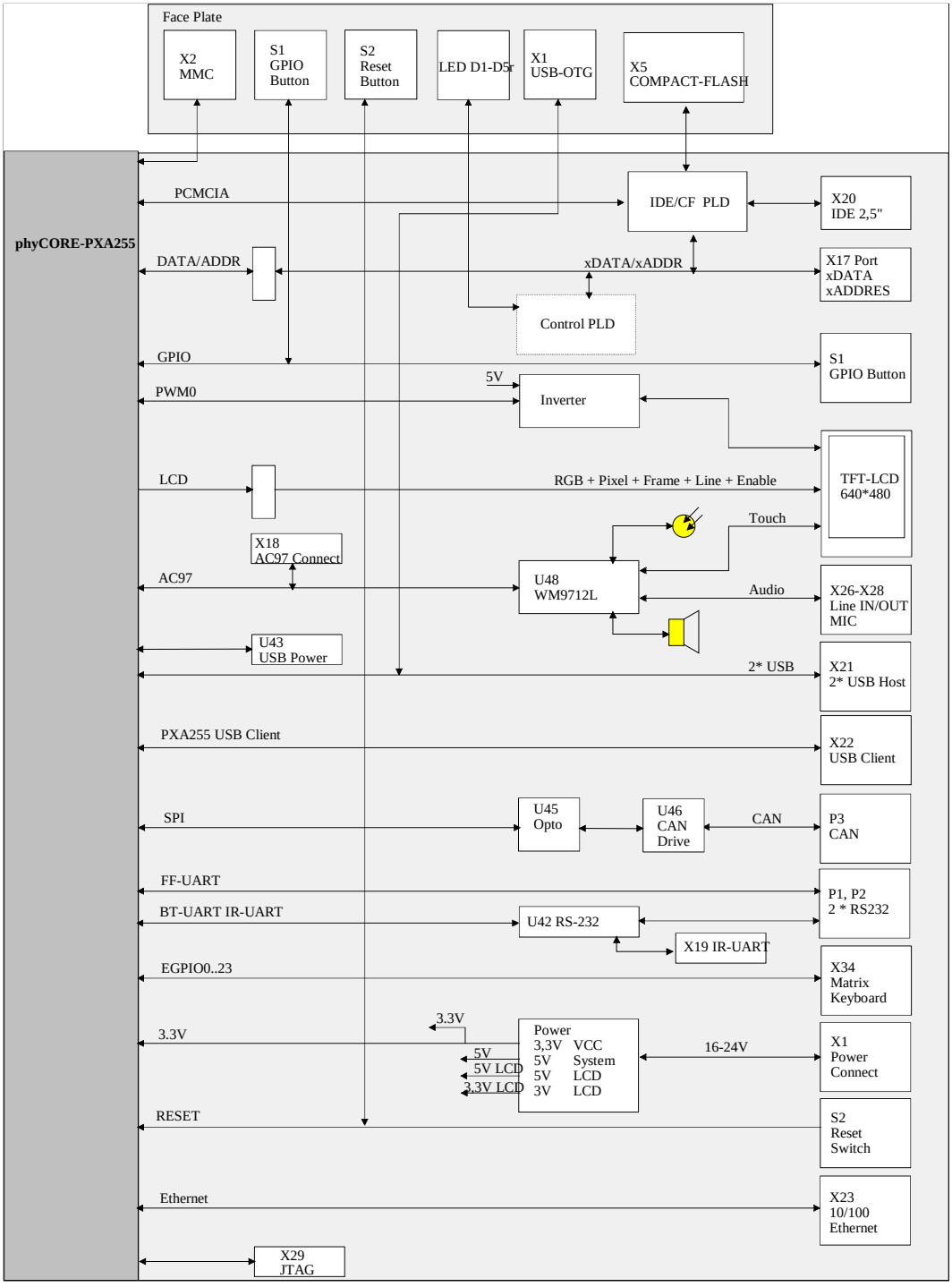


Figure 1: Block Diagram of the Development Board

1.2 Overview

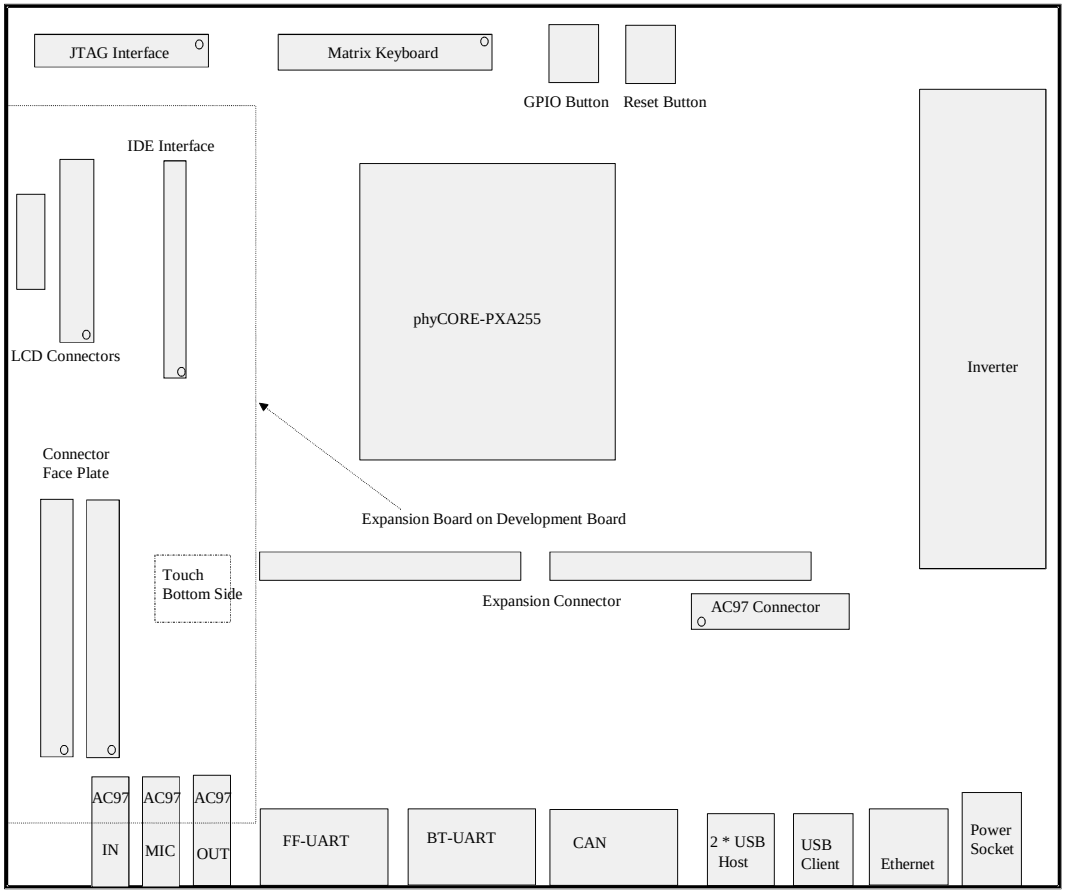


Figure 2: Development Board Overview (Top View)

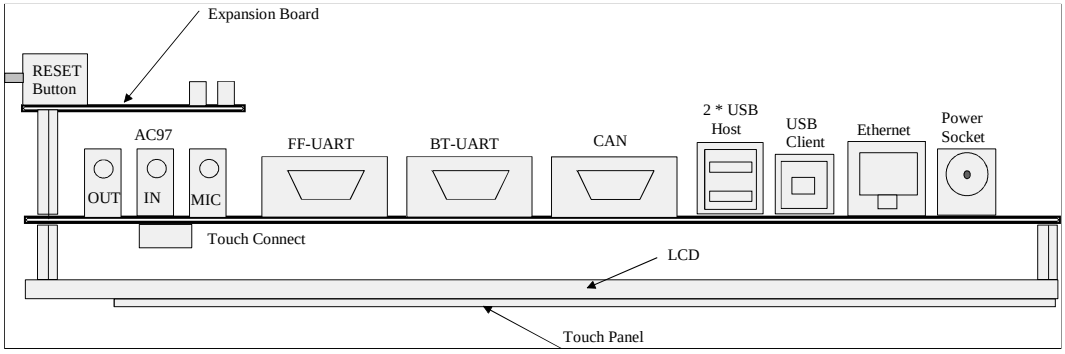


Figure 3: Development Board Overview (Connector Side View)

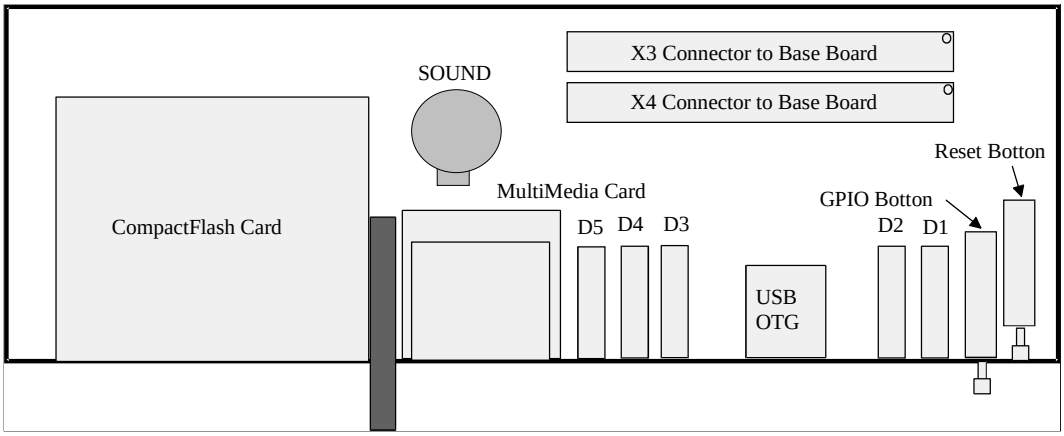


Figure 4: Expansion Board Overview (Top View)

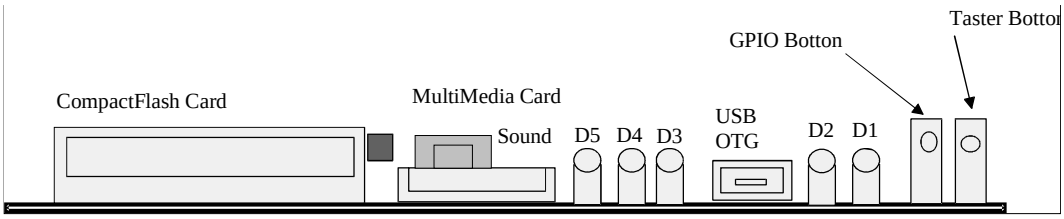


Figure 5: Expansion Board Overview (Side View)

2 Port Pin Initialization

The Intel PXA255 controller provides a wide variety of chip-level features that are routed to GPIO pins with alternative functions. The following functions are used on the phyCORE-PXA255 Development Board:

- MMC Card 0/1
- PCMCIA interface
- 16-bit LCD interface
- AC97 interface
- FF-UART, BT-UART and IR-UART
- SSP and NSSP
- I²C bus

Either the operating system installed on the phyCORE-PXA255 or the boot loader (e.g. U-Boot) must initialize the port pins in questions as shown in the table below:

Port	**I/O**	**Configuration**
GPIO0	I	GPIO0 as interrupt for RTC
GPIO1	I	GPIO1 as interrupt/wake-up for push botton S1
GPIO2	I	GPIO2 as Ethernet interrupt
GPIO3	I	GPIO3 as interrupt 1 for ISP1362 USB controller
GPIO4	I	GPIO3 as interrupt 2 for ISP1362 USB controller
GPIO5	I	GPIO5 as interrupt for MCP2515 CAN controller
GPIO6	O	MMCCLK
GPIO7	I	GPIO7 as interrupt for Control PLD
GPIO8	O	MMCCS0
GPIO9	O	MMCCS1
GPIO10	I	GPIO10 as interrupt for AC97 controller
GPIO11	I	GPIO11 as interrupt for IDE interface
GPIO12	I	GPIO12 as PEN interrupt for AC97 controller
GPIO13	I	GPIO13 as CF card interrupt
GPIO14	I	GPIO14 as interrupt for CF card CD signals
GPIO15	O	/CS1 free
GPIO16	O	PWM0 as output for inverter enable (adjusting the LCD background illumination)

GPIO17	O	PWM1 as clock signal
GPIO18	I	Controller READY inut
GPIO19	I	DREQ0
GPIO20	I	DREQ1
GPIO21	I	GPIO21 output for RUN LED
GPIO22	I	GPIO22 output for BUSY LED
GPIO23	I	SSPCLK SSP clock for EGPIO
GPIO24	I	SFRM SPI FRAME signal as /CS_EGPIO (MAX7301)
GPIO25	O	SSP TxD line for EGPIO expander
GPIO26	I	SSP RxD line for EGPIO expander
GPIO27	I	SSP EXTCLK as interrupt for EGPIO expander
GPIO28	O	AC97 BitCLK
GPIO29	I	AC97 SDATA_IN0
GPIO30	O	AC97 SDATA_OUT
GPIO31	O	AC97 SYNC
GPIO32	I	AC97 SDATA_IN1
GPIO33	O	/CS5 32-bit VLIO for Ethernet controller
GPIO34	I	FF-UART RxD
GPIO35	I	FF-UART CTS
GPIO36	I	FF-UART DCD
GPIO37	I	FF-UART DSR
GPIO38	I	FF-UART RI
GPIO39	O	FF-UART TxD

Table 1: Port Configuration GPIO0-39

Port	**I/O**	**Configuration**
GPIO40	O	FF-UART DTR
GPIO41	O	FF-UART RTS
GPIO42	I	BT-UART RxD
GPIO43	O	BT-UART TxD
GPIO44	I	BT-UART CTS
GPIO45	O	BT-UART RTS
GPIO46	I	IR-UARTRxD
GPIO47	O	IR-UARTTxD
GPIO48	O	/POE PCMCIA
GPIO49	O	/PWE PCMCIA
GPIO50	O	/PIOR PCMCIA
GPIO51	O	/PIOW PCMCIA
GPIO52	O	/PCE1 PCMCIA
GPIO53	O	/PCE2 PCMCIA
GPIO54	O	/PKSEL PCMCIA (for selecting the two PCMCIA cards)

GPIO55	O	/PREG PCMCIA
GPIO56	I	/PWAIT PCMCIA
GPIO57	I	/IOIS16 PCMCIA
GPIO58	O	LDD0 data bus for LCD
GPIO59	O	LDD1 data bus for LCD
GPIO60	O	LDD2 data bus for LCD
GPIO61	O	LDD3 data bus for LCD
GPIO62	O	LDD4 data bus for LCD
GPIO63	O	LDD5 data bus for LCD
GPIO64	O	LDD6 data bus for LCD
GPIO65	O	LDD7 data bus for LCD
GPIO66	O	LDD8 data bus for LCD
GPIO67	O	LDD9 data bus for LCD
GPIO68	O	LDD10 data bus for LCD
GPIO69	O	LDD11 data bus for LCD
GPIO70	O	LDD12 data bus for LCD
GPIO71	O	LDD13 data bus for LCD
GPIO72	O	LDD14 data bus for LCD
GPIO73	O	LDD15 data bus for LCD
GPIO74	O	LCD_FCLK frame clock
GPIO75	O	LCD_LCLK line clock
GPIO76	O	LCD_PCLK pixel clock
GPIO77	O	LCD_ACBIAS BIAS / LCD_Enable
GPIO78	O	/CS2 free
GPIO79	O	/CS3 16-bit VLIO for PLD
GPIO80	O	/CS4 16-bit VLIO for ISP1362 USB Controller
GPIO81	O	NSSP-CLK for CAN
GPIO82	O	NSSP-FRAM as /CS_CAN (MPC2515)
GPIO83	O	NSSP-TXD for CAN
GPIO84	I	NSSP-RXD for CAN

Table 2: Port Configuration GPIO40-84

3 Jumpers

For configuration purposes, the phyCORE-PXA255 Development Board has 7 removable and 8 solder jumpers, most of which have been installed prior to delivery depending on the board's configuration. Solder jumpers should not be changed by the user. *Figure 6* illustrates the numbering of the jumper pads, while *Figure 7* indicates the location of the jumpers on the board.

Figure 6: Numbering of the Jumper Pads

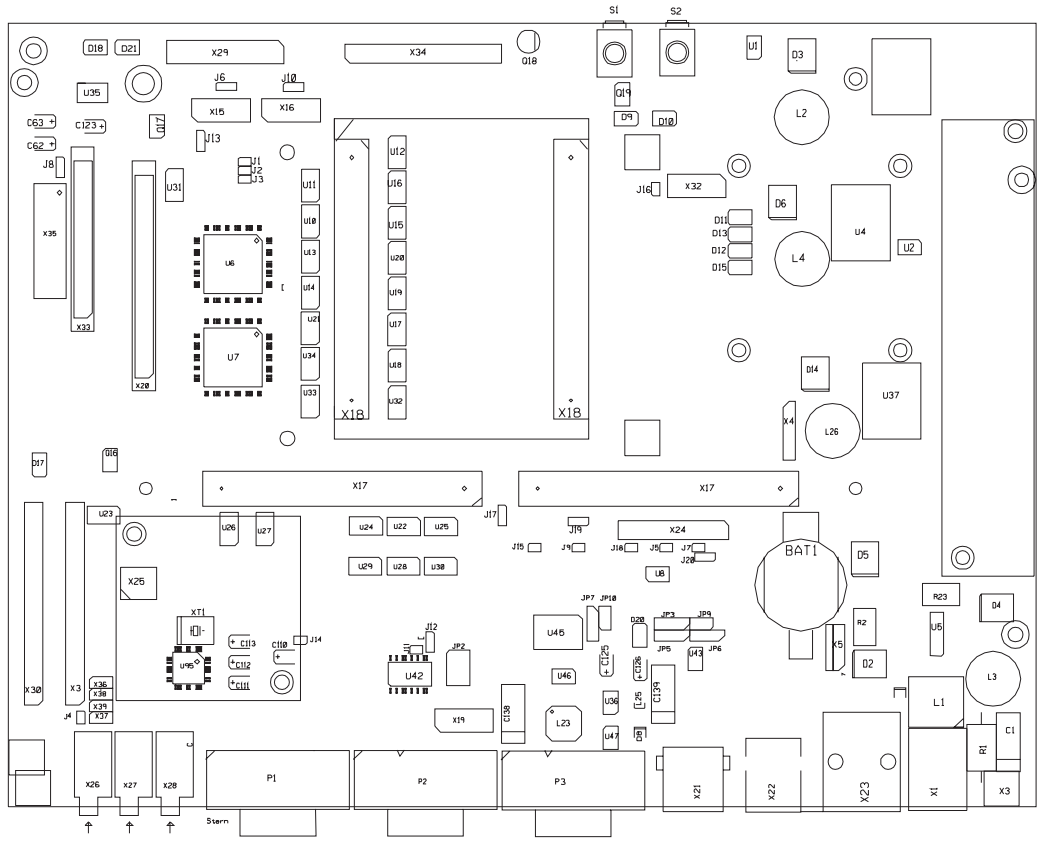


Figure 7: Location of the Jumpers (Development Board)

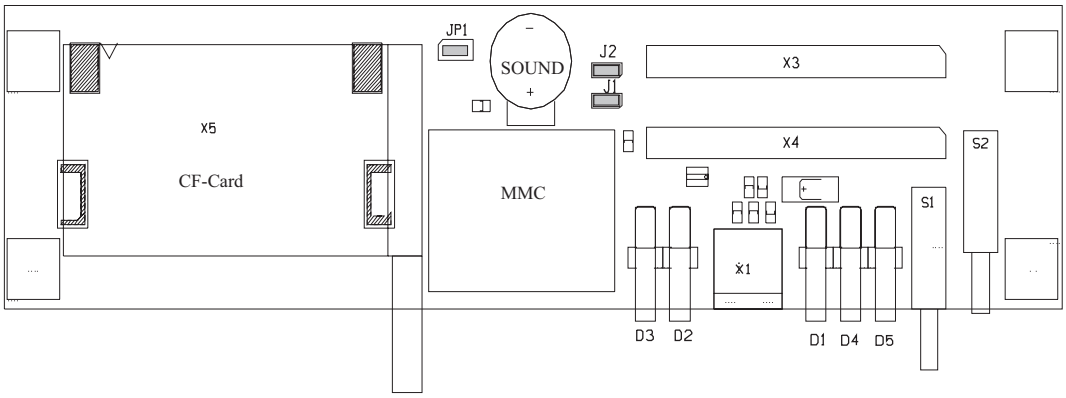


Figure 8: Location of the Jumpers (Expansion Board)

Description of the jumper functions is provided in the following manual sections. The jumpers are grouped by function as follows:

Jumper	**Function/Section**
JP3, JP5, JP6, JP9	USB host Interface, *refer to section 7*
JP7, JP10	CAN Interface, refer to section
JP2	RS-232 Transceiver BT-UART and IR-UART, *refer to section 10*

Table 3: Jumper Functions and Section Reference

4 Power Supply System

The Development Board functions with a supply voltage of 8 VDC to 24 VDC. The on-board voltage converters generate all supply voltages required for the components on the Development Board, the Expansion Board and the phyCORE-PXA255. The supply voltage can also be used for the optional battery charger circuitry.

Supply voltage 1: +3.3 V (VCC)
Supply voltage 2: +5 V (DIE and CF card)
Supply voltage 3: +5 V (LCD and inverter)

Supply voltage 1: +3.3 V (VCC)

Nearly all of the components on the Development Board, the Expansion Board and the phyCORE-PXA255 are powered by VCC (+3.3 V). The supply voltages for the CompactFlash Card and the Multimedia Card on the Expansion Board can be switched with the help of transistors. The voltage converter allows for a maximum current draw of 2 amps at 3.3 V (+/-5 %). The efficiency of the converter is over 80 %.

Supply voltage 2: +5 V (IDE and CF card)

The 5 V supply voltage is intended only for the 2.5" hard drive and the CF card. It can be switched on or off during operation. The voltage converter allows for a maximum current draw of 2 amps at 5 V (+/- 5 %). The efficiency of the regulator is over 80 %.

Supply voltage 3: +5 V (LCD and inverter)

The inverter for the LCD background lighting is powered by this 5 V supply voltage. The PXA255 switches the background lighting on and off or dims it over its PWM0 signal. A linear voltage regulator is used to generate the 3.3 V LCD logic supply voltage from the 5 V LCD. The voltage converter allows for a maximum current draw of 1.5 amps at 5 V (+/- 5 %). The efficiency of the regulator is over 80 %.

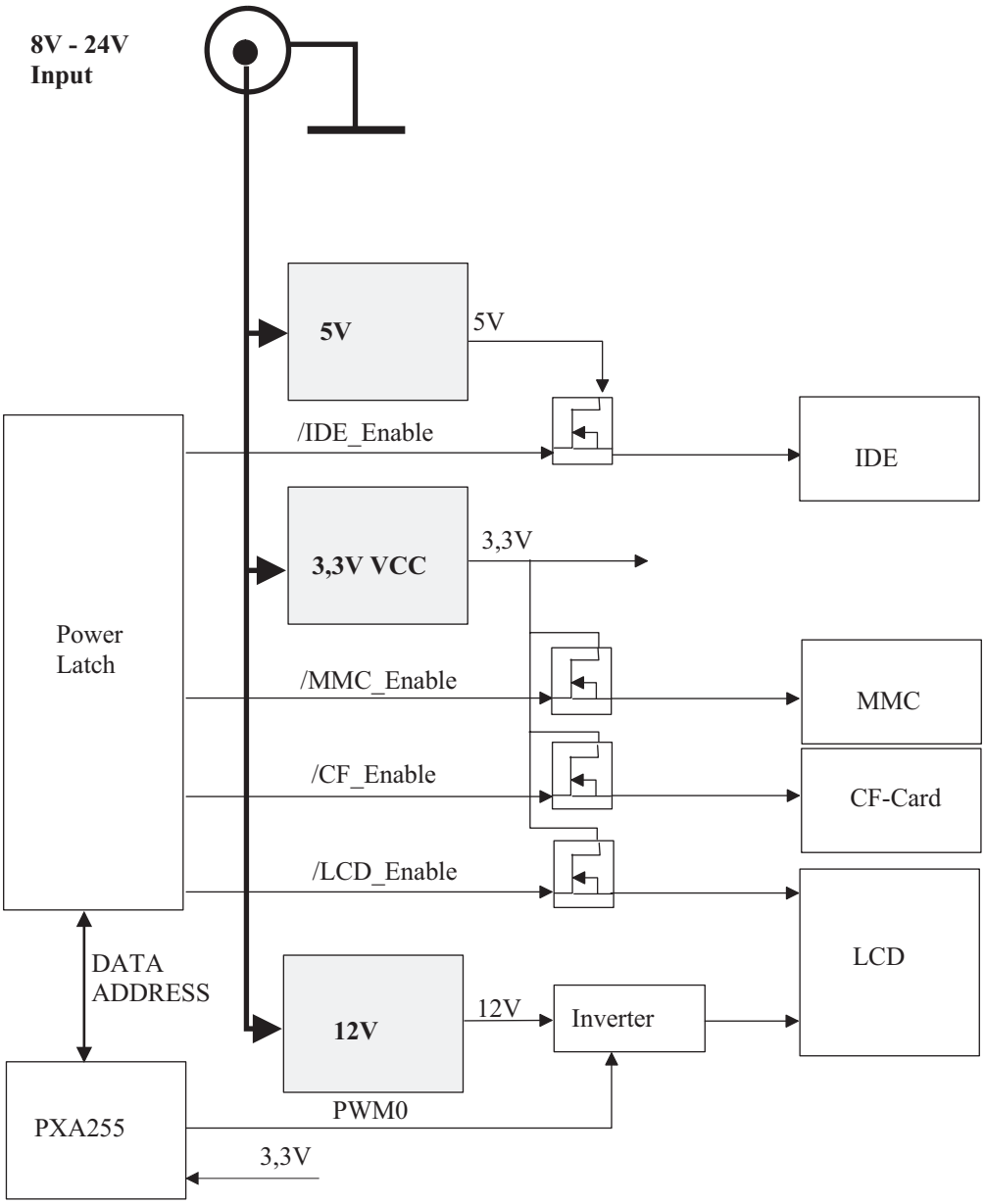


Figure 9: Power Supply Block Diagram

Battery Charger Circuitry for 6 NiMH Batteries

The Development Board can be populated with an optional battery charger circuit for six (when using a 12 V input voltage) (up to 12 possible, requires different hardware configuration and 24 V input voltage) NiMH batteries. In this case the BQ24703 battery charge controller switches the voltage from the power adapter to battery operation. It will charge the batteries when the Development Board is supplied with voltage by a wall adapter.

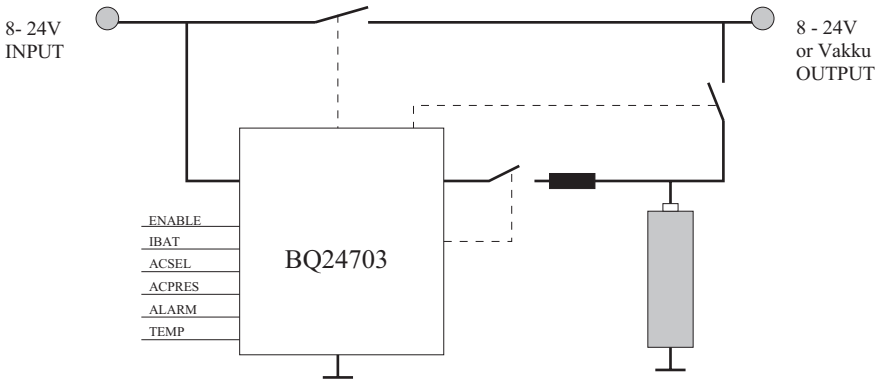


Figure 10: Battery Charger Circuitry

Note:
The battery charger register is only available with PCB revision 1220.2 and higher.

5 Memory Configuration

The Development Board for the phyCORE-PXA255 uses the /CS signals /CS2 and /CS3 as well as the PCMCIA interface for controlling the components on the data bus. The other /CS signals on the phyCORE-PXA255 are controlled by the address decoder (control PLD U7) in order to connect the data bus driver. The PCMCIA interface is managed by the second address decoder (Control PLD U6), which generates all necessary signals for the CF card and the IDE interface.

/CS0	2 * 16-bit Flash memory 16 to 64 MByte asynchronous / synchronous (optional 16-bit Flash memory 8 MByte asynchronous)
/CS1	free (pre-configured 16-bit asynchronous ROM/RAM)
/CS2	16-bit VLIO interface, expansion connector X17 on the Development Board
/CS3	16-bit VLIO interface, address decoder U7 on the Development Board
/CS4	USB host with 16-bit VLIO interface on th phyCORE-PXA255 module
/CS5	Ethernet chip with 32-bit VLIO interface on the phyCORE-PXA255 module

The SDRAM /CS signals extend to the Development Board (X23) but are not used. Depending on the phyCORE-PXA255 configuration option, these /CS signals /SDCS_0 through /SDCS_3 are connected with the chips of both SDRAM banks.

/SDCS_0	64 MB 2*16-bit SDRAM on the phyCORE-PXA255
/SDCS_1	optional 64 MB 2*16-bit SDRAM on the phyCORE-PXA255
/SDCS0/1	optional 128 MB 2*16-bit SDRAM on the phyCORE-PXA255
/SDCS2/3	optional 128 MB 2*16-bit SDRAM on the phyCORE-PXA255

5.1 Interrupts

The interrupt signals of the components on the phyCORE-PXA255 are configured on the phyCORE module itself. Because of the limited number of available GPIOs, the functions /MMC_DET and MMC-WP cannot be connected to GPIO7 and GPIO10 on the phyCORE module. The interrupt inputs /PLD_INT for power management functions and AC_INT from the AC97 Codec are implemented on the Development Board.

GPIO	Signal	Description
GPIO0	/RTC_INT	Low active interrupt RTC-8564
GPIO2	LAN_IRQ	High active interrupt for LAN91C11 Ethernet controller
GPIO3	/OTG_INT1	Low active interrupt 1 for ISP1362 USB controller
GPIO4	/OTG_INT2	Low active interrupt 2 for ISP1362 USB controller
GPIO5	/CAN_INT	Low active interrupt for MCP2515 CAN controller
GPIO27	EGPIO27	Low active interrupt for MAX7301 matrix keyboard

Table 4: Interrupt Assignment phyCORE-PXA255

On the Development Board interrupts are used for the CF card, IDE interface, AC97, touch and power management circuits. These are either hard-wired over solder jumpers or managed in the two address decoders.

GPIO	Signal	Description
GPIO7	/PLD_INT	Low active interrupt for power management
GPIO10	AC_INT	High active interrupt for WML9712 AC97 controller
GPIO11	IDE_IRQ	High active interrupt for IDE drive
GPIO12	/CF_IRQ	Low active interrupt /CD1 and /CD2 CF card. Support of hot-plugging CF cards; an interrupt is released each time a card is inserted ot removed, only available with PCB revision 1220.2 and higher.
GPIO13	CF_IRQ	High active interrupt CF card. The active level of an interrupt depends on the card type (memory, TrueIDE, etc.) With TrueIDE cards the level is active high.

Table 5: Interrupt Assignment Development Board

5.2 Control PLD (U6)

Control PLD U6 controls the drivers for the buffered data and the address bus. Furthermore, all power management, control and interrupt functions, except for the CF card and the IDE interface are contained as well. The individual functions will be explained in greater detail in the register description.

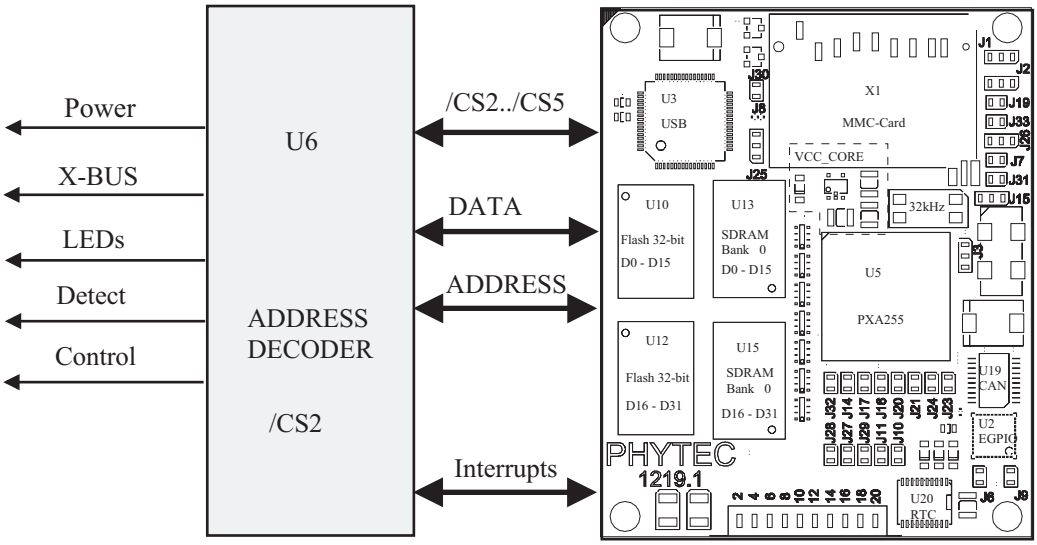


Figure 11: Control PLD U6

5.2.1 Control PLD (U6) Registers

Control PLD U6 is addressed over the PXA255's Chip Select signal /CS_3. The bus width is set to 16-bit as a VLIO interface. The registers of the Control PLD are listed in the following table. The register's reset value after the system start is shown below the description.

REG	ADDR.	D7-D4	D3	D2	D1	D0
CTRL0 RESET	0x0c000000	Res	Res	GPIO0 0	RESOUT 0	SRES 0
CTRL 1 RESET	0x0c000002	Res	PM_5V X	CANPWR 0	Res	5V_OFF 0
CTRL 2 RESET	0x0c000004	Res	Res	LEDBAS 0	LEDUSR 0	LEDPWR 0
CTRL 3 RESET	0x0c000006	Res	POS1 0	POS2 0	LCDON 0	LCDPWR 0
CTRL 4 RESET	0x0c000008	Res	Res	Res	Res	MMC1PWR 0
CTRL 5 RESET	0x0c00000A	Res	WP	DET	LED	MMC2PWR
CTRL 6 RESET	0x0c00000C	Res	INT3 0	INT2 0	INT1 0	INT0 0
CTRL 7 RESET	0x0c00000E	Res	INT PM_5V 0	INT MMCDET 0	INT FF_RI 0	INT BT_DET 0
CTRL 8 RESET	0x0c000010	Res	BT_Rx	FF_RI	BT_SD 0	FF_SD 0
CTRL 9 RESET	0x0c000012	Res	Res	AC97 ENA 0	/FL_DIS 0	FL_WP 1
CTRL 10 RESET	0x0c000014	Res	Res	Res	Res	Res
CTRL 11 RESET	0x0c000016	Res	ALARM	ACPRES	ACSEL 0	ACENA 0

Table 6: Control PLD U6 Reset Values

The reset properties for RES_DEV on the Development Board are set in control register 0. RES_DEV is the reset signal that only affects the USB, CAN and Ethernet controller of the phyCORE-PXA255. Therefore it is possible to use the RESETOUT of the PXA255 controller in watchdog mode without having to reinitialize these controllers.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL0 RW	0x0c000000	Res R/W=0	Res R/W=0	GPIO0 R/W	RESOUT R/W	SRES R/W

Table 7: PLD U6 Control Register 0

SRES Setting this bit generates a system reset.

RESOUT If this bit is set and RESETOUT = 0 on the PXA255, then a RES_DEV will be generated.

GPIO0 If this bit is set and GPIO0 = 0 on the PXA255, then a RES_DEV will be generated.

PLD U6 control register 1 is used for switching and controlling various supply voltages. The bit PM_5V displays whether the 5 V voltage is still active or if it was shut off due to a wall adapter output voltage drop to less than 8 V. If 5V_OFF is set, the 5 V supply can be shut off independently of the input voltage level. The external CAN supply voltage can be switched on with the CANPWR bit.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL1	0x0c000002	Res	PM_5V	CANPWR	Res	5V_OFF
RW		R/W=0	R	R/W	R/W=0	R/W

Table 8: PLD U6 Control Register 1

5V_OFF Turns off the 5 V supply (bit set).
CANPWR Turns on the external CAN supply voltage (bit set).
PM_5V Indicates that 5 V supply voltage is active.

The registers for controlling the Development Board's user LEDs D11, D12 and D15 are in control register 2 of U6. The register values are negated by the PLD so that the LEDs can be switched with a high-active level. The LEDs are located to the right of the phyCORE module.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL2	0x0c000004	Res	Res	LEDBAS	LEDUSR	LEDPWR
RW		R/W=0	R/W=0	R/W	R/W	R/W

Table 9: PLD U6 Control Register 2

LEDPWR Setting this bit will turn on user LED D11.
LEDUSR Setting this bit will turn on user LED D12.
LEDBAS Setting this bit will turn on user LED D15.

The voltage settings and the adjustment of the TFT display can be carried out in control register 3. The bit POS1 is connected to the R/L signal of the display while POS2 is connected to the display's U/D signal. The data line drivers can be switched to active with LCD_ON. The supply voltage of the LCD is switched on with LCDPWR.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 3	0x0c000006	Res	POS1	POS2	LCDON	LCDPWR
RW		R/W=0	R/W	R/W	R/W	R/W

Table 10: PLD U6 Control Register 3

POS1/POS2 The display adjustment is set here. The display can be mirrored in the X direction as well as the Y direction with these two bits. If both bits are changed at the same time, then the image will be rotated in an 180 degree angle.

LCDON With a "1" (high level) the driver circuits for the LCD data and control bus are switched active connected.

LCDPWR Setting this bit turns on the supply voltage for the TFT display.

Control register 4 controls the external supply voltage MultiMediaCard 1 on the phyCORE-PXA255.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 4	0x0c000008	Res	Res	Res	Res	MMC1PWR
RW		R/W=0	R/W=0	R/W=0	R/W=0	R/W

Table 11: PLD U6 Control Register 4

MMC1PWR Setting this bit turns on the supply voltage for the MMC card 1.

Control register 5 is reserved for MultiMediaCard2. Here the supply voltage can be switched on and the access LED can be activated. The register bits WP and DET return the card status.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 5	0x0c00000A	Res	WP	DET	LED	MMC2PWR
RW		R/W=0	R	R	R/W	R/W

Table 12: PLD U6 Control Register 5

MMC2PWR Setting this bit turns on the supply voltage for the MMC card 2.

LED Setting this bit turns on the access indication LED for then MMC card on the Expansion Board.

DET If a MMC card is inserted in the socket then reading this bit returns a "0", otherwise it is set to "1".

WP If a MMC card is inserted in the socket that is write protected then reading this bit returns a "0", otherwise it is set to "1".

Control registers 6 and 7 contain the interrupt sources for the interrupt input GPIO_7. In control register 6 the register bits are deleted by an interrupt. If one of the 4 bits is 0 then a high-active interrupt is generated on GPIO_7. The value 0xFF has to be written to this control register after the interrupt has been serviced in order to allow another interrupt. The interrupt control register 7 is used to free individual interrupt inputs. If the current bit is set to 1, the interrupt causes the bits in control register 6 to be deleted, otherwise this will not occur. The interrupt sources correspond to the designations of control register 7.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 6	0x0c00000C	Res	INT3	INT2	INT1	INT0
RW		R/W=0	R/W	R/W	R/W	R/W
CTRL 7	0x0c00000E	Res	INT PM_5V	INT MMCDET	INT FF_RI	INT BT_DET
RW		R/W=0	R/W	R/W	R/W	R/W

Table 13: PLD U6 Control Registers 6 and 7

INT0 IRQ status bit for BT-UART detect
INT1 IRQ status bit for FF-UART detect
INT2 IRQ status bit for MMC-Card 2 detect
INT3 IRQ status bit for 5 V power not present

Clear bit = interrrupt active if one of the four bit = 0 => /INT0-BIT

INT_BT_DET Enable bit for BT-UART detect
INT_FF_DET Enable bit for FF-UART detect
INT_MMCDET Enable bit for MMC card 2 detect
INT_PM5V Enable bit for 5 V power not present

Only if the corresponding bit is set to "1", then an interrupt will erase the "clear bit" and hence release an interrupt.

Control register 8 controls the RS-232 transceiver for the BT/IR UART and the FF-UART.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 8	0x0c000010	Res	BT_Rx	FF_RI	BT_SD	FF_SD
RW		R/W=0	R	R	R/W	R/W

Table 14: PLD U6 Control Register 8

FF-SD Setting this bit shuts down the RS-232 transceiver for the FF-UART.
BT-SD Setting this bit shuts down the RS-232 transceiver for the BT-UART and IR-UART.
FF_RI If the RS-232 transceiver for the FF-UART is in power down mode then this bit returns an active RI signal.
BT_Rx If the RS-232 transceiver for the BT-UART or IR-UART is in power down mode then this bit returns an active RxD signal.

The Flash device on the phyCORE module and the AC97 expansion interface can be configured in control register 9. If /FL_DIS is set to 0, then it is possible to boot from an external Flash (not on the phyCORE-PXA255).

However it is important to be aware of the bus configuration on the phyCORE module. When setting the bit FL_WP the Flash will be write-protected with WP.

AC97ENA is an output that extends to the expansion socket of the AC97 interface. This is provided so that the expansion circuitry supply voltage can be turned off or switched to power down mode. The connections have to be made on the AC97 expansion board. *Refer to section 12 for more details on this AC97 expansion connector.*

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 9	0x0c000012	Res	Res	AC97 ENA	/FL_DIS	FL_WP
RW		R/W=0	R/W=0	R/W	R/W	R/W

Table 15: PLD U6 Control Register 9

FL_WP Setting this bit disables writing the on-board Flash on the phyCORE-PXA255.

/FL_DIS This bit can be used to disable the on-board Flash on the phyCORE-PXA255. This bit is active low

AC97_ENA This bit controls an output signal routed to the AC97 expansion connector. It can be used to turn the supply voltage for an AC97 module connected to X24 on or off.

Control register 10 of the PLD U6 ist not supported in the current version of the Development Board. This register is reserved for future use.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 10	0x0c000014	Res	Res	Res	Res	Res
RW		R/W=0	R/W=0	R/W=0	R/W=0	R/W=0

Table 16: PLD U6 Control Register 10

The optional battery charger circuitry is configured with control register 11.

Note:
The battery charger register is only available with PCB revision 1220.2 and higher.

REG	ADDR	D7-D4	D3	D2	D1	D0
CTRL 11	0x0c000016	Res	ALARM	ACPRES	ACSEL	ACENA
RW		R/W=0	R	R	R/W	R/W

Table 17: PLD U6 Control Register 11

ACENA Setting this bit turns on the battery charger controller.

ACSEL This bit selects the source of the board's power supply, "1" specifies supply via DC adapter, "0" via battery.

ACPRES Reading a "1" from this input indicates that a DC adapter is currently connected to the board.

ALARM This bit returns the alarm status information of the battery charger controller.

5.2.2 External Data and Address Bus

The data and address bus on the phyCORE-PXA255 operates with a clock frequency of 100 MHz, therefore it must be decoupled for external use. All components on the Development Board except the Control PLD are connected to the decoupled data and address bus. The driver ICs are controlled by the PLD at U6 depending on the state of the current Chip Select signal.

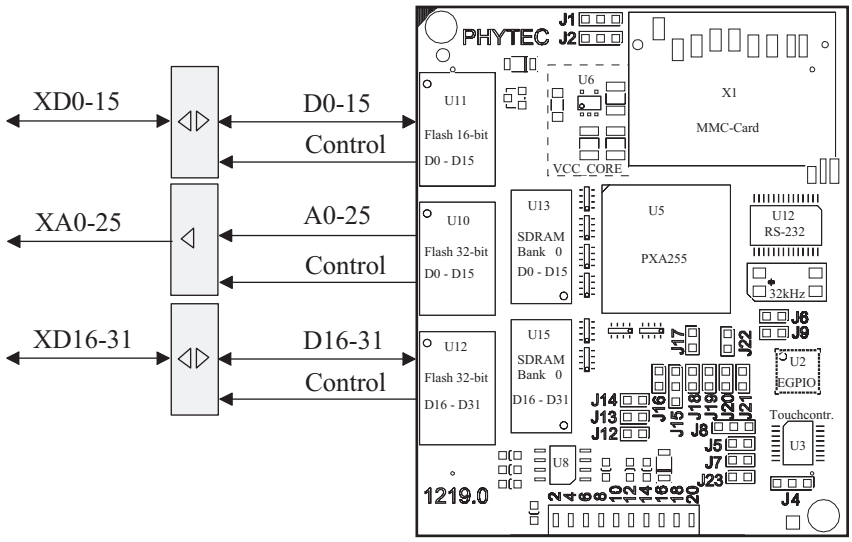


Figure 12: Decoupling the Data and Address Bus

5.3 IDE Interface and CF Card PLD (U7)

The phyCORE-PXA255 provides a PCMCIA interface that supports two independent PCMCIA sockets. The first socket is available on the Development Board as an IDE interface, the second interface extends as a CF card socket to the Expansion Board. The PLD U7 is provided for controlling the additional functions such as TruIDE mode, power and others.

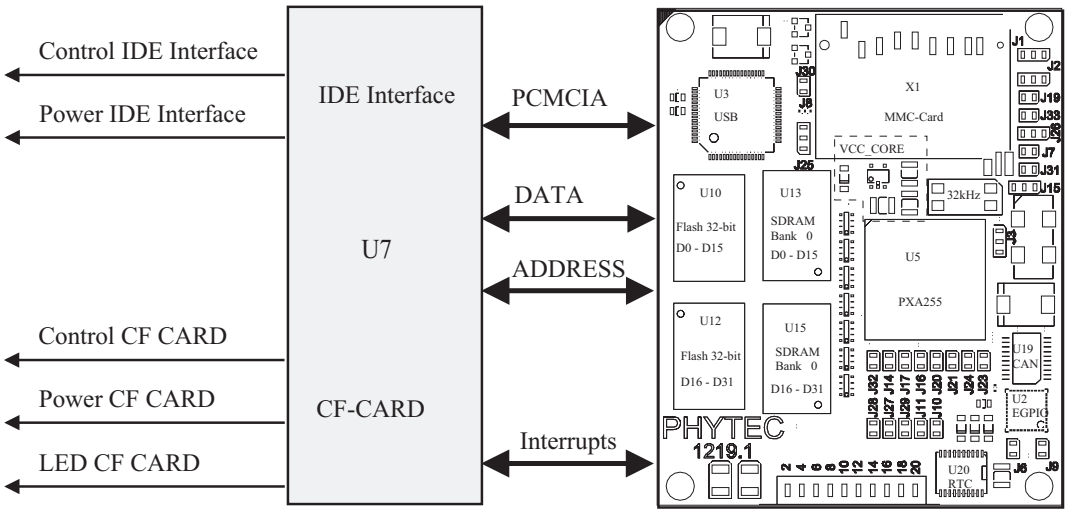


Figure 13: CF Card and IDE PLD U7

5.3.1 IDE Interface

The PXA255 controller's first PCMCIA interface is used on the Development Board to realize an IDE socket for 2.5" hard drives. PLD U7 provides all the control logic to operate the IDE interface and the 2.0 mm header connector is located at X20 on the Development Board. Mounting holes for attaching the hard drive are located on the Development Board. The hard disk will be attached to the board using spacers above of the phyCORE-PXA255 module *(refer to Figure 14 for details)*.

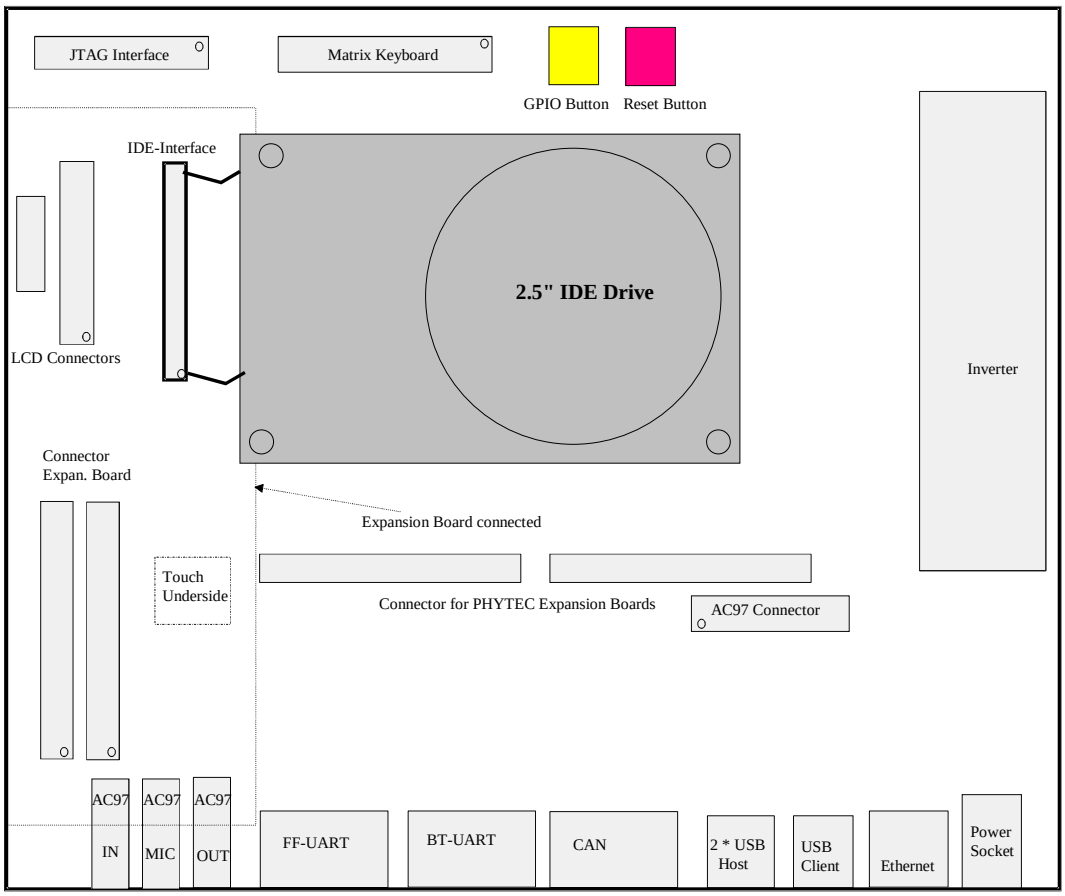


Figure 14: IDE Hard Drive Mounting Location

The hard drive, running on 5 V, is decoupled from the buffered data and address bus on the Development Board with 74LVC245 line driver ICs.

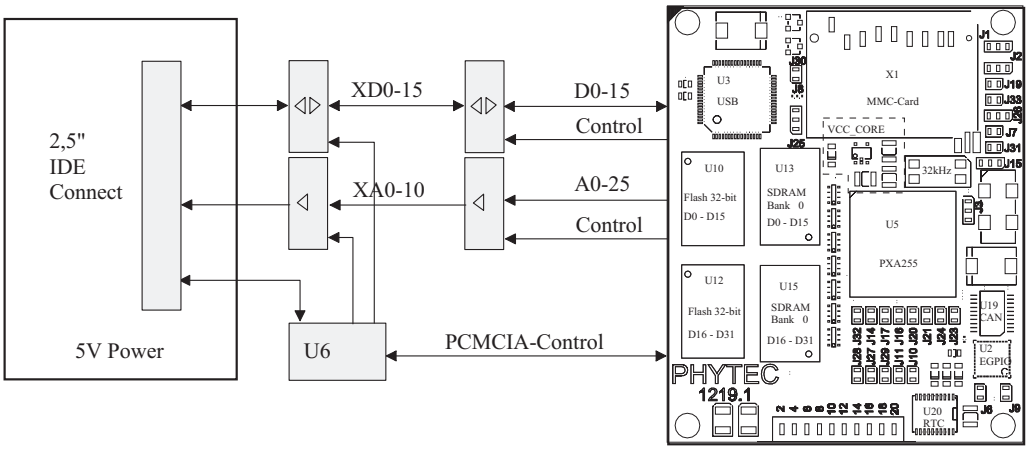


Figure 15: IDE Circuitry

The PCMCIA interface settings are made in the PXA255 controller. The IDE register of the PLD U7 along with their reset values are given in the following table.

REG	ADDR	D7	D3	D2	D1	D0
IDE 0 Reset	0x2001000	Res	Res	PM_5V X	RES	RES
IDE 1 Reset	0x2001002	Res	DMA0/1 0	DMAEN 0	RES	IDE/MEM 0
IDE 2 Reset	0x2001004	Res	RDY 0	Res	/IDE_RES 0	Res
IDE 3 Reset	0x2001006	Res	Res	IDEIN 0	IDEON 0	IDEOE 0
IDE 4 Reset	0x2001008	Res	IDE5V x	RES	5V/3V 1	IDEPWR 0

Table 18: IDE Control Register with Reset Values

The operating states of the 5 V supply voltage can be read in the IDE control register 0. If the Development Board's input voltage drops below 8 V, the 5 V supply voltage will be shut off.

REG	ADDR	D7	D3	D2	D1	D0
IDE 0	0x2001000	Res	Res	PM_5V	RES	RES
RW		R/W=0	R/W=0	R	R/W=0	R/W=0

Table 19: IDE Control Register 0

PM_5V Reading a "1" from this input indicates that the 5 V supply voltage des System und des LCD aktiv

IDE control register 1 is used to set the memory interface and the DMA access. Since a hard drive only supports the TruIDE mode of a CF card interface, this has a fixed setting in register bit 0. The PXA255 controller's PCMCIA interface does not support TruIDE mode. Therefore the /IDE_PCE1 signal is linked with A11='0' and the /IDE_PCE2 signal is linked with A11='1'. Both signals are active during 8-bit as well as 16-bit accesses. As an option the IDE interface can also run in DMA mode. The DMA mode is activated by setting DMAENA. The free DMA channel can be selected in register DMA0/1. The DACK signal is generated if A21=1 and A13=0.

REG	ADDR	D7	D3	D2	D1	D0
IDE 1	0x2001002	Res	DMA0/1	DMAEN	RES	IDE/MEM
RW		R/W=0	R/W	R/W	R/W=0	R=1/W=1

Table 20: IDE Control Register 1

IDE/MEM Setting this bit to "1" selects the TrueIDE mode. In this mode address line A11 is used to switch the PCE1 and PCE2 memory areas. It is not possible to use the memory mode.

DMAEN This bit enables the optional DMA mode.

DMA0/1 This bit configures the available DMA channel.

IDE control register 2 includes the control signals for Reset and Ready. The hard drive reset can be controlled via software. Bit 1 of the IDE control register 2 will generate a reset if set to "0" while setting this bit to "1" will end the reset cycle. Reading bit 3 returns the status of the hard drive RDY signal.

REG	ADDR	D7	D3	D2	D1	D0
IDE 2	0x2001004	Res	RDY	Res	/IDE_RES	Res
RW			R		RW	

Table 21: IDE Register 2

/IDE_RES Low active reset signal for the hard drive.

/RDY Shows current state of the hard drive Ready signal.

The IDE interface is separated from the data, address and control bus by line driver circuits. The drivers for the data bus can be activated with the signal IDEOE. IDEON activates the drivers for the address and control signal outputs and IDEIN activates the drivers for the input signals such as IRQ.

REG	ADDR	D7	D3	D2	D1	D0
IDE 3	0x2001006	Res	Res	IDEIN	IDEON	IDEOE
RW		R/W=0	R/W=0	R/W	R/W	R/W

Table 22: IDE Control Register 3

IDEOE Setting this bit turns on the data bus line drivers.

IDEON Setting this bit turns on the control and address lines.

IDEIN Setting this bit turns on the input signals.

The IDE control register 4 is responsible for the supply voltage to the IDE hard drive. The register bit 5 V/3 V is always set to 1 because the hard drive runs with 5 V. If IDEPWR is set then the 5 V is connected to the hard drive. The IDE5V bit is set in response.

REG	ADDR	D7	D3	D2	D1	D0
IDE 4	0x2001008	Res	IDE5V	RES	5V/3V	IDEPWR
RW		R/W=0	R	R/W=0	R=1/W=1	R/W

Table 23: IDE Control Register 4

IDEPWR Setting this bit turns on the 5 V supply voltage for the IDE drive.

3V/5V This bit will always retunr a "1" because only a 5 V supply voltage is permissible.

IDE5V Indicates that the 5 V supply voltage has been turned on.

The PXA255 PCMCIA interface does not support TrueIDE mode. When operating in TrueIDE mode signals /IDE_PCE1 and /IDE_PCE2 don't control the LowByte and HighByte but two different memory areas. LowByte or HighByte are selected via address line A0 in TrueIDE mode. PLD U7 allows access to the two separate memory areas (Controlregister 1 Bit 0 = 1) by using address line A11 in order to decide which of the two Chip Select signals is active.

A11	**/IDE_PCE1 and /IDE_PCE2 Level**
0	/IDE_PCE1 = active, /IDE_PCE2 = not active
1	/IDE_PCE2 = active, /IDE_PCE1 = not active

Table 24: TrueIDE Memory Area Assignment

Based on the above assignment scheme the following memory areas are used in conjunction with the physical address range of the PXA255 controller. It should be noted that operating systemns such as Linux and WinCE use virtual addresses. This means that physical addresses can also be mapped to other memory areas.

Active Address Range	**Corresponding Chip Select Signal**
0x2000 0000	/IDE_PCE1
0x2000 0800	/IDE_PCE2

Table 25: Physical Address Range of the IDE Interface

For more information consult your IDE data sheet.

5.3.2 Compact Flash Interface

The PXA255 controller supports two PCMCIA interfaces. The second interface is used on the Development Board as a CompactFlash socket. PLD U7 provides all the control logic to operate the CompactFlash interface. The connector is located on the corresponding Expansion Board.

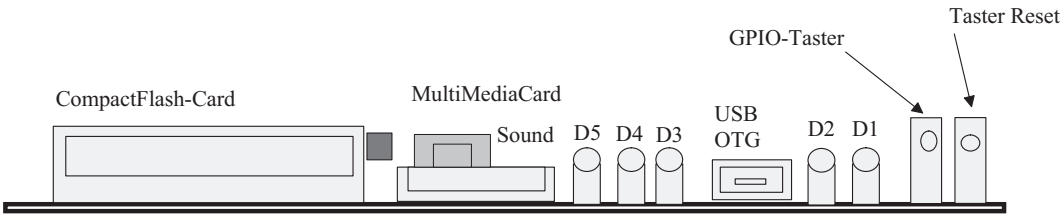


Figure 16: Compact Flash Interface on the Expansion Board

The CompactFlash card is operated in TrueIDE mode. The interface is decoupled from the buffered data and address bus on the Development Board with 74LVC245 line driver ICs.

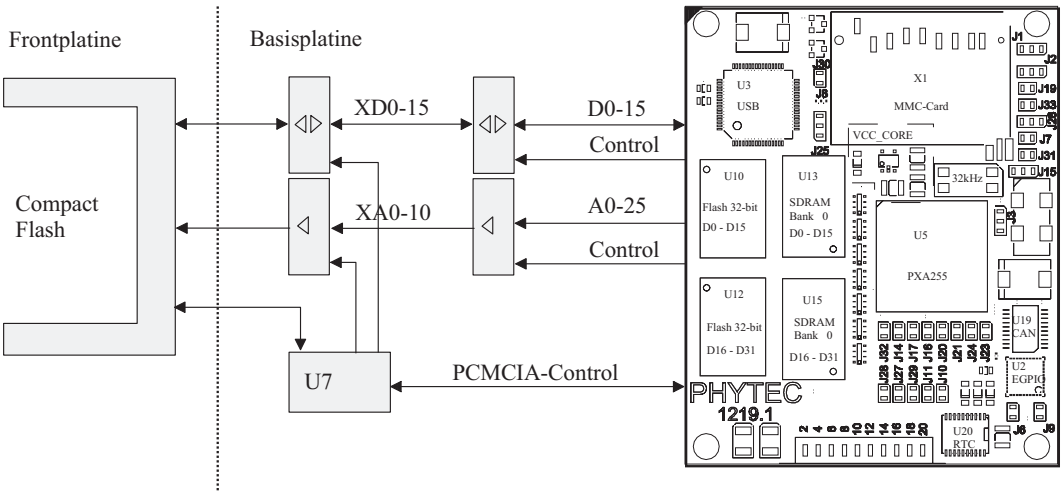


Figure 17: Compact Flash Circuitry

Caution!
The CompactFlash connector can only be operated at 3.3 V when using the Development Board with PCB revision 1220.1.

The settings for the PCMCIA interface are made in the PXA255 controller. The CF card registers of the PLD U7 along with their reset values are given in the following table.

REG	ADDR	D7	D3	D2	D1	D0
CF0	0x3001000	Res	Res	PM_5V	Res	LED
Reset				X		0
CF1	0x3001002	Res	Res	Res	Res	IDE/MEM
Reset						0
CF2	0x3001004	Res	RDY	RDYEN	RESET	RESEN
Reset			0	0	0	0
CF3	0x3001006	Res	CFCD	IDEIN	IDEON	IDEOE
Reset			0	0	0	0
CF4	0x3001008	Res	CF5V	CF3V	5V/3V	CFPWR
Reset			0	0	0	0
CF5	0x300100A	Res	/VS2	/VS1	/BVD2	/BVD1
Reset			X	X	X	X
CF6	0x300100C	Res	WP	Res	/CD2	/CD1
Reset			X		X	X

Table 26: CF Card Control Register with Reset Values

The operating states of the 5 V supply voltages can be read in the CF control register 0. If the Development Board's input voltage drops below 8 V, the 5 V supply voltage will be shut off. The CF LED is located at register bit 0. The LED is switched on by setting the bit and can be used as an access display for the CF card socket.

REG	ADDR	D7	D3	D2	D1	D0
CF0	0x3001000	Res	Res	PM_5V	Res	LED
RW				R		RW

Table 27: CF Card Control Register 0

LED Controls the CF card access LED.

PM_5V This bit indicates that the 5 V supply voltage is active.

CF control register 1 is used to set the memory interface. The CF card interface can operate in TruIDE mode if the register bit is set to 0. The PXA255 controller's PCMCIA interface does not support TruIDE mode. Therefore the /CF_PCE1 signal is linked with A11='0' and the /CF_PCE2 signal is linked with A11='1'. Both signals are active during 8-bit as well as 16-bit accesses. If register bit 0 is set to '0' then the memory mode of the CF card is configured. This memory interface is supported directly by the PXA255.

REG	ADDR	D7	D3	D2	D1	D0
CF1	0x3001002	Res	Res	Res	Res	IDE/MEM
RW		R/W=0	R/W=0	R/W=0	R/W=0	R=1/W=1

Table 28: CF Card Control Register 1

IDE/MEM Setting this bit to "1" turns on the TrueIDE mode, writing a "0" selects the memory mode.

The CF card settings for Reset and RDY are made in CF control register 2. With RES_POL the polarity of the reset signal can be set and with RESENA the Reset can be activated. RDYENA connects the RDY signal of the CF card to the controller signal PWAIT. The RDY signal can be read on the RDY bit.

REG	ADDR	D7	D3	D2	D1	D0
CF2	0x3001004	Res	RDY	RDYENA	RES_POL	RESENA
RW		R/W=0	R/W	R/W	R/W	R=1/W=1

Table 29: CF Card Control Register 2

RESENA Activates the CF card reset.
RESPOL Indicates the polarity for the CF card reset.
RDYEN Connects the RDY input with PWAIT.
RDY Returns the state of the RDY signal.

The CF interface is separated from the data, address and control bus by line driver circuits. The drivers for the data bus can be activated with the signal CFOE. CFON activates the drivers for the address and control signal outputs and CFIN activates the drivers for the input signals such as IRQ.

REG	ADDR	D7	D3	D2	D1	D0
CF3	0x3001006	Res	CFCD	CFIN	CFON	CFOE
RW		R/W=0	R/W	R/W	R/W	R/W

Table 30: CF Card Control Register 3

CFOE Turns on the data bus line driver.
CFON Turns on the address bus and contol line driver.
CFIN Turns on the line driver for input signals.
CFCD Turns on the line driver with the CF card control output signals such as CD1/2 etc.

CF control register 4 configures the supply voltage for the CF card interface. The register bit 5 V/3 V is used to configure the CF card voltage. If the bit is set to '1' the CF card is supplied with 5 V, if the bit is set to '0' then the CF card is supplied with 3.3 V. If CFPWR is set then the configured voltage (5 V or 3.3 V) is connected to the CF card. In response the CF5V bit will be set for a 5 V supply voltage or CF3V if a 3.3 V supply is used.

REG	ADDR	D7	D3	D2	D1	D0
CF4	0x3001008	Res	CF5V	CF3V	5V/3V	CFPWR
RW		R/W=0	R	R	R/W	R/W

Table 31: CF Card Control Register 4

CFPWR Turns on the selected CF card voltage.
5V/3V Selects the CF card voltage; 1 = 5 V, 0 = 3.3 V
CF3V Indicates 3.3 V supply active.
CF5V Indicates 5 V supply active.

Control register 5 displays the CF card signals /VS1, /VS2, /BVD1 and /BVD2. /VS1 and /VS2 should be read in order to set the correct CF card supply voltage in CF card control register 4.

REG	ADDR	D7	D3	D2	D1	D0
CF5	0x3000100A	Res	/VS2	/VS1	/BVD2	/BVD1
RW		R/W=0	R	R	R	R

Table 32: CF Card Control Register 5

/BVD1 Returns the CF card /BVD1 signal.
/BVD2 Returns the CF card /BVD2 signal.
/VS1 Returns the CF card /VS1 signal.
/VS2 Returns the CF card /VS2 signal.

The CF card CD signals can be read via control register 6. If a CR card is inserted correctly in the socket both signals should read back the value '0'.

REG	ADDR	D7	D3	D2	D1	D0
CF6	0x3000100C	Res	WP	Res	/CD2	/CD1
RW		R/W=0	R/W=0	R/W=0	R	R

Table 33: CF Card Control Register 6

/CD1 Returns the Card Detect1 signal, active low.
/CD2 Returns the Card Detect2 signal, active low.

6 Ethernet Interface

The Ethernet interface of the phyCORE-PXA255 is supplemented on the Development Board by the Ethernet transformer and the RJ45 connector.

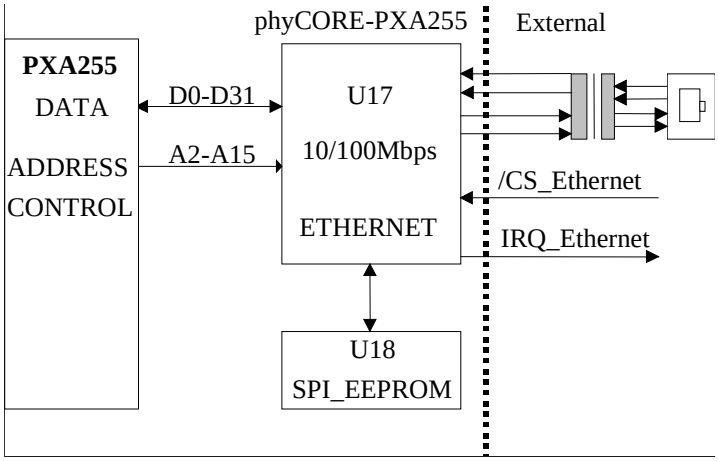


Figure 18: Ethernet Circuitry

The Ethernet interface is accessible on the RJ45 socket at X23. The yellow LED extends to the /LAN_LED_A signal and the green LED extends to /LAN_LED_B. The organization of the LED functions is freely programmable in the LAN91C111 Ethernet chip and is therefore operating system dependent.

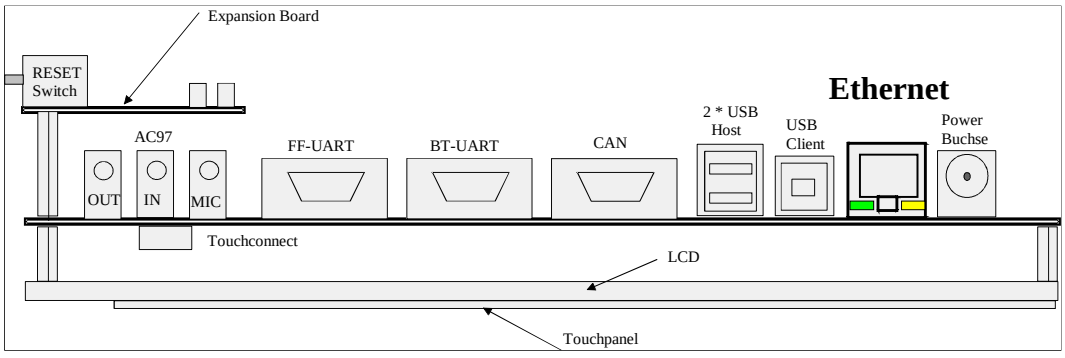


Figure 19: Location of the Ethernet Socket

The Ethernet chip's physical memory area is given in the following table. The address decoder generates the Ethernet /CS at address 0x14000000. In addition an offset of 0x00000300 has to be added.

Ethernet	**Start Address**
/CS_ETH + OFFSET	0x 1400 0000 + 0x 0000 0300 = 0x 1400 0300

Table 34: Address Space for Ethernet Controller

7 USB Host

The PXA255 controller lacks support of controlling input devices such as a keyboard or a mouse. Therefore the Philips ISP1362 USB host OTG (on the go) controller has been integrated on the phyCORE-PXA255. This controller supports two USB host interfaces, whereby one can function as an OTG interface. On the Development Board the USB host interfaces are connected to a double USB host socket. The first USB host interface can also operate in OTG mode and is also connected to an OTG socket on the Expansion Board. The first USB host interface can only be used either on the Development Board in OTG mode or on the Expansion Board.

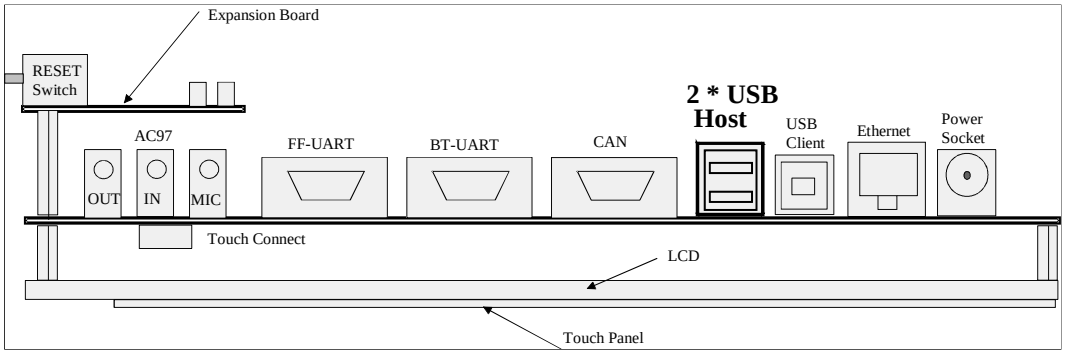


Figure 20: USB Host Connector

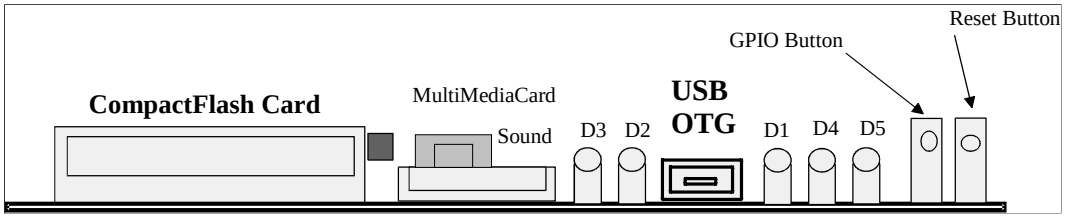


Figure 21: Location of the USB OTG Socket

The following table gives an overview of jumpers relevant for configuring the USB interface:

Jumper	Default	Comment
JP3		This jumper configures the USB controller OTG ID input. *Refer to ISP1362 USB-OTG controller data sheet and user's manual for details.*
1 + 2	-	OTG ID = 10 kOhm pull-up,for external OTG ID signal
2 + 3	X	OTG ID tied to Ground.
JP5		This jumper configures the USB controller VDD_5V input. *Refer to ISP1362 USB-OTG controller data sheet and user's manual for details.*
1 + 2	-	OTG_5V connected to 3.3V (VDD_5V pin on ISP1362)
2 + 3	X	OTG_5V connected to 5V (VDD_5V pin on ISP1362)
JP6		This jumper configures the routing of the first USB channel supply voltage. *Refer to ISP1362 USB-OTG controller data sheet and user's manual for details.*
1 + 2	-	USB 5V routed to OTG interface on expansion board.
2 + 3	X	USB 5V routed to USB host interface on development board.
JP9		This jumper configures reference voltage for the OTG interface. *Refer to ISP1362 USB-OTG controller data sheet and user's manual for details.*
1 + 2	-	OTG_VBUS connected to USB 5V from interface #1
2 + 3	X	OTG_VBUS open

Table 35: USB Host Jumpers

8 USB Client

The PXA255 controller is equipped with a USB client interface for communication with a PC. The interface extends to a USB client socket X22 on the Development Board.

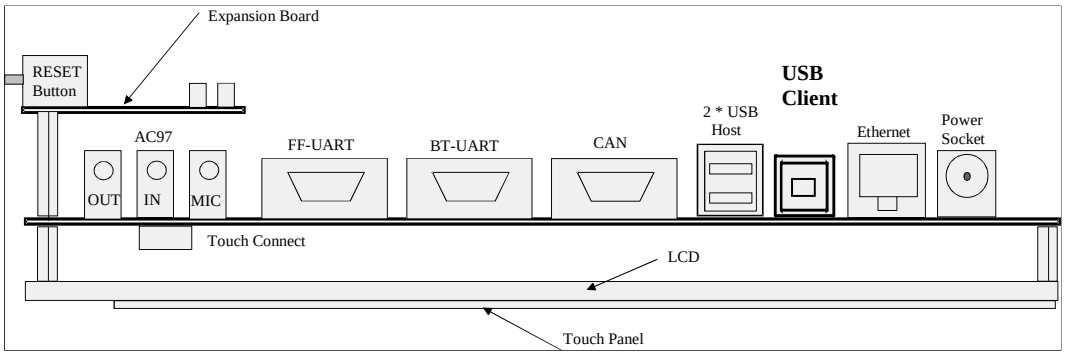


Figure 22: USB Client Connector

9 LCD Interface

There is an active TFT-LCD interface on the Development Board for controlling displays with 18-bit color depth (6 each for red, green and blue). The LCD signals are decoupled from the PXA255 controller with 74LVC254 line driver circuits. Since the controller only supports 16-bit color information, the least significant bits decoding blue and red are connected to GND.

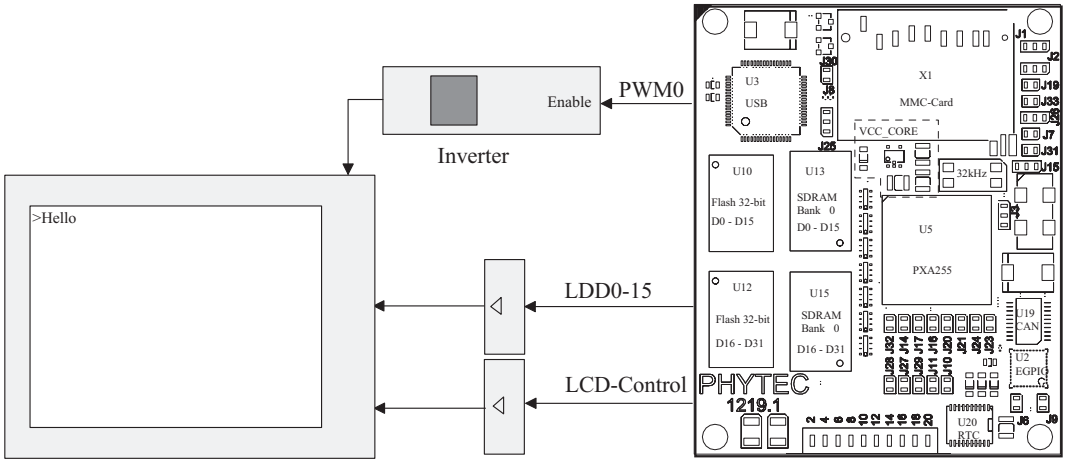


Figure 23: Active TFT LCD Connection

The Sharp display used on the Development Board offers the possibility of adjusting the display size and position via two inputs. The control PLD U6 enables configuration of these inputs over internal registers.

The Development Board can be connected to the TFT display with the help of a 33-pin ribbon cable on the connector plug X35. An LCD-001 adapter board is necessary when using the Sharp TFT display in order to convert the Hirose connector plug to a ribbon cable connector plug. Furthermore, there is a 2.0 mm universal connector plug on the board at X33, where other display types can be adapted to the PXA255's LCD port.

Signal		A	B		Signal
GND		**1**	**1**		PCLK
GND		**2**	**2**		LCLK
GND		**3**	**3**		FCLK
GND		**4**	**4**		R0
R1		**5**	**5**		R2
R3		**6**	**6**		R4
R5		**7**	**7**		GND
G0		**8**	**8**		G1
G2		**9**	**9**		G3
G4		**10**	**10**		G5
GND		**11**	**11**		B0
B1		**12**	**12**		B2
B3		**13**	**13**		B4
B5		**14**	**14**		GND
LCD_ENAB		**15**	**15**		3.3V VCC
3.3V VCC		**16**	**16**		LCD_POS1
LCD_POS2		**17**	**17**		LCD_POS3

Table 36: LCD Connector at X33

The supply voltage for the TFT display and the inverter can be turned on with the help of a register in control PLD U6. The brightness of the background illumination can be set using the controller's PWM0 signal. The inverter is located on the Development Board near the LCD inverter cable.

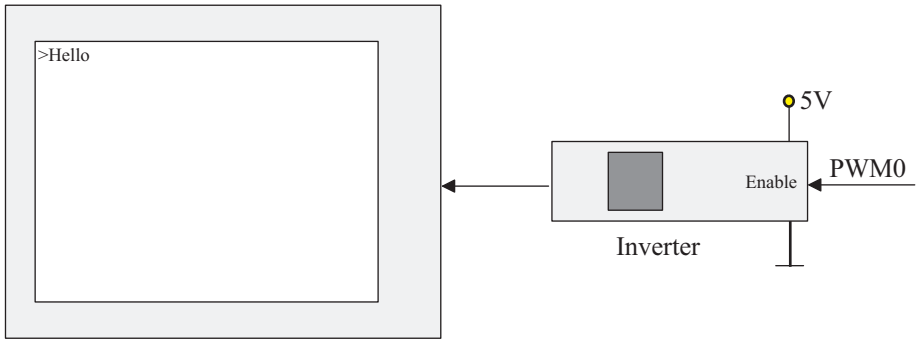


Figure 24: LCD Inverter Circuitry

10 RS-232 Interface

The PXA255 controller has four internal UARTS. Three of these are supported in the current version of the phyCORE-PXA255. Two of the interfaces are accessible in the standard RS-232 level over DB-9 sockets at P1 (FF-UART) and P2 (BT-UART).

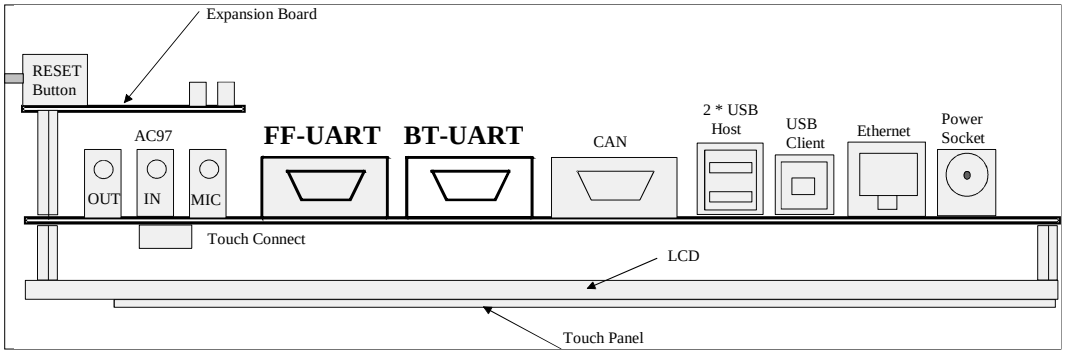


Figure 25: RS-232 Connectors (FF-UART, BT-UART)

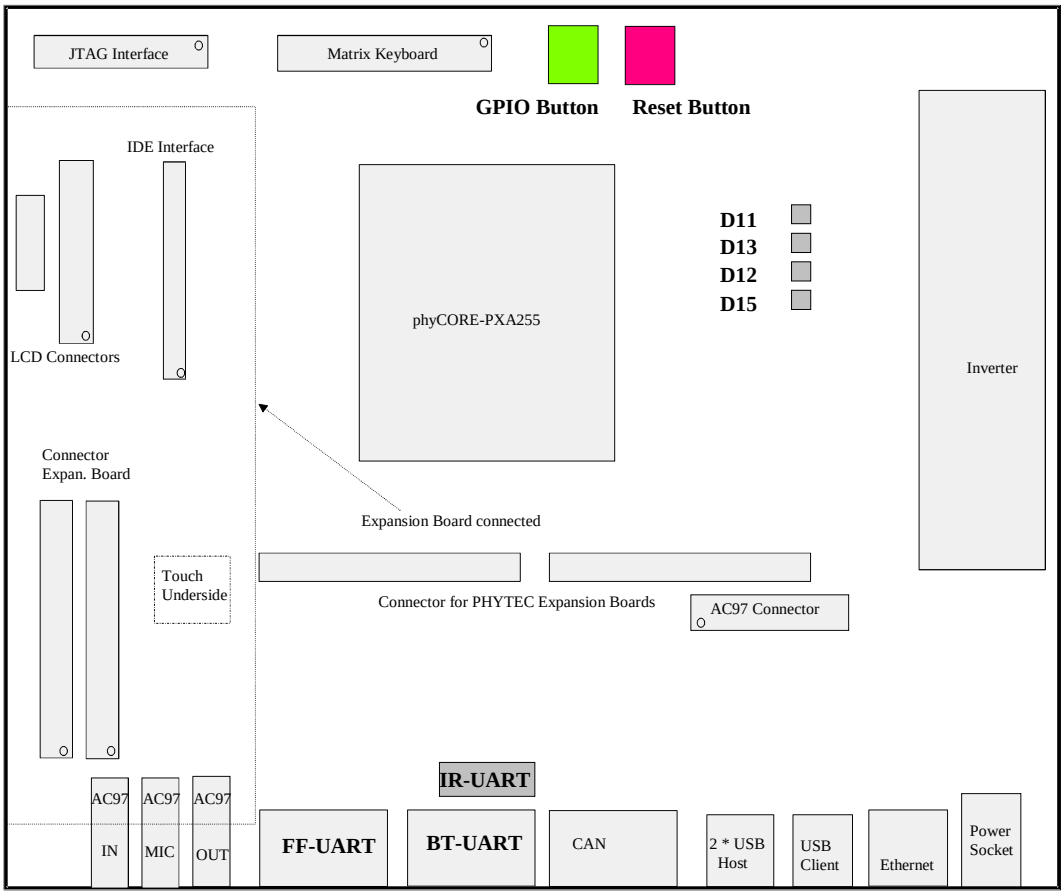
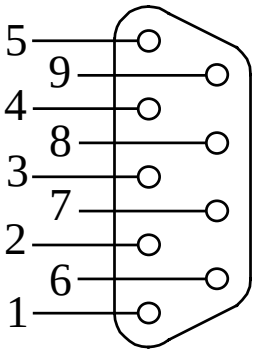


Figure 26: IR-UART Connector

10.1 FF-UART

The FF-UART (Full Feature UART) is a UART with all modem and control signals and a maximum transfer rate of 921.5 kBaud. This interface is used on the phyCORE-PXA255 for communication with the PC. The RS-232 transceiver device is located on the phyCORE module at U1. The RS-232 transceiver is configured for auto shutdown, which means that the driver shuts off automatically after a few seconds in order to conserve power. The RS-232 transceiver can be made inactive over the PowerLatch (data bit D1). On the Development Board, the interface always extends to socket P1.

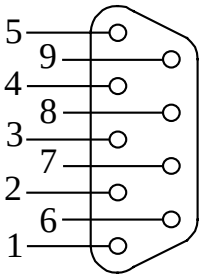


Pin 5:	GND
Pin 9:	FF_RI
Pin 4:	FF_DTR
Pin 8:	FF_CTS
Pin 3:	FF_TxD
Pin 7:	FF_RTS
Pin 2:	FF_RxD
Pin 6:	FF_DSR
Pin 1:	FF_DCD

Figure 27: P1 Pin Assignment, FF-UART

10.2 BT-UART

The BT-UART has the same properties as the FF-UART, however only the signals BT_RxD, BT_CTC and BT_RTS are supported. The TTL signals RXD and CTS can be separated from the RS-232 transceiver at U42 with Jumper JP2 set to 3+4 and 5+6. The RS-232 transceiver is located on the Development Board.



Pin 5: GND
Pin 9: nc
Pin 4: nc
Pin 8: BT_CTS
Pin 3: BT_TxD
Pin 7: BT_RTS
Pin 2: BT_RxD
Pin 6: nc
Pin 1: nc

Figure 28: P2 Pin Assignment, BT-UART

Jumper	Default	Comment
JP2		This jumper connects the BT-UART to the RS-232 transceiver.
1 + 2	-	IR_RXD connected to RS-232 transceiver.
3 + 4	closed	BT_RXD connected to RS-232 transceiver.
5 + 6	closed	BT_CTS connected to RS-232 transceiver.

Table 37: BT-UART Jumper Configuration

10.3 IR-UART

The IR-UART has the same properties as the FF-UART, however only the signals IR_RxD and IR_TxD are supported. The TTL level signals RXD and CTS can be separated from the RS-232 transceiver U42 with Jumper JP2 set to 1+2. The RS-232 transceiver is located on the Development Board. The IR-UART extends to a 10-pin header connector at X19, to which an optional flat band cable with a DB 9 socket can be connected.

Signal		A	B		Signal
n.c.		**1**	**1**		n.c.
STD_RxD		**2**	**2**		n.c.
STD_TxD		**3**	**3**		n.c.
n.c.		**4**	**4**		n.c.
GND		**5**	**5**		VCC via J20

Table 38: IR-UART Connector at X19

Jumper	Default	Comment
JP2		This jumper connects the IR-UART to the RS-232 transceiver.
1 + 2	closed	IR_RXD connected to RS-232 transceiver.
3 + 4	-	BT_RXD connected to RS-232 transceiver.
5 + 6	-	BT_CTS connected to RS-232 transceiver.

Table 39: IR-UART Jumper Configuration

11 CAN Interface

An industry-standard CAN interface is populated on the PXA255 Development Board for integration into networked machines and systems. The CAN controller is located on the phyCORE module.

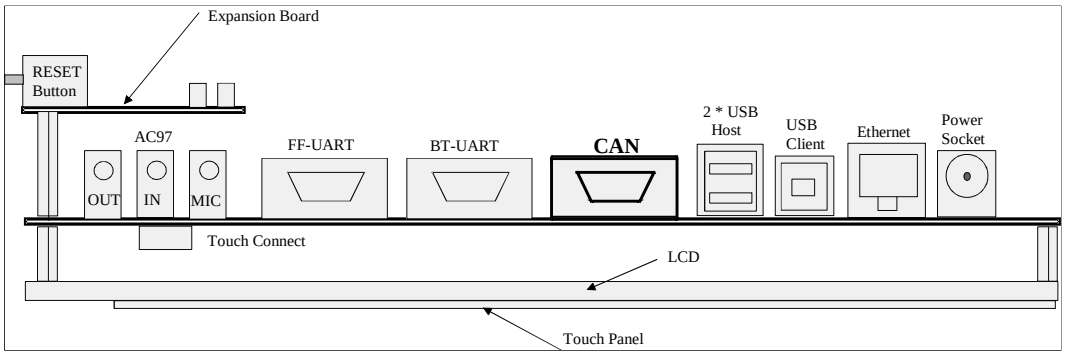


Figure 29: CAN Connector

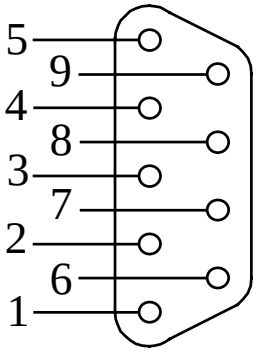
The signals CAN-RxD and CAN-TxD are optically isolated from the phyCORE module over an ADU1402 opto-coupler (U45) and are converted over an 82C251 CAN transceiver (U46) to CANH and CANL. A switching voltage regulator converts the exernal CAN supply voltage in a range from 8-24V to a 5V/0.5A CANVCC. This enables galvanic separation of the CAN circuitry from the potential of the Development Board. Jumpers JP7 and JP10 must be closed at position 2+3 in order to support galvanic separation, when closed at position 1+2 the CAN interface is powered by the internal 5 V supply from the Development Board.

Jumper	Default	Comment
JP7		This jumper configures the CAN circuitry supply voltage.
1 + 2	-	CAN supply voltage derived from on-board supply voltage
2 + 3	X	CAN supply voltage from external source for optical isolation
JP10		This jumper configures the CAN circuitry supply voltage.
open	X	CAN Ground from external source for optical isolation.
closed	-	CAN Ground connected to on-board Ground potential.

Table 40: CAN Interface Jumper Configuration

Note:
Support of the external CAN supply voltage is only available with PCB revision 1220.2 or higher.

The following figure depicts the CAN connector pin assignment:



Pin 9: CANV+

Pin 3: CANV-
Pin 7: CAN-H (optically isolated)
Pin 2: CAN-L (optically isolated)
Pin 6: CANV-

Figure 30: CAN Connector P3 Pinout

12 AC97 Interface and Touch Controller

The PXA255 controller feataures an AC97 interface for controlling sound decoders such as the WM9712L from Wolfson. The WM9712L also has an integrated touch controller.

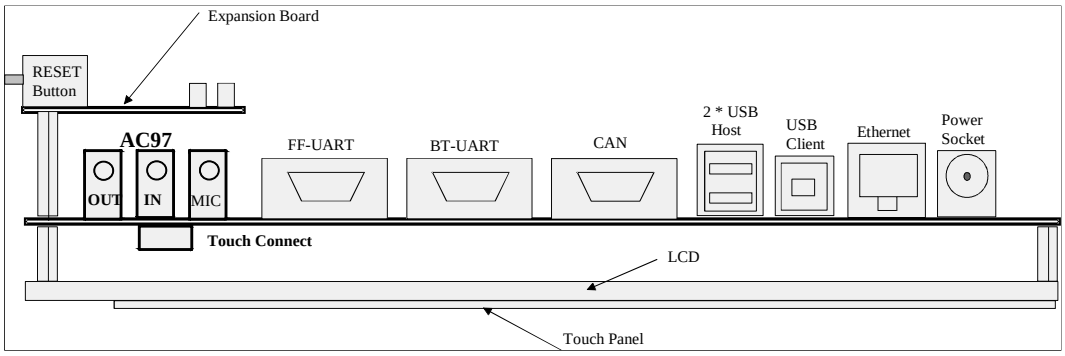


Figure 31: Sound and Touch Controller Interfaces

The sound decoder WM9712L is controlled via the controller's AC97 interface. The SDATA_IN0 is used as the input channel. The second channel is available on the AC97 expansion socket at X24. Connection to other AC97 devices such as modems is possible via this socket.

Signal		A	B		Signal
VCC (3,3V)		**1**	**2**		VCC (3,3V)
/ENA_AC97		**3**	**4**		/ACRESET
SYNC		**5**	**6**		GND
BITCLK		**7**	**8**		GND
SDATA_OUT		**9**	**10**		GND
SDATA_IN0		**11**	**12**		GND
SDATA_IN1		**13**	**14**		GND
AC_INT		**15**	**16**		GND

Table 41: AC97 Expansion Socket at X24

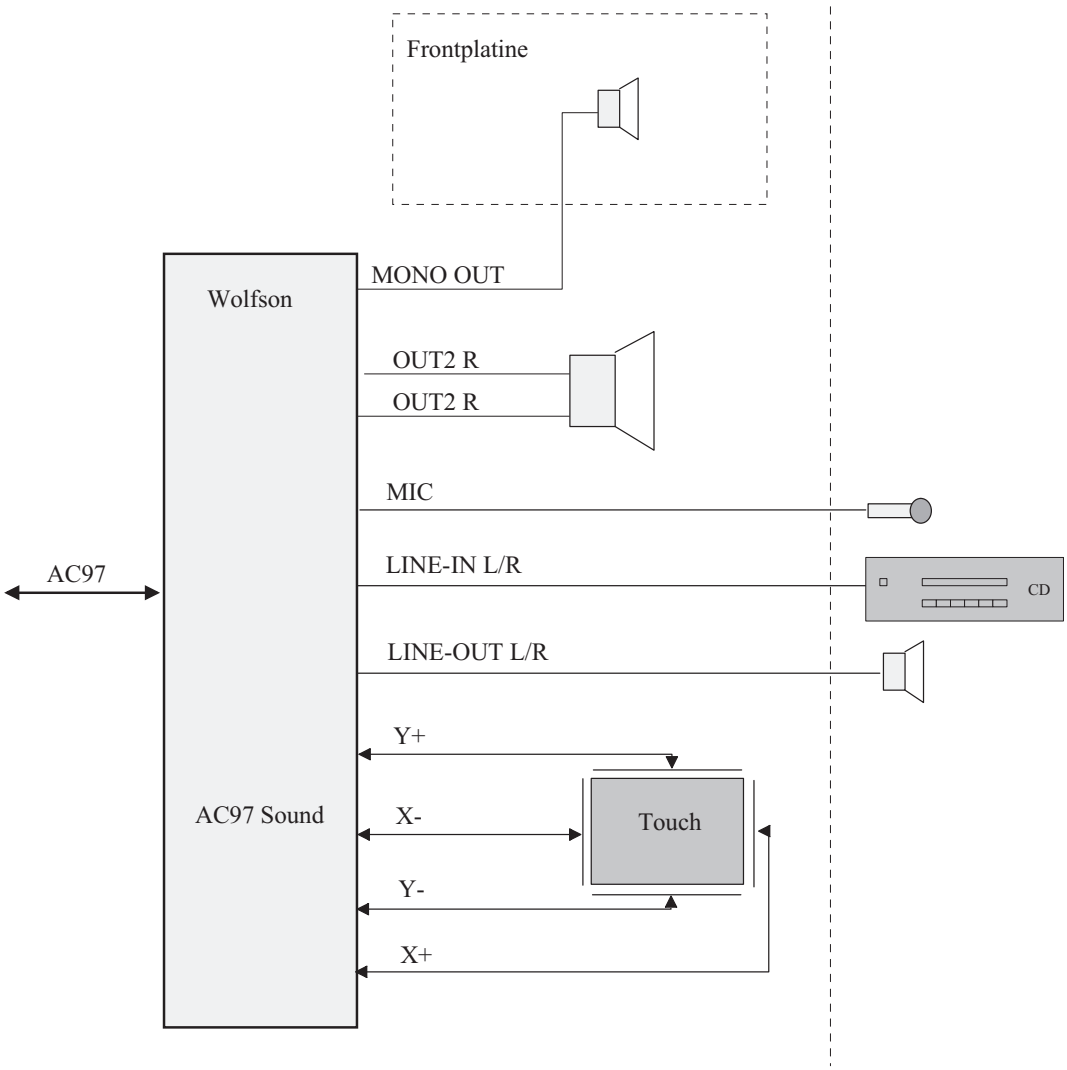


Figure 32: AC97 with WM9712L

The signals from the integrated touch controller are routed to connector X25 on the Development Board.

The WM9712L IC also provides four analog inputs that can be used for voltage monitoring purposes.

ADC	**Function**
AUX0	AKKU_COMP, battery voltage
AUX 1	AKKU_IBAT, battery current draw
AUX 2	AKKU_TEMP, battery temperature
AUX 3	Light sensor

Table 42: Voltage Supervision with WM9712L

The sound portion of the WM9712L supports microphone (mono), stereo input und stereo output.

Sound Jack	**Functions**
X28	Mikrophone input (mono)
X27	Stereo input
X26	Stereo output

Table 43: Sound Jacks

Another functional block of the WM9712L allows for controlling of loudspeakers. A miniature loudspeaker connected to MonoOut is implemented on the Expansion Board. A larger 0.4W loudspeaker is located on the Development Board at X36 and is connected to signals LOUT2 and ROUT2.

13 MultiMedia Card

The second PCMCIA interface of the PXA255 controller is available on the Expansion Board and supports MultiMedia cards. MultiMedia cards are available as memory devices with capacities of 8 to 256 MByte that can be easily removed by the user. Access to the MMC connector is controlled via MMC-CS1.

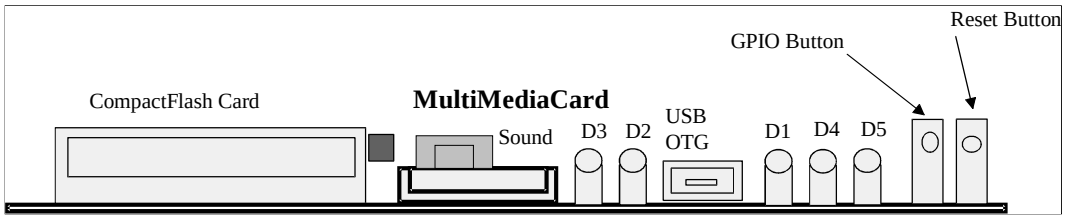


Figure 33: MultiMedia Card

14 Expansion Board

The LCD is mounted on the backside of the Development Board to enable easy installation of the Development Board inside an enclosure. All important interfaces and sockets that need to be accessed by the user are populated on an Expansion Board. These can be mounted in the housing at a 90° angle to the display, whereby access to a MultiMediaCard, CompactFlash, USB and push buttons is possible.

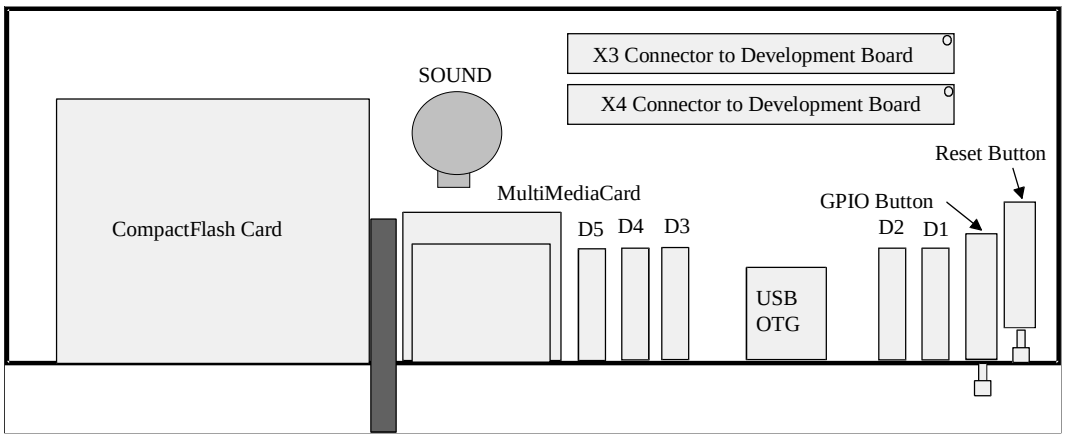


Figure 34: Expansion Board, Top View

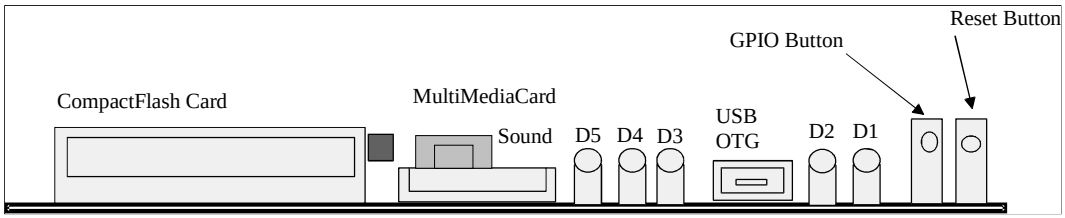


Figure 35: Expansion Board, Side View

The Expansion Board is connected over two, 2.0 mm, 44-pin flat band cables. The pinout of the Development Board plugs X30 and X31 is given in the following table. Using a customer-specific Expansion Board instead of the standard Expansion Board is also possible given the removable connection via flat band cables. The connector X10 contains the signals for the CompactFlash card. The voltage pin CF_VCC can only be used for the CF card, because it is switched on or off depending on the operating status of the socket.

Signal	X30		Signal
CF_VCC	**1**	**2**	CF_VCC
GND	**3**	**4**	GND
CF_D0	**5**	**6**	CF_D1
CF_D2	**7**	**8**	CF_D3
CF_D4	**9**	**10**	CF_D5
CF_D6	**11**	**12**	CF_D7
GND	**13**	**14**	GND
CF_D8	**15**	**16**	CF_D9
CF_D10	**17**	**18**	CF_D11
CF_D12	**19**	**20**	CF_D13
CF_D14	**21**	**22**	CF_D15
GND	**23**	**24**	GND
CF_A0	**25**	**26**	CF_A4
CF_A1	**27**	**28**	CF_A5
CF_A2	**29**	**30**	CF_A6
CF_A3	**31**	**32**	CF_A7
GND	**33**	**34**	GND
CF_A8	**35**	**36**	/CF_CS1
CF_A9	**37**	**38**	/CF_CS2
CF_A10	**39**	**40**	/CF_WE
/CF_PREG	**41**	**42**	/CF_OE
GND	**43**	**44**	GND

Table 44: Expansion Board Connector X30 Pinout

Connector X31 contains the signals for controlling the CF card, the LEDs, push buttons, USB client and MMC. The 3.3 V supply voltage is fed to the Expansion Board over pins 1 and 2.

Signal	X31		Signal
VCC	**1**	**2**	VCC
GND	**3**	**4**	GND
/CF_IORD	**5**	**6**	/CF_CD1
/CF_IOWR	**7**	**8**	/CF_CD2
CF_IRQ	**9**	**10**	/CF_RDY
/CF_RESET	**11**	**12**	/CF_IOIS16
GND	**13**	**14**	GND
OTG_ID	**15**	**16**	/CF_BVD1
OTG_DP1	**17**	**18**	/CF_BVD2
OTG_DM1	**19**	**20**	/CF_LED
OTG_VCC	**21**	**22**	/CF_VS1
GND	**23**	**24**	GND
/CF_VS2	**25**	**26**	/CF_INPACK
/RESIN	**27**	**28**	/OTG_LED
/SW_ON	**29**	**30**	AUDIO_P
/LED_USR	**31**	**32**	AUDIO_N
GND	**33**	**34**	GND
/LED_PWR	**35**	**36**	MMC_WP2
/MMC_LED	**37**	**38**	MMC_CS1
MMCDET2	**39**	**40**	MMC_CLK
MMCDAT	**41**	**42**	MMC_CMD
GND	**43**	**44**	GND

Table 45: Expansion Board Connector X31 Pinout

15 Push Buttons and LEDs

Four push buttons and 3 LEDs are integrated on the Development Board and corresponding Expansion Board serving as user input and display elements. Push Button S2 on both the Expansion Board and the Development Board serves as a reset button, push button S1 is connected with the GPIO0 signal for both boards and can be used freely. The 4 LEDs are controlled with a low level over the PowerLatch. It is important that the other PowerLatch settings are not changed during a write to these LEDs.

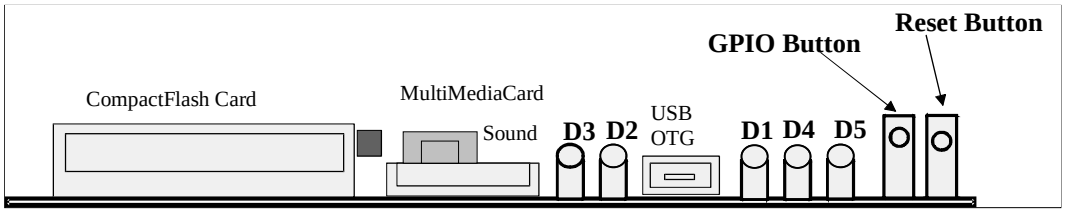


Figure 36: Location of Push Buttons and LEDs (Side View)

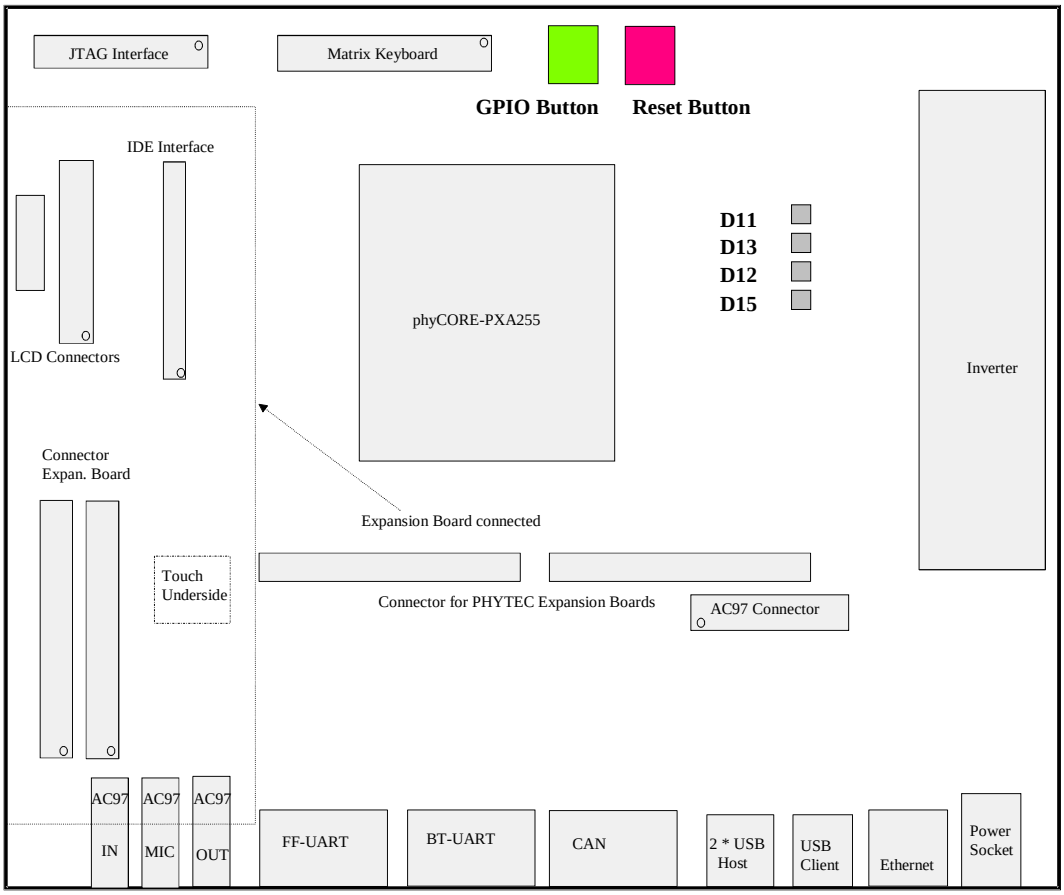


Figure 37: Location of Push Buttons and LEDs (Top View)

16 Matrix Keyboard

The phyCORE-PXA255 is populated with a GPIO expander, which can be used for the connection of a matrix keyboard. The signal lines extend to connector X4 and are arranged in columns and rows. The column outputs have an in-line resistance of 33R and the row inputs have an RC combination with R=1 kOhm against VCC and C = 100 nF against GND to prevent a possible signal bounce.

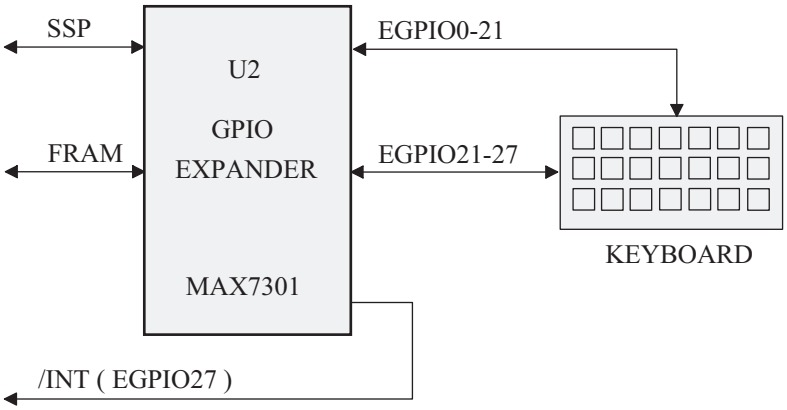


Figure 38: Matric Keyboard Connection

17 GPIO Expansion Board Interface

The Development Board also provides a socket for standardized PHYTEC Expansion Boards. All signals except the data, address and control bus of the phyCORE-PXA255 extend from phyCORE connector X18 to the expansion connector X17 in a strict 1:1 arrangement. The data, address and control bus is buffered on the Development Board over line driver circuits before being connected to X17. The Ethernet signals do not extend to the expansion socket.

Similar to the numbering scheme of the phyCORE connector, the expansion connector also uses a two-dimensional number matrix. Because of its different layout, however, the arrangement of the expansion connector's number matrix differs from that of the phyCORE connector.

Please refer to the following figure for the arrangement of the number matrix for the expansion connector:

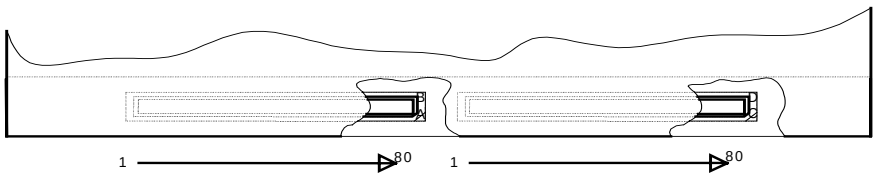


Figure 39: GPIO Expansion Bus Numbering Scheme

In the current version of the address decoder there is no memory area provided for the expansion card receptacle, because all /CS signals of the PSA255 are occupied. The following tables give the signal assignments for the signals of the phyCORE connector X18 to the expansion bus connector. Signals that are in bold are buffered on the Development Board.

Pin Number	Signal	I/O	Comments
Pin Row X17A			
1A	CLKIN	I	Optional external clock input of the processor
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	GPIO2	I/O	Processor I/O port, *alternative: interrupt*
4A	GPIO0	I/O	Processor I/O port, *alternative: interrupt*
5A	**/CS_2**	I/O	Freely available /CS signal of the processor, *alternative: GPIO78*
6A	**/CS_4**	I/O	Chip Select signal of the processor, can be used to access the USB controller, *alternative: GPIO80*
8A	**/WE**	O	Write-enable signal for SDRAM, SRAM and Flash devices. Please note that the /PWE signal must be used for I/O components.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A, 36A	**A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23, A24**	I/O	Address lines
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	**D1, D2, D4, D7, D9, D10, D12, D15, D18, D19, D20, D22, D25, D27, D28, D30**	I/O	Data lines
34A, 35A	**DQM_1, DQM_2**	O	Byte enable signals
48A	**RDY**	I/O	Ready signal of the processor, *alternative: GPIO 18*
49A	**RDnWR**	O	Bus control signal of the processor

Pin Number	Signal	I/O	Comments
Pin row X17A			
50A, 51A	**DREQ_0** **DREQ_1**	O	DMA request singal DREQ0 *alternative: GPIO 20* DREQ1 *alternative: GPIO 19*
53A, 54A	**/SDCKE_0** **/SDCKE_1**	O	Clock enable for synchronous memory
55A, 56A	**/SDCLK_0** **/SDCLK_1**	O	Clock signal for synchronous memory
58A, 59A	**/PCE_1** **/PCE_2**	I/O	PCMCIA Chip Select resp. byte control signal, *alternative: GPIO52/53*
60A	**/PWAIT**	I/O	PCMCIA wait signal, *alternative: GPIO56*
61A	**/IOIS16**	I/O	PCMCIA 16-bit access *alternative: GPIO57*
63A	**/PREG**	I/O	PCMCIA register control signal *alternative: GPIO55*
64A	/LAN_CS	I	I/O Chip Select for LAN controller
65A	/LAN_DATA	I	DATA Chip Select for LAN controller
66A	LAN_RDY	O	Ready output of LAN controller
68A	**L_PCLK**	I/O	LCD pixel clock *alternative: GPIO76*
69A	**L_LCLK**	I/O	LCD line clock *alternative: GPIO75*
70A	**L_FCLK**	I/O	LCD frame clock *alternative: GPIO74*
71A	**L_BIAS**	I/O	LCD enable *alternative: GPIO77*
73A, 74A, 75A, 76A, 78A, 79A, 80A	**L_DD3, L_DD5** **L_DD6, L_DD8,** **L_DD11,** **L_DD13** **L_DD14**	I/O	LCD data *alternative: GPIO61, GPIO63, GPIO64, GPIO66, GPIO69, GPIO71, GPIO72*

Pin Number	Signal	I/O	Comments
Pin row X17B			
1B	DEV_RES	I	Reset for USB, CAN and Ethernet Device only
2B	GPIO_3	I/O	Processor I/O port, *alternative: interrupt*
3B	GPIO_1	I/O	Processor I/O port, *alternative: interrupt*
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND	-	Ground 0 V
5B	**/CS_3**	I/O	Freely available /CS signal of the processor, *alternative: GPIO79*
6B	**/CS_5**	I/O	Chip Select signal of the processor, can be used to access the LAN controller, *alternative: GPIO33*
7B	**/OE**	O	Output-enable signal of the processor
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B 36B	**A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22, A25**	I/O	Address lines
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	**D0, D3, D5, D6, D8, D11, D13, D14, D16, D17, D21, D23, D24, D26, D29, D31**	I/O	Data lines
33B, 35B	**DQM_0, DQM_3**	o	Byte enable signals
47B	**/CS_0**	O	Chip Select for on-board Flash
48B	**/CS_1**	I/O	/CS-Signal for second on-board 16-bit Flash, *alternative: GPIO15*
50B 51B 52B 53B	**/SDCS_0** **/SDCS_1** **/SDCS_2,** **/SDCS_3**	O	/CS SDRAM bank #0 /CS SDRAM bank #1 /CS SDRAM bank #2 /CS SDRAM bank #3
55B	**/SDCLK_2**	O	Clock signal for synchronous memory
56B	**/SDRAS**	O	/SDRAS control signal for SDRAM
57B	**/SDCAS**	O	/SDCAS control signal for SDRAM

Pin Number	Signal	I/O	Comments
Pin row X17B			
58B	**/PKSEL**	I/O	Card0/1 select *alternative: GPIO 54*
60B	/PWE	I/O	PCMCIA memory write signal and I/O write signal *alternative: GPIO 49*
61B	/POE	I/O	PCMCIA memory read signal *alternative: GPIO 48*
62B	/PIOR	I/O	PCMCIA I/O write signal *alternative: GPIO 50*
63B	/PIOW	I/O	PCMCIA I/O read signal *alternative: GPIO 51*
65B	/LAN_IRQ	I/O	Interrupt LAN controller
66B	/OTG_CS	I	/CS signal for USB controller (PXA /CS_2 or /CS_4)
67B	/OTG_INT1	I	Interrupt /INT1 signal USB controller
68B	/OTG_INT2	I	Interrupt /INT2 signal USB controller
70B, 71B, 72B, 73B, 75B, 76B 77B, 78B 80B	**L_DD0, L_DD1, L_DD2, L_DD4, L_DD7, L_DD9, L_DD10, L_DD12, L_DD15**	I/O	LCD data bus *alternative: GPIO 58, GPIO 59, GPIO 62, GPIO 65, GPIO 67, GPIO 68, GPIO 70, GPIO 73*
Pin row X17C			
1C, 2C	+3V3	P	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C 72C, 77C	GND	P	Ground 0 V
4C	VMMC	P	Optional supply voltage for internal MMC card
5C	VBAT	P	Input for external battery
6C	OTG_5V	I	USB Controller VDD_5V Pin
8C, 9C	/H_OC1, /H_OC2	I	USB Controller Over Current Inputs Cannel 1 /2
10C	/RESIN	I/O	/Reset input for reset controller at U9
11C	/RESET_OUT	I/O	/Reset output of the PXA255 processor
13C	NSSP_FRM	I/O	Network SPI Frame signal, use for CAN Controller *alternative: GPIO 82*

Pin Number	Signal	I/O	Comments
Pin row X17C			
14C	NSSP_CLK	I/O	Network SPI Clock signal, use for CAN Controller *Alternative: GPIO 81*
15C	NSSP_TxD	I/O	Network SPI TxD signal, use for CAN Controller *Alternative: GPIO 83*
16C	NSSP_RxD	I/O	Network SPI RxD signal, use for CAN Controller *Alternative: GPIO 84*
18C	IR_TXD	O	IrDA TxD *Alternative: GPIO 47*
19C	IR_RXD	I	IrDA RxD *Alternative: GPIO 46*
20C	FF_RI_DETECT	O	RI-Detect FF-UART (for interrupt)
21C	FF_/INVALID	O	Invalid level FF_UART
23C	/ACRESET	O	/RESET AC97
24C	SYNC	I/O	SYNC AC97 *Alternative: GPIO 31*
25C	BITCLK	I/O	BITCLK *Alternative: GPIO 28*
26C	SDATA_IN_1	I/O	SDATA_IN 1 AC97 Interface *Alternative: GPIO 32*
28C	SDATA_IN_0	I/O	SDATA_IN0 AC97 Interface *Alternative: GPIO 29*
29C	SDATA_OUT	I/O	SDATAOUT AC97 Interface *Alternative: GPIO 30*
30C	SDA	I/O	I^2C data from processor
31C	SCL	I	I^2C clock from processor
33C	/LAN_LED_A-	O	Not connected
34C	/LAN_LED_B	O	Not connected
35C	LAN_TPI-	O	Not connected
36C	LAN_TPO-	O	Not connected
38C	OTG_ID	I	OTD ID Input USB Controller
39C	PWM0	O	PWM output #0 *Alternative: GPIO 16*
40C	PWM1	O	PWM output #1 *Alternative: GPIO 17*
41C	/TRST	O	JTAG reset
43C	H_DP2	IO	USB H_DP2
44C	H_DM2	IO	USB H_DM2
45C	MMC_CS_1	O	MMC_C1 for external MMC card *Alternative: GPIO 8*

Pin Number	Signal	I/O	Comments
Pin row X17C			
46C	MMC_CS_0	O	MMC_C0 for internal MMC card *Alternative: GPIO 9*
48C, 49C, 50C, 51C, 53C	GPIO4, GPIO7 GPIO10, GPIO12, GPIO21	I/O	GPIOs *Alternative: interrupt signals*
54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C	EGPIO0, EGPIO1, EGPIO3, EGPIO6, EGPIO8, EGPIO9, EGPIO11, EGPIO14, EGPIO16, EGPIO17 EGPIO18, EGPIO22, EGPIO24 EGPIO25, EGPIO27	I/O	Additional GPIOs generated by the MAX7301 IC
73C	SSP_RXD	I	SPI RxD signal
74C	SSP_TXD	O	SPI TxD signal
75C	/CS_EGPIO	I	SSP /CS1 signal for MAX7301 (EGPIO)
76C	/CAN_CS	I	NSSP /CS2 signal for MCP2515 (CAN)
78C	/CAN_INT	O	CAN Interrupt
79C	CANRXD	I/O	CAN RxD signal
80C	CANTXD	I/O	CAN TxD signal
Pin row X17D			
1D, 2D	VCC	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	-	Ground 0 V
4D, 5D	VCC1	I	Optional external supply voltage VCORE for processor, 3-5.0 V
6D	OTG_VBUS	IO	USB Controller VBUS signal
7D	/H_PSW1	O	USB Controller Power Switch 1 signal
8D	/H_PSW2	O	USB Controller Power Switch 1 signal
10D	/RESET	O	Reset output from reset controller
11D	/BATT_FAULT	I	Low battery voltage indication

Pin Number	Signal	I/O	Comments
Pin row X17D			
12D	/VCC_FAULT	I	Low supply voltage indication
13D	PWR_ENAB	O	Power Enable PXA255
15D	BT_CTS	I	CTS Bluetooth UART *Alternative: GPIO 44*
16D	BT_RXD	I	RXD Bluetooth UART *Alternative: GPIO 42*
17D	BT_TXD	O	TXD Bluetooth UART *Alternative: GPIO 43*
18D	BT_RTS	O	RTS Bluetooth UART *Alternative: GPIO 45*
20D	FF_/SHDN	I	FF-UART power up
21D	FL_WP_PEN	I	Flash Write Protect
22D	RS_RXD	I	FF-UART RxD signal (RS-232)
23D	RS_TXD	O	FF-UART TxD signal (RS-232)
25D	RS_RTS	I	FF-UART RTS signal (RS-232)
26D	RS_CTS	I	FF-UART CTS signal (RS-232)
27D	RS_DSR	I	FF-UART DSR signal (RS-232)
28D	RS_DTR	O	FF-UART DTR signal (RS-232)
30D	RS_RI	I	FF-UART RI signal (RS-232)
31D	RS_DCD	I	FF-UART DCD signal (RS-232)
32D	USB_P	I/O	USB Client positive, from processor
33D	USB_N	I/O	USB Client negative, from processor
35D	LAN_TPI+	O	Not connected
36D	LAN_TPO+	O	Not connected
37D	OTG_DP1	I/O	USB Controller OTG_DP1
38D	OTG_DM1	I/O	USB Controller OTG_DM1
40D	TDI	I	JTAG TDI signal
41D	TDO	O	JTAG TDO signal
42D	TMS	I	JTAG TMS signal
43D	TCK	I	JTAG TCK signal
45D	MMC_CLK	I/O	MMC_CLK signal
46D	MMC_DAT	I/O	MMC_DAT signal
47D	MMC_CMD	I/O	MMC_CMD signal
48D, 50D, 51D, 52D, 53D	GPIO5, GPIO11, GPIO13, GPIO14, GPIO22,	I/O	GPIOs, *alternative: interrupt signals*

Pin Number	Signal	I/O	Comments
Pin row X17D			
55D, 56D, 57D, 58D, 60D, 61D, 62D, 63D, 65D, 66D, 67D, 68D, 70D	EGPIO2, EGPIO4, EGPIO5, EGPIO7 EGPIO10, EGPIO12, EGPIO13, EGPIO15, EGPIO19, EGPIO20, EGPIO21, EGPIO23, EGPIO26	I/O	Additional GPIOs generated by the MAX7301 IC with 7 interrupt-capable inputs for connection to a matrix keyboard
71D	SSP_EXTCLK	I	SSP external clock *alternative: GPIO 27*
72D	SSP_CLK	O	SSP clock signal *alternative: GPIO 23*
73D	SSP_SFRM	I/O	SSP frame signal *alternative: GPIO 24*
75D	FL_DIS	I	Signal to disable internal Flash
76D	H_SUSWKUP	I/O	USB controller /H_SUSWKUP
77D	D_SUSWKUP	I/O	USB controller /D_SUSWKUP
78D	OTG_LED	I/O	USB controller LED signal
80D	/INT_RTC	O	Interrupt output RTC

Table 46: GPIO Expansion Bus X17 Pin Assignment

The pin assignment on the phyCORE-PXA255, in conjunction with the expansion bus (X2) on the Development Board and the patch field on an expansion board, is as follows:

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
1A	CLKIN	BUS0	1A	BUS0	28A
3A	GPIO_2	BUS3	3A	BUS3	28B
4A	GPIO_0	BUS5	4A	BUS5	29A
5A	/CS_2	BUS6	5A	BUS6	29E
6A	/CS_4	BUS8	6A	BUS8	29D
8A	/WE	BUS11	8A	BUS11	30E
9A	A1	BUS13	9A	BUS13	30D
10A	A2	BUS14	10A	BUS14	30F
11A	A4	BUS16	11A	BUS16	31E
13A	A7	BUS19	13A	BUS19	32A
14A	A9	BUS21	14A	BUS21	32E
15A	A10	BUS22	15A	BUS22	32B
16A	A12	BUS24	16A	BUS24	33A
18A	A15	BUS27	18A	BUS27	33B
19A	D1				
20A	D2				
21A	D4				
23A	D7				
24A	A17	BUS37	24A	BUS37	35D
25A	A18	BUS38	25A	BUS38	35F
26A	A20	BUS40	26A	BUS40	36E
28A	A23	BUS43	28A	BUS43	37A
29A	D9				
30A	D10				
31A	D12				
33A	D15				
34A	DQM_1	BUS53	34A	BUS53	39A
35A	DQM_2	BUS54	35A	BUS54	39E
36A	A24	BUS56	36A	BUS56	39D
38A	D18	BUS59	19A	BUS29	34A
39A	D19	BUS61	20B	BUS31	34B
40A	D20	BUS62	21A	BUS32	34D
41A	D22	BUS64	22B	BUS34	35A
43A	D25	BUS67	29A	BUS45	37E
44A	D27	BUS69	30B	BUS47	37F

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
45A	D28	BUS70	31A	BUS48	38A
46A	D30	BUS72	32B	BUS50	38E
48A	RDY	BUS75	38A	BUS59	40E
49A	RDnWR	BUS77	39A	BUS61	40D
50A	DREQ_0	BUS78	40A	BUS62	40F
51A	DREQ_1	BUS80	41A	BUS64	41E
53A	/SDCKE_0	BUS83	43A	BUS67	42A
54A	/SDCKE_1	BUS85	44A	BUS69	42E
55A	/SDCLK_0	BUS86	45A	BUS70	42B
56A	/SDCLK_1	BUS88	46A	BUS72	43A
58A	/PCE_1	BUS91	48A	BUS75	43B
59A	/PCE_2	BUS93	49A	BUS77	44A
60A	/PWAIT	BUS94	50A	BUS78	44E
61A	/IOIS16	BUS96	51A	BUS80	44D
63A	/PREG	BUS99	53A	BUS83	45E
64A	/LAN_CS	BUS101	54A	BUS85	45D
65A	/LAN_DATA	BUS102	55A	BUS86	45F
66A	LAN_RDY	BUS104	56A	BUS88	46E
68A	L_PCLK	BUS107	58A	BUS91	47A
69A	L_LCLK	BUS109	59A	BUS93	47E
70A	L_FCLK	BUS126	60A	BUS94	47B
71A	L_PCLK	BUS128	61A	BUS96	48A
73A	L_DD3	BUS131	63A	BUS99	48B
74A	L_DD5	BUS133	64A	BUS101	49A
75A	L_DD6	BUS134	65A	BUS102	49E
76A	L_DD8	BUS136	66A	BUS104	49D
78A	L_DD11	BUS139	68A	BUS107	50E
79A	L_DD13	BUS141	69A	BUS109	50D
80A	L_DD14	BUS142	70A	BUS110	50F
1B	DEV_RESET	BUS1	1B	BUS1	28C
2B	GPIO_3	BUS2	2B	BUS2	28E
3B	GPIO_1	BUS4	3B	BUS4	28F
5B	/CS_3	BUS7	5B	BUS7	29B
6B	/CS_5	BUS9	6B	BUS9	29F
7B	/OE	BUS10	7B	BUS10	30A
8B	A0	BUS12	8B	BUS12	30B
10B	A3	BUS15	10B	BUS15	31A
11B	A5	BUS17	11B	BUS17	31B
12B	A6	BUS18	12B	BUS18	31F

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
13B	A8	BUS20	13B	BUS20	32C
15B	A11	BUS23	15B	BUS23	32F
16B	A13	BUS25	16B	BUS25	33C
17B	A14	BUS26	17B	BUS26	33E
18B	D0				
20B	D3				
21B	D5				
22B	D6				
23B	A16	BUS36	23B	BUS36	35B
25B	A19	BUS39	25B	BUS39	36A
26B	A21	BUS41	26B	BUS41	36B
27B	A22	BUS42	27B	BUS42	36F
28B	D8				
30B	D11				
31B	D13				
32B	D14				
33B	DQM_0	BUS52	33B	BUS52	38F
35B	DQM_3	BUS55	35B	BUS55	39B
36B	A25	BUS57	36B	BUS57	39F
37B	D16	BUS58	18B	BUS28	33F
38B	D17	BUS60	20A	BUS30	34E
40B	D21	BUS63	21B	BUS33	34F
41B	D23	BUS65	23A	BUS35	35E
42B	D24	BUS66	28B	BUS44	37C
43B	D26	BUS68	30A	BUS46	37B
45B	D29	BUS71	31B	BUS49	38C
46B	D31	BUS73	33A	BUS51	38B
47B	/CS_0	BUS74	37B	BUS58	40A
48B	/CS_1	BUS76	38B	BUS60	40B
50B	/SDCS_0	BUS79	40B	BUS63	41A
51B	/SDCS_1	BUS81	41B	BUS65	41B
52B	/SDCS_2	BUS82	42B	BUS66	41F
53B	/SDCS_3	BUS84	43B	BUS68	42C
55B	/SDCLK_2	BUS87	45B	BUS71	42F
56B	/SDRAS	BUS89	46B	BUS73	43C
57B	/SDCAS	BUS90	47B	BUS74	43E
58B	/PKSEL	BUS92	48B	BUS76	43F
60B	/PWE	BUS95	50B	BUS79	44B
61B	/POE	BUS97	51B	BUS81	44F
62B	/PIOR	BUS98	52B	BUS82	45A

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
63B	/PIOW	BUS100	53B	BUS84	45B
65B	LAN_IRQ	BUS103	55B	BUS87	46A
66B	/OTG_CS	BUS105	56B	BUS89	46B
67B	/OTG_INT1	BUS106	57B	BUS90	46F
68B	/OTG_INT2	BUS108	58B	BUS92	47C
70B	L_DD0				
71B	L_DD1				
72B	L_DD2				
73B	L_DD4				
75B	L_DD7				
76B	L_DD9				
77B	L_DD10				
78B	L_DD12				
80B	L_DD15	BUS127	60B	BUS95	47F
1C	VCC				
2C	VCC				
4C	VMMC				
5C	VBAT				
6C	OTG_5V	VBAT	6C	VBAT	2B
8C	/H_OC1	PFO	8C	PFO	3E
9C	/H_OC2	BOOT//BOOT	9C	BOOT//BOOT	3B
10C	/RESIN	/HDRESET	10C	/RESET	3D
11C	/RESET_OUT	/PORESET	11C	/RESOUT	4E
13C	NSSP_SFRM	GPIO2	13C	GPIO2	4F
14C	NSSP_CLK	GPIO4	14C	GPIO4	5C
15C	NSSP_TXD	GPIO5	15C	GPIO5	5E
16C	NSSP_RXD	GPIO7	16C	GPIO7	5F
18C	IR_TXD	GPIO10	18C	GPIO10	6E
19C	IR_RXD	GPIO12	19C	GPIO12	6F
20C	FF_IR_DETECT	GPIO13	20C	GPIO13	7A
21C	FF_/INVALID	GPIO15	21C	GPIO15	7B
23C	/ACRESET	GPIO18	23C	GPIO18	8A
24C	SYNC	GPIO20	24C	GPIO20	8B
25C	BITCLK	GPIO21	25C	GPIO21	8D
26C	SDATA_IN_1	GPIO23	26C	GPIO23	9A
28C	SDATA_IN_0	GPIO26	28C	GPIO26	9F
29C	SDATA_OUT	GPIO28	29C	GPIO28	10C
30C	SDA	GPIO29	30C	GPIO29	10E
31C	SCL	GPIO31	31C	GPIO31	10F

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
33C	/LAN_LED_A				
34C	/LAN_LED_B				
35C	LAN_TPI-				
36C	LAN_TPO-				
38C	OTG_ID	GPIO42	33C	GPIO34	11E
39C	PWM0	GPIO44	34C	GPIO36	11F
40C	PWM1	GPIO45	35C	GPIO37	12A
41C	/TRST	GPIO47	36C	GPIO39	12B
43C	H_DP2	GPIO50	38C	GPIO42	13A
44C	H_DM2	GPIO52	39C	GPIO44	13B
45C	MMC_CS_1	GPIO53	40C	GPIO45	13D
46C	MMC_CS_0	GPIO55	41C	GPIO47	14A
48C	GPIO_4	GPIO58	43C	GPIO50	14F
49C	GPIO_7	GPIO60	44C	GPIO52	15C
50C	GPIO_10	GPIO61	45C	GPIO53	15E
51C	GPIO_12	GPIO63	46C	GPIO55	15F
53C	GPIO_21	GPIO66	48C	GPIO58	16E
54C	EGPIO0	GPIO68	49C	GPIO60	16F
55C	EGPIO1	GPIO69	50C	GPIO61	17A
56C	EGPIO3	GPIO71	51C	GPIO63	17B
58C	EGPIO6	GPIO74	53C	GPIO66	18A
59C	EGPIO8	GPIO76	54C	GPIO68	18B
60C	EGPIO9				
61C	EGPIO11				
63C	EGPIO14				
64C	EGPIO16				
65C	EGPIO17				
66C	EGPIO18				
68C	EGPIO22				
69C	EGPIO24				
70C	EGPIO25	GPIO93	55C	GPIO69	18D
71C	EGPIO27	GPIO95	56C	GPIO71	19A
73C	SSP_RXD	GPIO98	58C	GPIO74	19F
74C	SSP_TXD				
75C	/CS_EGPIO				
76C	/CAN_CS				
78C	/CAN_INT				
79C	CANRXD	GPIO108	59C	GPIO76	20C
80C	CANTXD	GPIO109	60C	GPIO77	20E

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
1D	VCC				
2D	VCC				
4D	VCC1				
5D	VCC1				
6D	OTG_VBUS	VPD	6D	VPD	2D
7D	/H_PSW1	PFI	7D	PFI	2F
8D	/H_PSW2	/SRESET	8D	WDI	3A
10D	/RESET	/RESIN	10D	/RESIN	3F
11D	/BATT_FAULT	GPIO0	11D	GPIO0	4A
12D	/VCC_FAULT	GPIO1	12D	GPIO1	4B
13D	PWR_ENAB	GPIO3	13D	GPIO3	5A
15D	BT_CTS	GPIO6	15D	GPIO6	5B
16D	BT_RXD	GPIO8	16D	GPIO8	6A
17D	BT_TXD	GPIO9	17D	GPIO9	6C
18D	BT_RTS	GPIO11	18D	GPIO11	6B
20D	FF_/SHDN	GPIO14	20D	GPIO14	7E
21D	FL_/WP_PEN	GPIO16	21D	GPIO16	7D
22D	RS_RXD	GPIO17	22D	GPIO17	7F
23D	RS_TXD	GPIO19	23D	GPIO19	8E
25D	RS_RTS	GPIO22	25D	GPIO22	8F
26D	RS_CTS	GPIO24	26D	GPIO24	9E
27D	RS_DSR	GPIO25	27D	GPIO25	9B
28D	RS_DTR	GPIO27	28D	GPIO27	10A
30D	RS_RI	GPIO30	30D	GPIO30	10B
31D	RS_DCD	GPIO32	31D	GPIO32	11A
32D	USB_P	GPIO33	32D	GPIO33	11C
33D	USB_N	GPIO35	33D	GPIO35	11B
35D	LAN_TPI+				
36D	LAN_TPO+				
37D	OTG_DP1	GPIO41	35D	GPIO38	12E
38D	OTG_DM1	GPIO43	36D	GPIO40	12D
40D	TDI	GPIO46	37D	GPIO41	12F
41D	TDO	GPIO48	38D	GPIO43	13E
42D	TMS	GPIO49	40D	GPIO46	13F
43D	TCK	GPIO51	41D	GPIO48	14E
45D	MMC_CLK	GPIO54	42D	GPIO49	14B
46D	MMC_DAT	GPIO56	43D	GPIO51	15A
47D	MMC_CMD	GPIO57	45D	GPIO54	15B
48D	GPIO_5	GPIO59	46D	GPIO56	16A
50D	GPIO_11	GPIO62	47D	GPIO57	16C

phyCORE-PXA255		**Development Board Expansion Bus**		**Expansion Board Patch Field**	
51D	GPIO_13	GPIO64	48D	GPIO59	16B
52D	GPIO_14	GPIO65	50D	GPIO62	17E
53D	GPIO_22	GPIO67	51D	GPIO64	17D
55D	EGPIO2	GPIO70	52D	GPIO65	17F
56D	EGPIO4	GPIO72	53D	GPIO67	18E
57D	EGPIO5	GPIO73	55D	GPIO70	18F
58D	EGPIO7	GPIO75	56D	GPIO72	19E
60D	EGPIO10				
61D	EGPIO12				
62D	EGPIO13				
63D	EGPIO15				
65D	EGPIO19				
66D	EGPIO20				
67D	EGPIO21				
68D	EGPIO23				
70D	EGPIO26				
71D	SSP_EXTCLK	GPIO96	57D	GPIO73	19B
72D	SSP_CLK	GPIO97	58D	GPIO75	20A
73D	SSP_SFRM				
75D	FL_DIS				
76D	H_SUSWKUP				
77D	D_SUSWKUP				
78D	OTG_LED				
80D	/INT_RTC	GPIO110	60D	GPIO78	20B

Table 47: Signal Pin Assignment for the phyCORE-PXA255 / Development Board / Expansion Board

18 JTAG Interface (X29)

The PXA255 provides a JTAG interface for debuggers, emulators and boundary scan. All JTAG interface signals extend from the phyCORE plug connector to an ARM-compatible, dual row, 20-pin connector at X254. This connector is located on the left side above the phyCORE module.

The following table describes the pin assignment for the JTAG interface.

Signal	X29		Signal
VREF	**1**	**2**	VCC
/JTAG-RESET	**3**	**4**	GND
JTAG-TDI	**5**	**6**	GND
JTAG-TMS	**7**	**8**	GND
JTAG-TCK	**9**	**10**	GND
JTAG-RTCK	**11**	**12**	GND
JTAG-TDO	**13**	**14**	GND
RESET (System)	**15**	**16**	GND
N.C.	**17**	**18**	GND
N.C.	**19**	**20**	GND

Table 48: JTAG Connector X29 Pinout

19 Technical Specifications

The physical dimensions of the Development Board are represented in *Figure 40*.

PHYTEC is currently working on an enclosure for this Development Board with Expansion Board. The dimensions shown below are subject to change. The maximum height of all components, the inserted phyCORE module and with a display mounted on the PCB is ca. 40 mm.

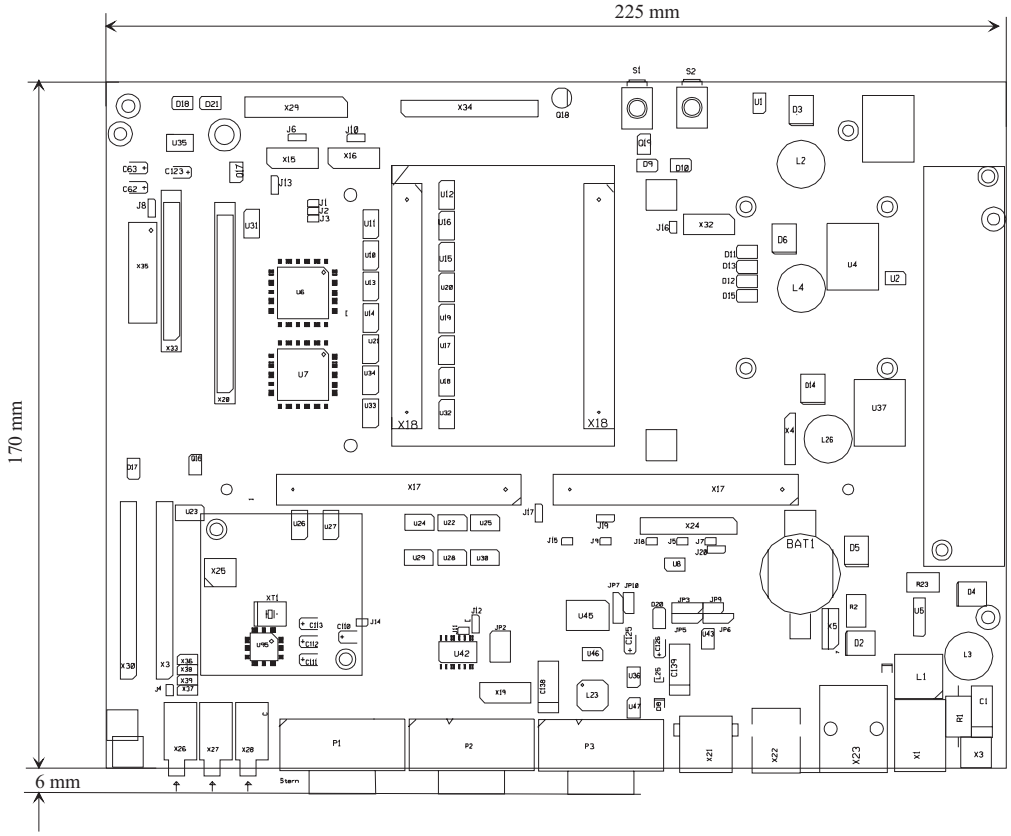


Figure 40: Physical Dimensions (Development Board)

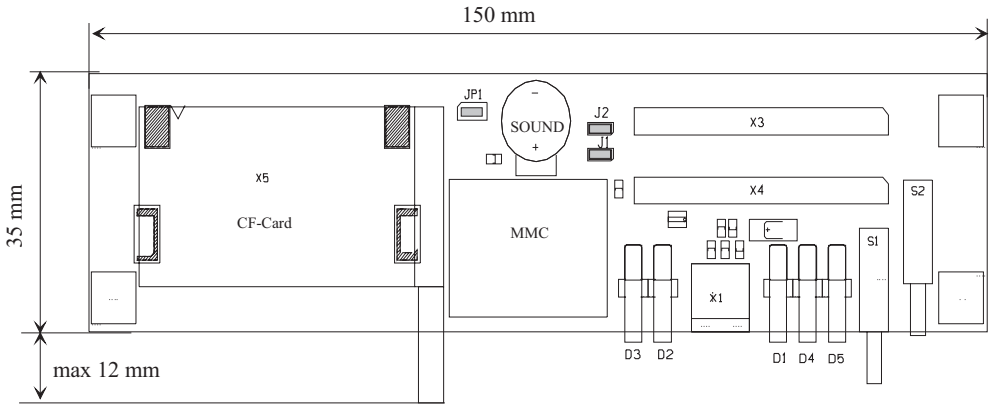


Figure 41: Physical Dimensions (Expansion Board)

Additional specifications:

- Dimensions (Development Board): 225 mm x 170 mm
- Dimensions (Expansion Board): 35 mm x 150 mm
- Weight: approximately 1000 grams
- Storage temperature: 0°C to +85°C
- Operating temperature: 0°C to +70°C
- Humidity: 95 % r.F. not condensed
- Operating voltage: 8 VDC – 24 VDC ±5 % supplied via power jack

- Power consumption:
  operating with peripheral components
  incl. LCD and hard disk min. 8.5 W, max 15 W

These specifications describe the standard configuration of the Development Board as of printing of this manual.

20 Hints for Handling the Module

- **Modifications on the phyCORE-PXA255 Development Board and Expansion Board**

Removal of various components is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-PXA255 into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected.

21 Component Placement Diagram

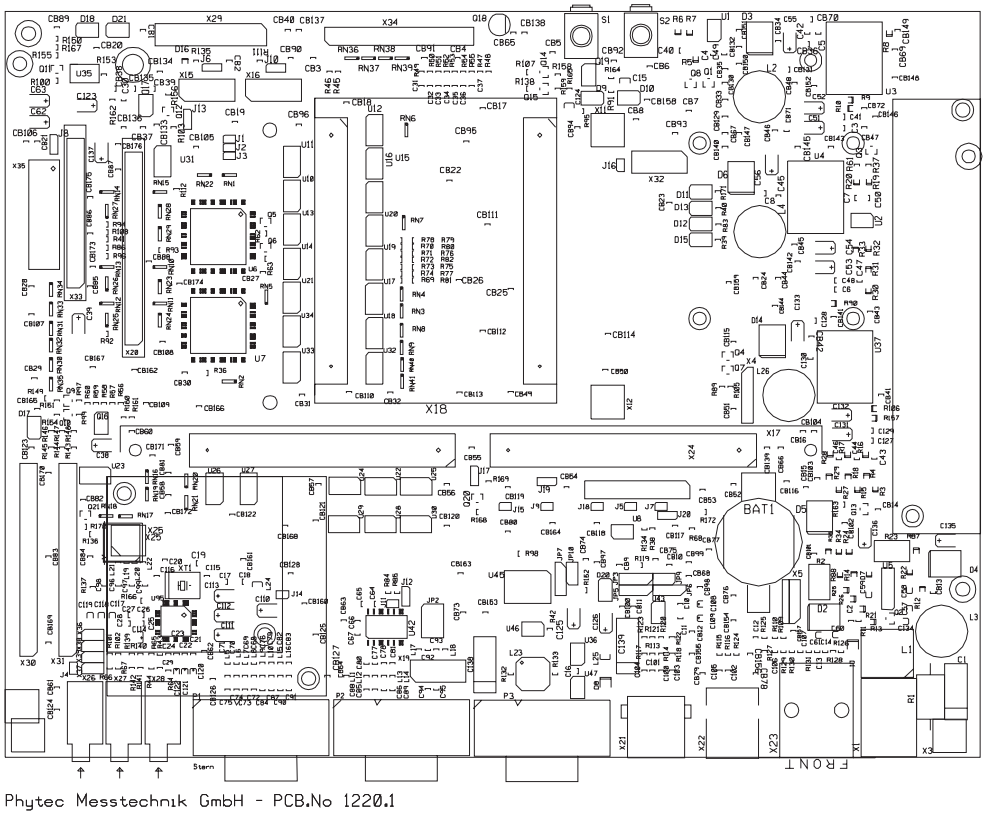


Figure 42: Component Placement Diagram Development Board (PCB Revision 1220.1)

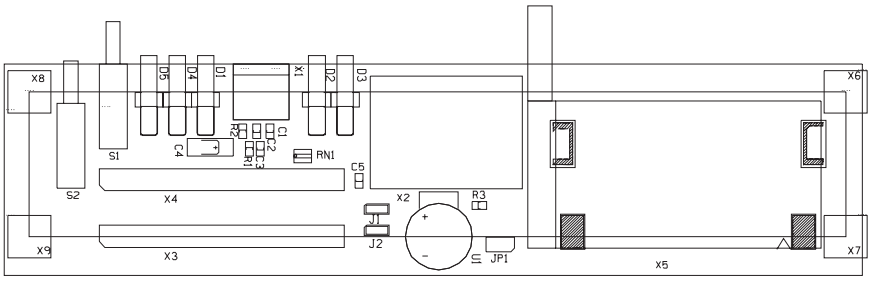


Figure 43: Component Placement Diagram Expansion Board

22 Revision History

Date	Version numbers	Changes in this manual
03-Oct.-2004	Manual L-657e_0 PCM-990 PCB# 1220.1/1220.2 PCM-985 PCB# 1222.1	First preliminary edition.

Appendices A

AI Hardware Revision

Index

Document: Development Board for phyCORE-PXA255
Document number: L-657e_0, Preliminary Edition November 2004

How would you improve this manual?

Did you find any mistakes in this manual? page

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