phyCORE®-MPC5676/57xx

Hardware Manual

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	EUROPE	NORTH AMERICA	FRANCE
Address:	PHYTEC Messtechnik GmbH Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA	PHYTEC France 17, place Saint-Etienne F-72140 Sillé-le-Guillaume FRANCE
Ordering Information:	+49 (6131) 9221-32 sales@phytec.de	+1 (800) 278-9913 sales@phytec.com	+33 (0)2 43 29 22 33 info@phytec.fr
Technical Support:	+49 (6131) 9221-31 support@phytec.de	+1 (206) 780-9047 support@phytec.com	support@phytec.fr
Fax:	+49 (6131) 9221-33	+1 (206) 780-9135	+33 (0)2 43 29 22 34
Web Site:	http://www.phytec.de http://www.phytec.eu	http://www.phytec.com	http://www.phytec.fr

	INDIA	CHINA
Address:	PHYTEC Embedded Pvt. Ltd. No. 1688, 25th A Cross 27th Main, 2nd Sector ,Opp. PEP School V2, HRS Layout Bangalore 560102 INDIA	PHYTEC Information Technology (Shenzhen) Co. Ltd. Suite 2611, Floor 26, Anlian Plaza, 4018 Jin Tian Road Futian District, Shenzhen CHINA 518026
Ordering Information:	+91-80-4086 7046/48 sales@phytec.in	+86 (755) 3395 5875 sales@phytec.cn
Technical Support:	+91-80-4086 7047 support@phytec.in	support@phytec.cn
Fax:		+86 (755) 3395 5999
Web Site:	http://www.phytec.in	http://www.phytec.cn

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List of Figures

List of Tables

Conventions, Abbreviations and Acronyms

This hardware manual describes the KSP-0180-0 System on Module in the following referred to as phyCORE®-MPC5676/57xx. The manual specifies the phyCORE®-MPC5676/57xx's design and function. Precise specifications for the Freescale Semiconductor MPC5676R microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Note: We refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products. Please read the paragraph "**Product Change Management and information in this manual on parts populated on the SOM"** within the *Preface.*

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The MSB and LSB of the data and address busses shown in the circuit diagram are based on the conventions of Freescale. Accordingly, D31 and A31 represent the LSB, while D0 and A0 represent the MSB.
  These conventions are also valid for the parallel I/O signals.
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connector on the undersides of the phyCORE-MPC5676/57xx System on Module.

Types of Signals

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of a signal.

Signal Type	Description	Abbr.
Power	Supply voltage input	PWR_I
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
IPU	Digital input with pull-up, must only be connected to GND. (jumper or open-collector output)	IPU
OC-Bidir PU	Open collector input/output with pull up	OC-BI
OC-Output	Open collector output without pull up, requires an external pull up	OC
5V Input PD	5 V tolerant input with pull down	5V_PD
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O

Table 1: Signal Types used in this Manual

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
CB	Carrier Board; used in reference to the phyCORE Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
GPI	General purpose input.
GPIO	General purpose input and output.
GPO	General purpose output.
IRAM	Internal RAM; the internal static RAM on the Freescale Semiconductor MPC5676R microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Extension Board
POR	Power-on reset
RTC	Real-time clock.
SMT	Surface mount technology.
SOM	System on Module; used in reference to the KSP-0180-0 /phyCORE®-MPC5676/57xx module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board.

Table 2: Abbreviations and Acronyms used in this Manual

Preface

As a member of PHYTEC's phyCORE® product family the phyCORE-MPC5676/57xx is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE® module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html

or

www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyCORE has the following structure:

KSP-0180-x (x=Version)

Product Specific Information and Technical Support

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phyCORE-MPC56xx_57xx.html or
http://www.phytec.eu/europe/support/faq/faq-phyCORE-MPC56xx_57xx.html

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE®-MPC5676/57xx

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM / SBC

When buying a PHYTEC SOM / SBC, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating longevity of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Change management in case of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

1 Introduction

The phyCORE-MPC5676/57xx belongs to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments approximately 20 % of all pin header connectors on the phyCORE bus are dedicated to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC5676/57xx is a subminiature (58 mm x 82 mm) insert-ready System on Module populated with the Freescale Semiconductor MPC5676R microcontroller. Its universal design enables its insertion in a wide range of embedded applications.

Precise specifications for the controller populating the board can be found in the applicable controller reference manual or datasheet. The descriptions in this manual are based on the Freescale Semiconductor MPC5676R. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC5676/57xx.

1.1 Features of the phyCORE-MPC5676/57xx

The phyCORE-MPC5676/57xx offers the following features:

- Subminiature System on Module (58 mm x 82 mm) achieved through modern SMD technology
- Populated with the Freescale Semiconductor MPC5676R/MPC5674F/MPC57xx microcontroller (BGA516 packaging)
- Controller signals and ports extend to two high-density (0.5 mm) Samtec connectors aligning two sides of the board enabling the phyCORE-MPC5676/57xx to be plugged like a "big chip" into target application
- FPGA ports extend to a third high-density (0.5 mm) Samtec connector placed on short side of the Module

1.1.1 Internal Features of the MPC5676R

- 32-bit Dual Power Architecture® 200z7 cores, up to 2 x 180MHz clock frequency
- 6 MB int. Flash memory
- 32ch eMIOS
- 3x +32 eTPU
- 64 channel 12-bit quad ADC
- 4 x FlexCAN
- 3-ch.eSCI
- 5-ch.DSPI
- 2-ch. FlexRay
- 12 decimation filters
- 384KB SRAM
- EBI (External Bus Interface)

1.2 Memory configuration of the phyCORE-MPC5676/57xx

- SRAM: 2 MByte to 8 MByte Synchronous Flow-Through Burst-RAM, 32-bit access
- Flash: 2 MByte to 8 MByte asynchronous standard Flash, 32-bit acces
- 32k kB SPI EEPROM
- 16Mbyte Dual/Quad SPI NOR-Flash (FPGA configuration memory)

1.3 Other Board-Level Features

- All controller and FPGA required supplies are generated on board
- Voltage Supervisor IC
- UART: two RS-232 transceivers for channel A and B (RxD/TxD), also usable as TTL
- Ethernet: 10/100 Mbit/s LAN9221I , 16-bit EBI access from CPU
- Bootconfig pins for boot source selection (int. Flash (standard), ext. Flash)
- Support of standard 14 pin debug interface through JTAG connector
- Xilinx Artix7 FPGA (XC7A35T...XCA100T)
- FPGA configuration memory programmable via JTAG
- SPI-RTC battery-buffered
- Watchdog
- Industrial temperature range (-40 °C to +85 °C)
- Free I/Os from CPU and 101 I/Os FPGA (Bank14/15/34) available on phyCORE-connector

1.4 Block Diagram

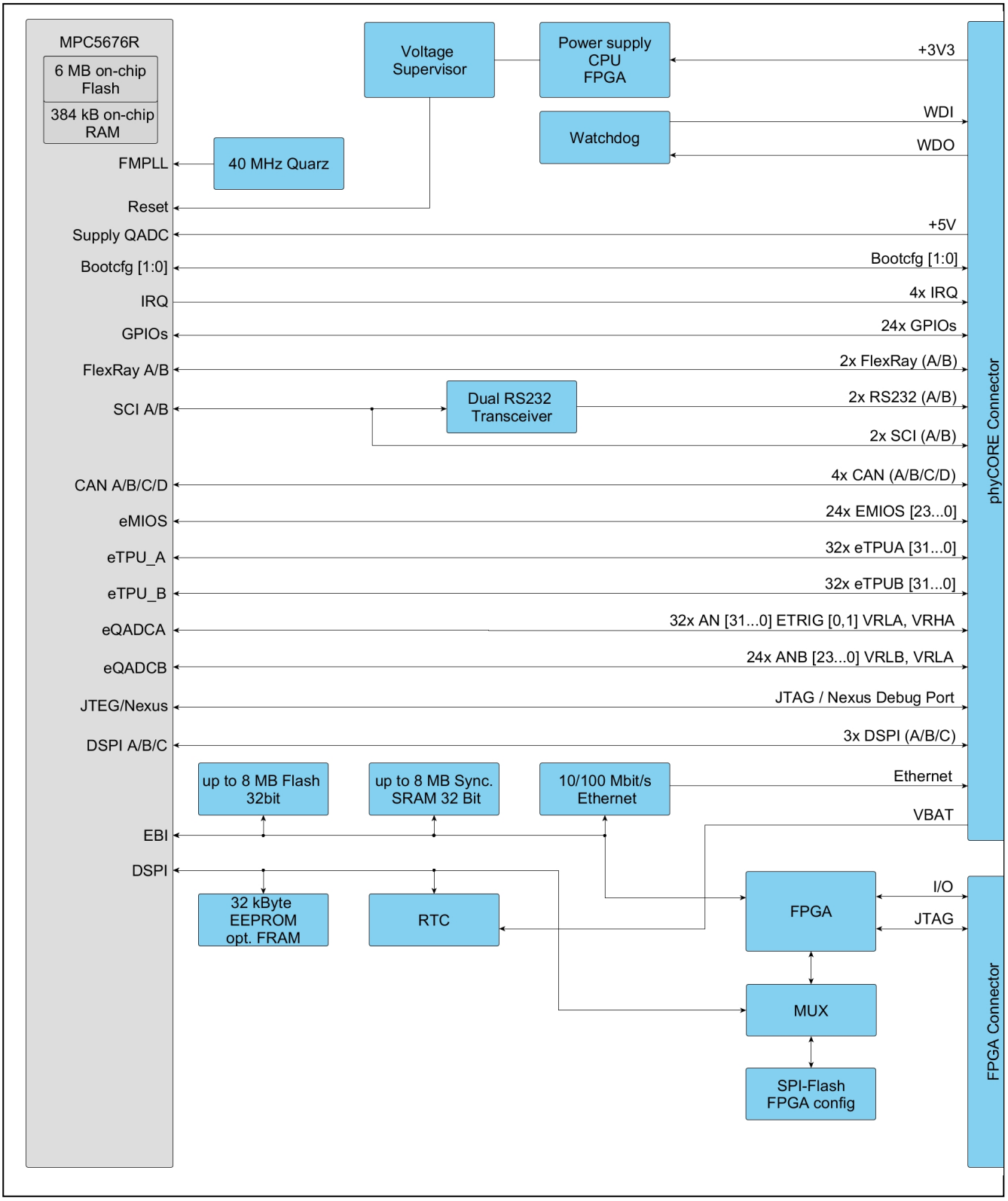

Figure 1: Block Diagram of the phyCORE-MPC5676/57xx

1.5 phyCORE-MPC5676/57xx Component Placement

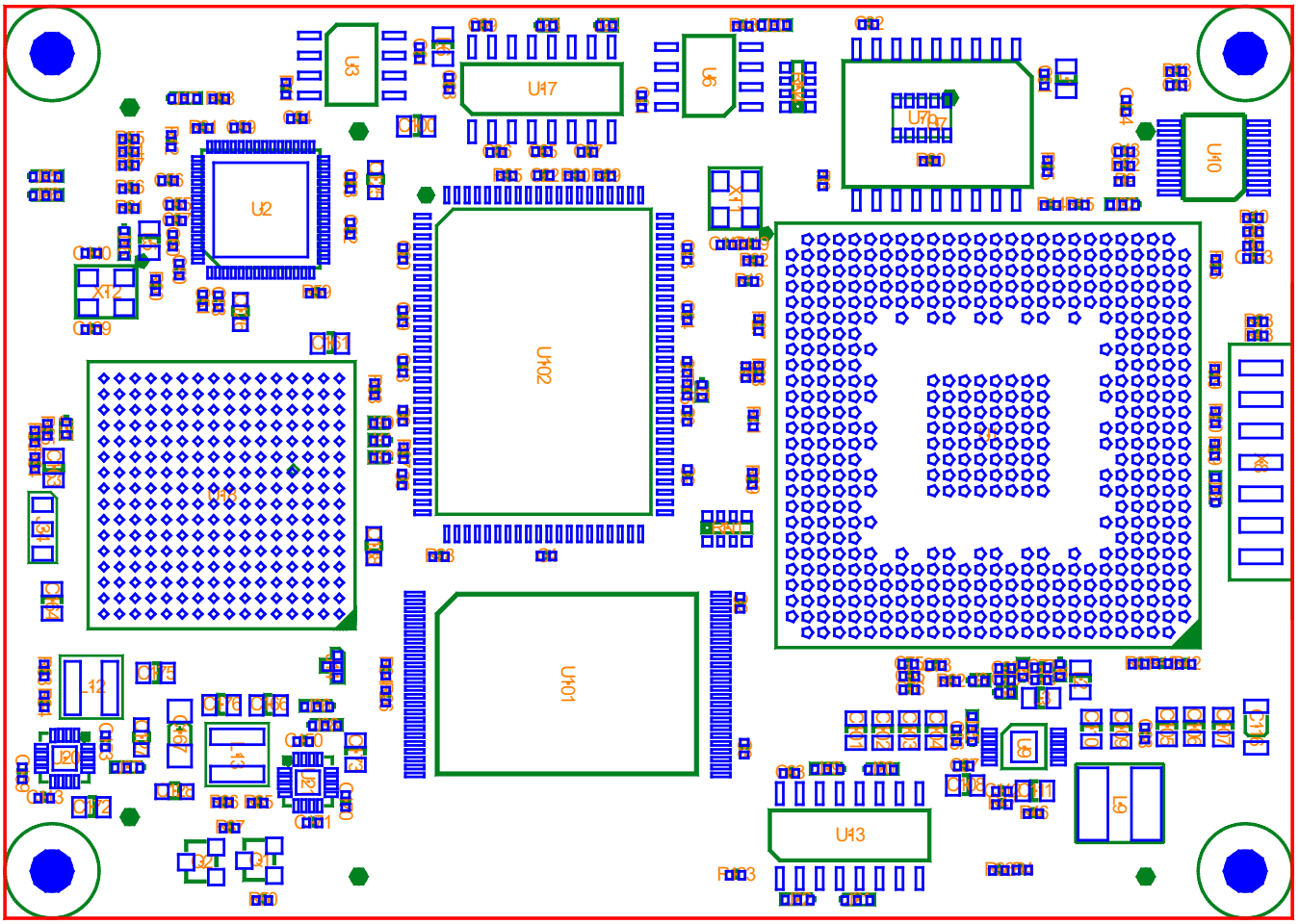

Figure 2: phyCORE-MPC5676/57xx Component Placement (top view)

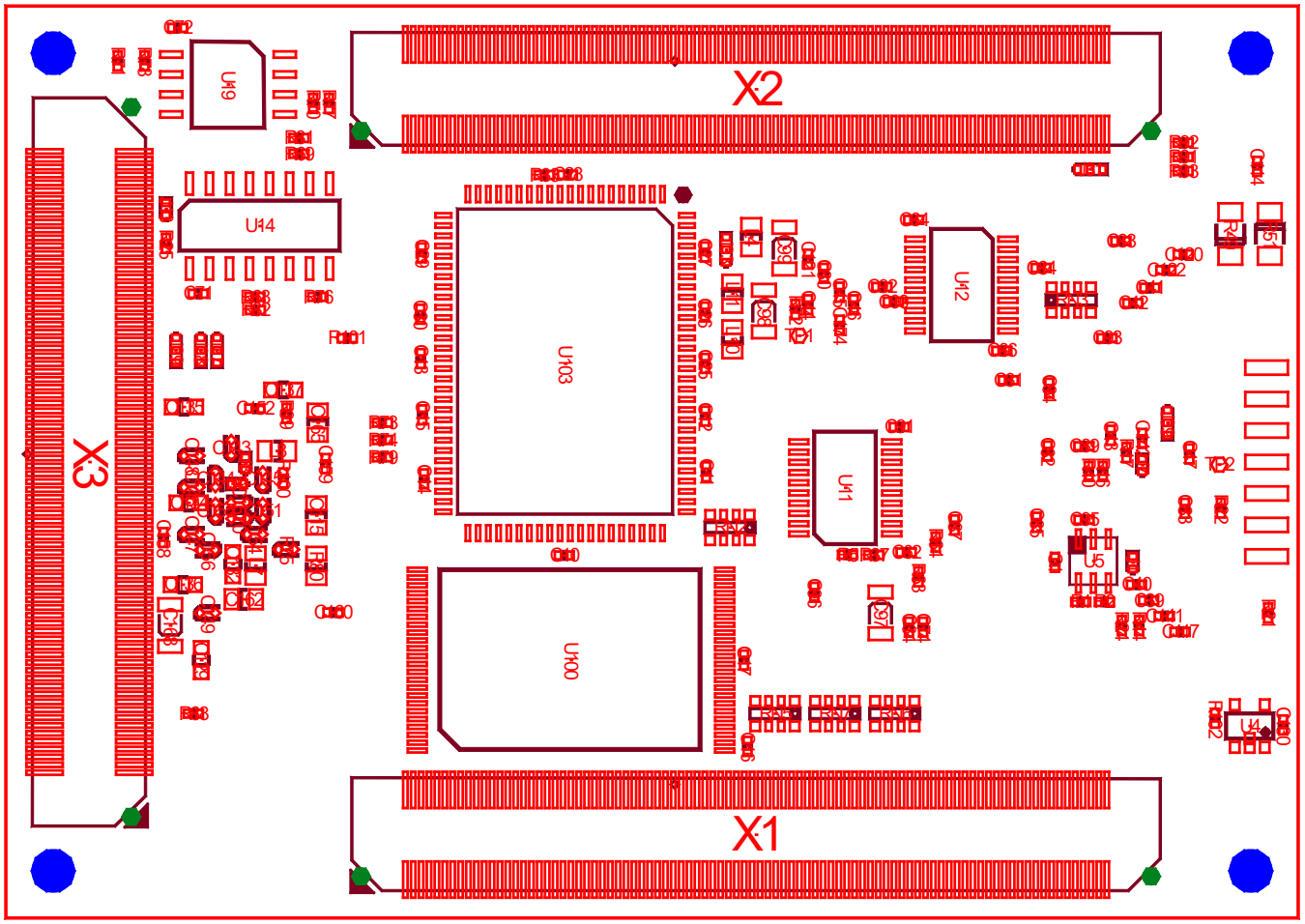

Figure 3: phyCORE-MPC5676/57xx Component Placement (top view)

1.6 Minimum Requirements to operate the phyCORE-MPC5676/57xx

Basic operation of the phyCORE-MPC5676/57xx only requires supply of a +3.3 V and a +5 V input voltage with TBD A load and the corresponding GND connection.

These supply pins are located at the phyCORE-Connector X1,X3:

VCC_3V3:	X2	A1, B1, B2,
	X3	B1, B2, B3
VCC_5V	X2	A4

Connect all +3.3 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND:	X2	A2, A7,B3,B8
Corresponding GND:	X3	B4, B9,B14

Please refer to *section 2* for information on additional GND Pins located at the phyCORE-Connector X1.

Caution!
We recommend connecting all available +3.3 V and +5V input pins to the power supply system on a custom carrier board housing the phyCORE-MPC5676/57xx and at least the matching number of GND pins neighboring the +3.3 V pins and +5V.

In addition, proper implementation of the phyCORE-MPC5676/57xx module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to *section 4* for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals selected extend to surface mount technology (SMT) connectors (0.5 mm) lining two sides of the module (referred to as phyCORE-Connector). This allows the phyCORE-MPC5676/57xx to be plugged into any target application like a "big chip".

The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number.

The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number with prefixed Connector Reference (X1, X2, and X3). Pin X1A1, for example, is located in the upper left hand corner of the matrix looking down through the top of the SOM (refer to *Figure 4*).

The numbered matrix can be aligned with the phyCORE-MPC5676/57xx (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-Connector as well as the mating connector on the phyCORE Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

The following figure illustrates the numbered matrix system. It shows a phyCORE-MPC5676/57xx with all three SMT phyCORE-Connectors on its underside (defined as dotted lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-MPC5676/57xx module showing the phyCORE-Connector mounted on the underside of the module's PCB.

Table 3 to *Table 8* provide an overview of the pinout of the different phyCORE-Connectors X1,X2,X3 with signal names and descriptions specific to the phyCORE-MPC5676/57xx. It also provides the appropriate voltage domain, signal type (ST) and a functional grouping of the signals. The signal type includes also information about the signal. A description of the signal types can be found in *Table 1*.

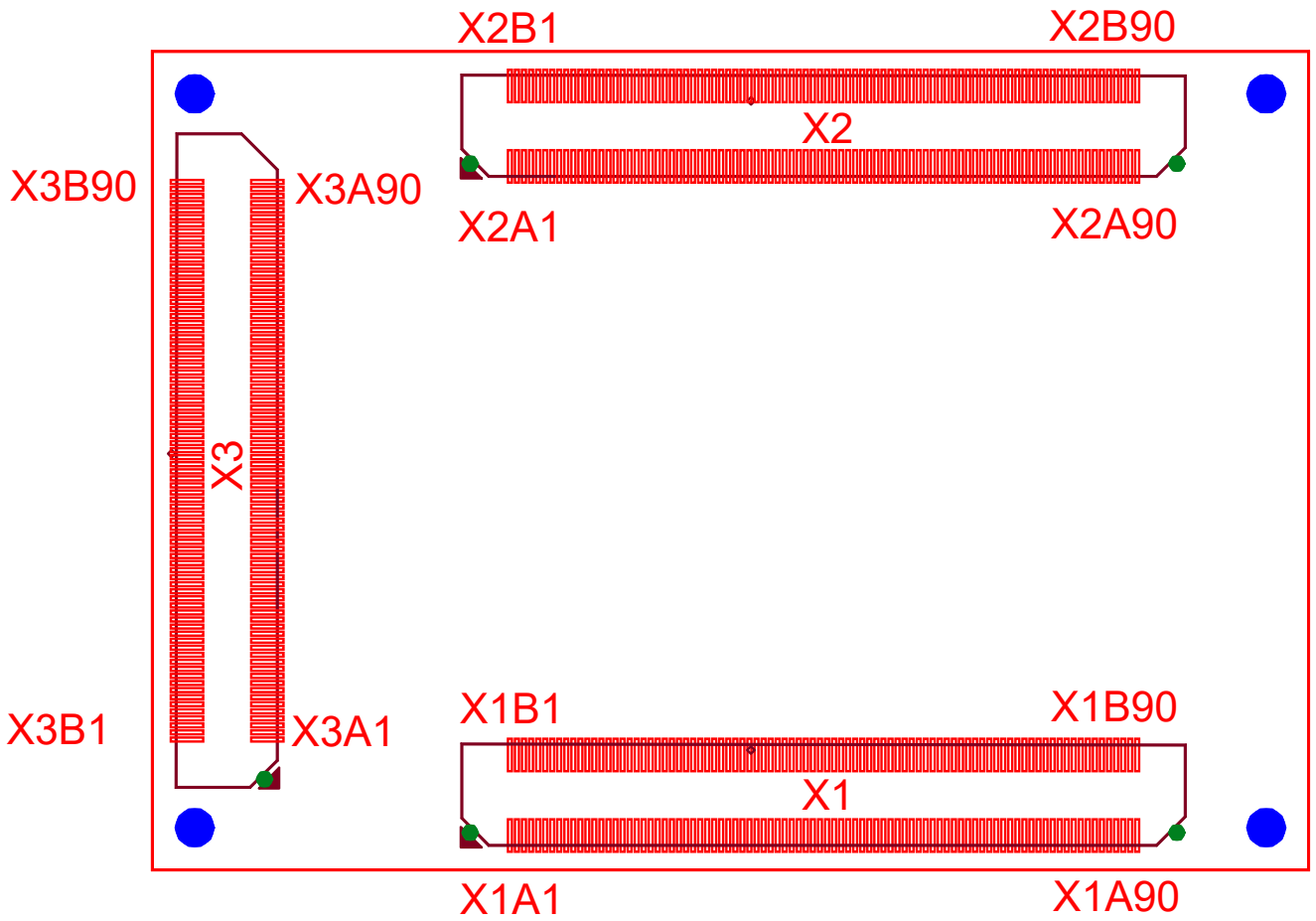

Figure 4: Pinout of the phyCORE-Connector (top view)

The Freescale Semiconductor MPC5676R is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Freescale Semiconductor MPC5676R Reference Manual* for details on the functions and features of controller signals and port pins.

Caution:
Most of the controller pins have multiple multiplexed functions. Because most of these pins are connected directly to the phyCORE-Connector the functions are also available there. Signal names and descriptions in *Table 3* to *Table 8* however, are in regard to the specification of the phyCORE-MPC5676/57xx and the functions defined therein. Please refer to the *MPC5676R Reference Manual*, or the schematic to get to know about alternative functions. In order to utilize a specific pin's alternative function the corresponding registers must be configured within the appropriate driver of the BSP. To support all features of the phyCORE-MPC5676/57xx Carrier Board a few changes have been made in the BSP delivered with the module.

Pin #	Signal	ST	Voltage domain	Description
X1A1	EXTCLK	I		Optional external clock input (R72)
X1A2	DGND	-		Ground 0 V
X1A3	IRQ2	I/O		IRQ2 interrupt (GPIO211) **used for onboard Ethernet -PHY U2)**
X1A4	IRQ3	I/O		IRQ3 interrupt (GPIO212)
X1A5	IRQ4	I/O		IRQ4 interrupt (GPIO208)
X1A6	IRQ5	I/O		IRQ5 interrupt (GPIO209)
X1A7	DGND	-		Ground 0 V
X1A8	TCRCLKB_IRQ6			eTPU B TCR clock (GPIO146)
X1A9	ETPUB26	I/O		eTPU B channel 26 (GPIO173)
X1A10	ETPUB28	I/O		eTPU B channel 28 (GPIO175)
X1A11	ETPUB30	I/O		eTPU B channel 30 (GPIO177)
X1A12	DGND	-		Ground 0 V
X1A13	ETPUB24	I/O		eTPU B channel 24 (GPIO171)
X1A14	ETPUB22	I/O		eTPU B channel 22 (GPIO169)
X1A15	ETPUB20	I/O		eTPU B channel 20 (GPIO167)
X1A16	ETPUB18	I/O		eTPU B channel 18 (GPIO165)
X1A17	DGND	-		Ground 0 V
X1A18	ETPUB16	I/O		eTPU B channel 16 (GPIO163)
X1A19	ETPUB14	I/O		eTPU B channel 14 (GPIO161)
X1A20	ETPUB12	I/O		eTPU B channel 12 (GPIO159)
X1A21	ETPUB10	I/O		eTPU B channel 10 (GPIO157)
X1A22	DGND	-		Ground 0 V
X1A23	ETPUB8	I/O		eTPU B channel 8 (GPIO155)
X1A24	ETPUB6	I/O		eTPU B channel 6 (GPIO153)
X1A25	ETPUB4	I/O		eTPU B channel 4 (GPIO151)
X1A26	ETPUB2	I/O		eTPU B channel 2 (GPIO149)
X1A27	DGND	-		Ground 0 V
X1A28	GPIO441	I/O		GPIO441
X1A29	GPIO443	I/O		GPIO443
X1A30	GPIO445	I/O		GPIO445
X1A31	GPIO447	I/O		GPIO447
X1A32	DGND	-		Ground 0 V
X1A33	GPIO457	I/O		GPIO457
X1A34	GPIO459	I/O		GPIO459
X1A35	EQADC_ANB23	I		eQADC B analog input 23
X1A36	EQADC_ANB21	I		eQADC B analog input 21
X1A37	AGND	-		Analog Ground 0 V

Table 3: Pinout of the phyCORE-Connector X1, Row A

Pin #	Signal	ST	Voltage Domain	Description
X1A38	EQADC_ANB19	I		eQADC B analog input 19
X1A39	EQADC_ANB17	I		eQADC B analog input 17
X1A40	EQADC_ANB15	I		eQADC B analog input 15
X1A41	EQADC_ANB13	I		eQADC B analog input 13
X1A42	AGND	-		Analog Ground 0 V
X1A43	EQADC_ANB11	I		eQADC B analog input 11
X1A44	EQADC_ANB9	I		eQADC B analog input 9
X1A45	EQADC_ANB7	I		eQADC B analog input 7
X1A46	EQADC_ANB5	I		eQADC B analog input 5
X1A47	AGND	-		Analog Ground 0 V
X1A48	EQADC_ANB3	I		eQADC B analog input 3
X1A49	EQADC_ANB1	I		eQADC B analog input 1
X1A50	EQADC_VRHB	I		ADC B Voltage reference high **refer to jumper J3-6**
X1A51	EQADC_VRLB	I		ADC B Voltage reference low **refer to jumper j3-6**
X1A52	AGND	-		Analog Ground 0 V
X1A53	EQADC_AN39	I		eQADC analog input 39 (GPIO451)
X1A54	EQADC_AN37	I		eQADC analog input 37 (GPIO450)
X1A55	EQADC_AN35	I		eQADC analog input 35 (GPIO449)
X1A56	EQADC_AN33	I		eQADC analog input 33 (GPIO448)
X1A57	AGND	-		Analog Ground 0 V
X1A58	EQADC_AN31	I		eQADC analog input 31 (GPIO465)
X1A59	EQADC_AN29	I		eQADC analog input 29 (GPIO464)
X1A60	EQADC_AN27	I		eQADC analog input 27 (GPIO463)
X1A61	EQADC_AN25	I		eQADC analog input 25 (GPIO466)
X1A62	AGND	-		Analog Ground 0 V
X1A63	EQADC_AN23	I		eQADC analog input 23
X1A64	EQADC_AN21	I		eQADC analog input 21
X1A65	EQADC_AN19	I		eQADC analog input 19
X1A66	EQADC_AN17	I		eQADC analog input 17
X1A67	AGND	-		Analog Ground 0 V
X1A68	EQADC_AN15	I		eQADC analog input 15
X1A69	EQADC_AN13	I		eQADC analog input 13
X1A70	EQADC_AN11	I		eQADC analog input 11
X1A71	EQADC_AN9	I		eQADC analog input 9
X1A72	AGND	-		Analog Ground 0 V
X1A73	EQADC_AN7	I		eQADC analog input 7
X1A74	EQADC_AN5	I		eQADC analog input 5

Table 3: Pinout of the phyCORE-Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1A75	EQADC_AN3	I		eQADC analog input 3
X1A76	EQADC_AN1	I		eQADC analog input 1
X1A77	AGND	-		Analog Ground 0 V
X1A78	TCRCLKA_IRQ7			eTPU A TCR clock (GPIO113)
X1A79	ETPUA30	I/O		eTPU A channel 30 (GPIO144)
X1A80	ETPUA28	I/O		eTPU A channel 28 (GPIO142)
X1A81	ETPUA26_IRQ14	I/O		eTPU A channel 26 (GPIO140)
X1A82	DGND	-		Ground 0 V
X1A83	ETPUA24_IRQ12	I/O		eTPU A channel 24 (GPIO138)
X1A84	ETPUA22_IRQ10	I/O		eTPU A channel 22 (GPIO136)
X1A85	ETPUA20_IRQ8	I/O		eTPU A channel 20 (GPIO134)
X1A86	ETPUA18	I/O		eTPU A channel 18 (GPIO132)
X1A87	DGND	-		Ground 0 V
X1A88	ETPUA16	I/O		eTPU A channel 16 (GPIO130)
X1A89	ETPUA14	I/O		eTPU A channel 14 (GPIO128)
X1A90	ETPUA12	I/O		eTPU A channel 12 (GPIO126)

Table 3: Pinout of the phyCORE-Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B1	ENGCLK	O		EBI engineering clock output
X1B2	DGND	-		Ground 0 V
X1B3	CLKOUT	O		EBI system clock output
X1B4	BOOTCFG0	I		Boot configuration Input0 **refer to Jumper J21, J22 for bootmodes**
X1B5	BOOTCFG1	I		Boot configuration Input1 **refer to Jumper J21, J22 for bootmodes**
X1B6	ETPUB31	I/O		eTPU B channel 31 (GPIO178)
X1B7	ETPUB29	I/O		eTPU B channel 29 (GPIO176)
X1B8	ETPUB27	I/O		eTPU B channel 27 (GPIO174)
X1B9	DGND	-		Ground 0 V
X1B10	NC	-		Not connected
X1B11	ETPUB25	I/O		eTPU B channel 25 (GPIO172)
X1B12	ETPUB23	I/O		eTPU B channel 23 (GPIO170)
X1B13	ETPUB21	I/O		eTPU B channel 21 (GPIO168)
X1B14	DGND	-		Ground 0 V
X1B15	ETPUB19	I/O		eTPU B channel 19 (GPIO166)
X1B16	ETPUB17	I/O		eTPU B channel 17 (GPIO164)
X1B17	ETPUB15	I/O		eTPU B channel 15 (GPIO162)

Table 4: Pinout of the phyCORE-Connector X1, Row B

Pin #	Signal	ST	Voltage Domain	Description
X1B18	ETPUB13	I/O		eTPU B channel 13 (GPIO160)
X1B19	DGND	-		Ground 0 V
X1B20	ETPUB11	I/O		eTPU B channel 11 (GPIO158)
X1B21	ETPUB9	I/O		eTPU B channel 9 (GPIO156)
X1B22	ETPUB7	I/O		eTPU B channel 7 (GPIO154)
X1B23	ETPUB5	I/O		eTPU B channel 5 (GPIO152)
X1B24	DGND	-		Ground 0 V
X1B25	ETPUB3	I/O		eTPU B channel 3 (GPIO150)
X1B26	ETPUB1	I/O		eTPU B channel 1 (GPIO148)
X1B27	ETPUB0	I/O		eTPU B channel 0 (GPIO147)
X1B28	GPIO440	I/O		GPIO440
X1B29	DGND	-		Ground 0 V
X1B30	GPIO442	I/O		GPIO442
X1B31	GPIO444	I/O		GPIO444
X1B32	GPIO446	I/O		GPIO446
X1B33	GPIO456	I/O		GPIO456
X1B34	DGND	-		Ground 0 V
X1B35	GPIO458	I/O		GPIO458
X1B36	EQADC_ANB22	I		eQADC B analog input 22
X1B37	EQADC_ANB20	I		eQADC B analog input 20
X1B38	EQADC_ANB18	I		eQADC B analog input 18
X1B39	AGND	-		Analog Ground 0 V
X1B40	EQADC_ANB16	I		eQADC B analog input 16
X1B41	EQADC_ANB14	I		eQADC B analog input 14
X1B42	EQADC_ANB12	I		eQADC B analog input 12
X1B43	EQADC_ANB10	I		eQADC B analog input 10
X1B44	AGND	-		Analog Ground 0 V
X1B45	EQADC_ANB8	I		eQADC B analog input 8
X1B46	EQADC_ANB6	I		eQADC B analog input 6
X1B47	EQADC_ANB4	I		eQADC B analog input 4
X1B48	EQADC_ANB2	I		eQADC B analog input 2
X1B49	AGND	-		Analog Ground 0 V
X1B50	EQADC_ANB0	I		eQADC B analog input 0
X1B51	EQADC_AN38	I		eQADC analog input 38(GPIO460)
X1B52	EQADC_AN36	I		eQADC analog input 36(GPIO461)

Table 4: Pinout of the phyCORE-Connector X1, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B53	EQADC_AN34	I		eQADC analog input 34(GPIO462)
X1B54	AGND	-		Analog Ground 0 V
X1B55	EQADC_AN32	I		eQADC analog input 32 (GPIO455)
X1B56	EQADC_AN30	I		eQADC analog input 30 (GPIO454)
X1B57	EQADC_AN28	I		eQADC analog input 28 (GPIO453)
X1B58	EQADC_AN26	I		eQADC analog input 26 (GPIO452)
X1B59	AGND	-		Analog Ground 0 V
X1B60	EQADC_VRHA	I		ADC A Voltage ref. high **refer to Jumper J3-6**
X1B61	EQADC_VRLA	I		ADC A Voltage ref. low **refer to Jumper J3-6**
X1B62	EQADC_AN24	I		eQADC analog input 24
X1B63	EQADC_AN22	I		eQADC analog input 22
X1B64	AGND	-		Analog Ground 0 V
X1B65	EQADC_AN20	I		eQADC analog input 20
X1B66	EQADC_AN18	I		eQADC analog input 18
X1B67	EQADC_AN16	I		eQADC analog input 16
X1B68	EQADC_AN14	I		eQADC analog input 14
X1B69	AGND	-		Analog Ground 0 V
X1B70	EQADC_AN12	I		eQADC analog input 12
X1B71	EQADC_AN10	I		eQADC analog input 10
X1B72	EQADC_AN8	I		eQADC analog input 8
X1B73	EQADC_AN6	I		eQADC analog input 6
X1B74	AGND	-		Analog Ground 0 V
X1B75	EQADC_AN4	I		eQADC analog input 4
X1B76	EQADC_AN2	I		eQADC analog input 2
X1B77	EQADC_AN0	I		eQADC analog input 0
X1B78	ETPUA31	I/O		eTPU A channel 31 (GPIO145)
X1B79	DGND	-		Ground 0 V
X1B80	ETPUA29	I/O		eTPU A channel 29 (GPIO143)
X1B81	ETPUA27_IRQ15	I/O		eTPU A channel 27 (GPIO141)
X1B82	ETPUA25_IRQ13	I/O		eTPU A channel 25 (GPIO139)
X1B83	ETPUA23_IRQ11	I/O		eTPU A channel 23 (GPIO137)
X1B84	DGND	-		Ground 0 V
X1B85	ETPUA21_IRQ9	I/O		eTPU A channel 21 (GPIO135)
X1B86	ETPUA19	I/O		eTPU A channel 19 (GPIO133)
X1B87	ETPUA17	I/O		eTPU A channel 17 (GPIO131)
X1B88	ETPUA15	I/O		eTPU A channel 15 (GPIO129)
X1B89	DGND	-		Ground 0 V
X1B90	ETPUA13	I/O		eTPU A channel 13 (GPIO127)

Table 4: Pinout of the phyCORE-Connector X1, Row B (continued)

Pin #	Signal	ST	Voltage domain	Description
X2A1	VCC_3V3	PWR_I		+3,3 V Primary Voltage Supply Input
X2A2	DGND	-		Ground 0 V
X2A3	VCC_5V	PWR_I		5 V Primary Voltage Supply Input
X2A4	VBAT	PWR_I		external battery input **(for RTC U7)**
X2A5	PWRGOOD	O		Power Good logic output signal U10 **(VCC_1V2 , VCC_3V3 , VCC_5V , opt. V3V3F)**
X2A6	WKPCFG	I		WKPCFG_NMI_GPIO213 **(R16/R40)**
X2A7	DGND	-		Ground 0 V
X2A8	/RESET	OC-Bidir PU		Reset I/O of the phyCORE supervisor U10
X2A9	/RSTOUT	I		Reset output of the MPC
X2A10	EMIOS1	I/O		eMIOS channel 1 (GPIO180)
X2A11	EMIOS3	I/O		eMIOS channel 3 (GPIO182)
X2A12	DGND			Ground 0 V
X2A13	EMIOS6	I/O		eMIOS channel 6 (GPIO185)
X2A14	SCIB_RX	I		Receive line of eSCI channel B (GPIO92) **refer to J24**
X2A15	SCIB_TX	O		Transmit line of eSCI channel B (GPIO91)
X2A16	CANA_TX	O		FlexCAN A transmit line (GPIO83)
X2A17	DGND	-		Ground 0 V
X2A18	CANB_TX	O		FlexCAN B transmit line (GPIO85)
X2A19	CANB_RX	I		FlexCAN B receive line (GPIO86)
X2A20	CAND_RX	I		FlexCAN D receive line (GPIO247)
X2A21	CAND_TX	O		FlexCAN D transmit line (GPIO246)
X2A22	DGND	-		Ground 0 V
X2A23	TXDB_RS232	O		TxD eSCI B RS232 (U17)
X2A24	RXDB_RS232	I		RxD eSCI B RS232 (U17) **refer to J24**
X2A25	EMIOS9	I/O		eMIOS channel 9 (GPIO188)
X2A26	EMIOS11	I/O		eMIOS channel 11 (GPIO190)
X2A27	DGND	-		Ground 0 V
X2A28	EMIOS14_IRQ0	I/O		eMIOS channel 14 (GPIO193)
X2A29	EMIOS16	I/O		eMIOS channel 16 (GPIO195)
X2A30	EMIOS18	I/O		eMIOS channel 17 (GPIO196)
X2A31	EMIOS20	I/O		eMIOS channel 20 (GPIO199)
X2A32	DGND	-		Ground 0 V
X2A33	EMIOS22	I/O		eMIOS channel 22 (GPIO201)
X2A34	EMIOS23	I/O		eMIOS channel 23 (GPIO202)
X2A35	ETH_SPEED	O		ETH output signal for SPEED-LED
X2A36	EQADC_ETRIG1	I/O		eQADC trigger input (GPIO101)
X2A37	DGND	-		Ground 0 V

Table 5: Pinout of the phyCORE-Connector X2, Row A

Pin #	Signal	ST	Voltage Domain	Description
X2A38	/RTC_IRQ	OC		Open Drain RTC IRQ Output (U7)
X2A39	GPIO204	I/O		GPIO204
X2A40	GPIO433	I/O		GPIO433
X2A41	GPIO435	I/O		GPIO435
X2A42	DGND	-		Ground 0 V
X2A43	GPIO437	I/O		GPIO437
X2A44	SPIA_SIN	I		DSPI A data input (GPIO94)
X2A45	SPIA_SOUT	O		DSPI A data output (GPIO95)
X2A46	SPIA_CS1	O		DSPI A chip select 1 (GPIO97)
X2A47	DGND	-		Ground 0 V
X2A48	SPIA_CS4	O		DSPI A chip select 4 (GPIO100)
X2A49	SPIB_SIN	I		DSPI B data input (GPIO103)
X2A50	SPIB_SOUT	O		DSPI B data output (GPIO104)
X2A51	SPIB_CS2_SOUTC	O		DSPI B chip select 2 (GPIO107)
X2A52	DGND	-		Ground 0 V
X2A53	NC	-		Not connected
X2A54	SPIB_CS4_SCKC	O		DSPI B chip select 4 (GPIO109)
X2A55	SPIC_SCK	O		DSPI C clock (GPIO235)
X2A56	SPIC_SIN	I		DSPI C data input (GPIO236)
X2A57	DGND			Ground 0 V
X2A58	SPIC_SOUT	O		DSPI C data output (GPIO237)
X2A59	GPIO241	I/O		GPIO241
X2A60	GPIO243	I/O		GPIO243
X2A61	EQADC_ETRIG0/TXDC	I/O		eQADC trigger input (GPIO244)
X2A62	DGND	-		Ground 0 V
X2A63	ETPUA10	I/O		eTPU B channel 10 (GPIO124)
X2A64	ETPUA8	I/O		eTPU B channel 8 (GPIO122)
X2A65	ETPUA6	I/O		eTPU B channel 6 (GPIO120)
X2A66	ETPUA4	I/O		eTPU B channel 4 (GPIO118)
X2A67	DGND	-		Ground 0 V
X2A68	ETPUA2	I/O		eTPU B channel 2 (GPIO116)
X2A69	ETPUA0	I/O		eTPU B channel 0 (GPIO114)
X2A70	NEX_JCOMP	I		JTAG TAP controller enable
X2A71	NEX_TDO	O		JTAG test data output
X2A72	DGND	-		Ground 0 V
X2A73	NEX_TCK	I		JTAG test clock input
X2A74	NEX_/MSEO0	O		Nexus message start/end out

Table 5: Pinout of the phyCORE-Connector X2, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2A75	NEX_/MSEO1	O		Nexus message start/end out
X2A76	NEX_MDO0	O		Nexus message data out 0 (GPIO220)
X2A77	DGND	-		Ground 0 V
X2A78	NEX_MDO2	O		Nexus message data out 2 (GPIO222)
X2A79	NEX_MDO4	O		Nexus message data out 4 (GPIO75)
X2A80	NEX_MDO6	O		Nexus message data out 6 (GPIO77)
X2A81	NEX_MDO8	O		Nexus message data out 8 (GPIO79)
X2A82	DGND	-		Ground 0 V
X2A83	NEX_MDO10	O		Nexus message data out 10 (GPIO81)
X2A84	NEX_MDO12	O		Nexus message data out12 (GPIO231)
X2A85	NEX_MDO14	O		Nexus message data out14 (GPIO233)
X2A86	ETH_LINK (MPC_AC5)	O		ETH out signal LINK-LED **refer to J31**
X2A87	DGND	-		Ground 0 V
X2A88	FR_B_TX_EN	O		FlexRay B transfer enable (GPIO253)
X2A89	FR_B_TX	O		FlexRay B transfer (GPIO251)
X2A90	FR_B_RX	I		FlexRay B receive (GPIO252)

Table 5: Pinout of the phyCORE-Connector X2, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2B1	VCC_3V3	PWR_I		+3,3 V Primary Voltage Supply Input
X2B2	VCC_3V3	PWR_I		+3,3 V Primary Voltage Supply Input
X2B3	DGND	-		Ground 0 V
X2B4	NC	-		Not connected
X2B5	MPC_VSTBY	PWR_I		MPC- SRAM stby power range 1V – 5V
X2B6	/WDO	OC- PU		Watchdog timeout signal (U10)
X2B7	WDI	I		Watchdog trigger input signal (U10)
X2B8	DGND	-		Ground 0 V
X2B9	EMIOS0	I/O		eMIOS channel 0 (GPIO179)
X2B10	EMIOS2	I/O		eMIOS channel 2 (GPIO181)
X2B11	EMIOS4	I/O		eMIOS channel 4 (GPIO183)
X2B12	EMIOS5	I/O		eMIOS channel 5 (GPIO184)
X2B13	DGND	-		Ground 0 V
X2B14	EMIOS7	I/O		eMIOS channel 7 (GPIO186)
X2B15	SCIA_RX	I		Receive of eSCI channel A (GPIO90) **refer to J23**
X2B16	SCIA_TX	O		Transmit of eSCI channel A (GPIO91)
X2B17	CANA_RX	I		FlexCAN A receive line (GPIO84)

Table 6: Pinout of the phyCORE-Connector X2, Row B

Pin #	Signal	ST	Voltage Domain	Description
X2B18	DGND	-		Ground 0 V
X2B19	CANC_TX	O		FlexCAN C transmit line (GPIO87)
X2B20	CANC_RX	I		FlexCAN C receive line (GPIO88)
X2B21	RXDA_RS232	O		RxD eSCI A RS232 (U17) **refer to J23**
X2B22	TXDA_RS232	I		TxD eSCI A RS232 (U17)
X2B23	DGND	-		Ground 0 V
X2B24	EMIOS8	I/O		eMIOS channel 8 (GPIO187)
X2B25	EMIOS10	I/O		eMIOS channel 10 (GPIO189)
X2B26	EMIOS12	I/O		eMIOS channel 12 (GPIO191)
X2B27	EMIOS13	I/O		eMIOS channel 13 (GPIO192)
X2B28	DGND	-		Ground 0 V
X2B29	EMIOS15_IRQ1	I/O		eMIOS channel 15 (GPIO194)
X2B30	EMIOS17	I/O		eMIOS channel 17 (GPIO196)
X2B31	EMIOS19	I/O		eMIOS channel 19 (GPIO198)
X2B32	EMIOS21	I/O		eMIOS channel 21 (GPIO200)
X2B33	DGND	-		Ground 0 V
X2B34	ETH_TXN	ETH_O		negative transmit output of Ethernet controller LAN9221I (U2)
X2B35	ETH_TXP	ETH_O		Positive transmit output of Ethernet controller LAN9221I (U2)
X2B36	ETH_RXP	ETH_I		positive receive input of Ethernet controller LAN9221I (U2)
X2B37	ETH_RXN	ETH_I		negative receive input of Ethernet controller LAN9221I (U2)
X2B38	DGND	-		Ground 0 V
X2B39	GPIO203	I/O		GPIO203
X2B40	GPIO432	I/O		GPIO432
X2B41	GPIO434	I/O		GPIO434
X2B42	GPIO436	I/O		GPIO436
X2B43	DGND	-		Ground 0 V
X2B44	SPIA_SCK	O		DSPI A clock (GPIO93)
X2B45	SPIA_CS0	O		DSPI A chip select 0 (GPIO96)
X2B46	SPIA_CS2	O		DSPI A chip select 2 (GPIO98)
X2B47	SPIA_CS3	O		DSPI A chip select 3 (GPIO99)
X2B48	DGND	-		Ground 0 V
X2B49	SPIB_SCK	O		DSPI B clock (GPIO102)
X2B50	SPIB_CS0	O		DSPI B chip select 0 (GPIO105)
X2B51	SPIB_CS1	O		DSPI B chip select 1 (GPIO106)
X2B52	SPIB_CS3_SINC	O		DSPI B chip select 3 (GPIO108)

Table 6: Pinout of the phyCORE-Connector X2, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2B53	DGND	-		Ground 0 V
X2B54	SPIB_CS5_CS0C	O		DSPI A chip select 5 (GPIO110)
X2B55	SPIC_CS0	O		DSPI C chip select 0 (GPIO238)
X2B56	GPIO239	I/O		GPIO239
X2B57	GPIO240	I/O		GPIO240
X2B58	DGND	-		Ground 0 V
X2B59	GPIO242	I/O		GPIO242
X2B60	GPIO245	I/O		GPIO245
X2B61	ETPUA11	I/O		eTPU A channel 11 (GPIO125)
X2B62	ETPUA9	I/O		eTPU A channel 9 (GPIO123)
X2B63	DGND	-		Ground 0 V
X2B64	ETPUA7	I/O		eTPU A channel 7 (GPIO121)
X2B65	ETPUA5	I/O		eTPU A channel 5 (GPIO119)
X2B66	ETPUA3	I/O		eTPU A channel 3 (GPIO117)
X2B67	ETPUA1	I/O		eTPU A channel 1 (GPIO115)
X2B68	DGND	-		Ground 0 V
X2B69	NEX_/TEST	I		Test mode select **(do not use this pin !)**
X2B70	NEX_TDI	I		JTAG test data input
X2B71	NEX_TMS	I		JTAG test mode select input
X2B72	NEX_/RDY	O		Nexus ready output
X2B73	DGND	-		Ground 0 V
X2B74	NEX_MCKO	O		Nexus message clock out
X2B75	NEX_/EVTI	I		Nexus event in
X2B76	NEX_/EVTO	O		Nexus event out **(refer to JP6 basboard)**
X2B77	NEX_MDO1	O		Nexus message data out 1 (GPIO221)
X2B78	DGND	-		Ground 0 V
X2B79	NEX_MDO3	O		Nexus message data out 3 (GPIO223)
X2B80	NEX_MDO5	O		Nexus message data out 5 (GPIO76)
X2B81	NEX_MDO7	O		Nexus message data out 7 (GPIO78)
X2B82	NEX_MDO9	O		Nexus message data out 9 (GPIO80)
X2B83	DGND	-		Ground 0 V
X2B84	NEX_MDO11	O		Nexus message data out 11 (GPIO82)
X2B85	NEX_MDO13	O		Nexus message data out 13 (GPIO232)
X2B86	NEX_MDO15	O		Nexus message data out 15 (GPIO234)
X2B87	FR_A_TX_EN	O		FlexRay A transfer enable (GPIO250)
X2B88	DGND			Ground 0 V
X2B89	FR_A_TX	O		FlexRay A transfer (GPIO248)
X2B90	FR_A_RX	I		FlexRay A receive (GPIO249)

Table 6: Pinout of the phyCORE-Connector X2, Row B (continued)

Pin #	Signal	ST	Voltage domain	Description
X3A1	V1V0F	PWR_OUT		1,0V FPGA supply **(generated on Board U20) (use pin X3A1/A3/A4 onl for sensing the 1,0V)**
X3A2	DGND	-		Ground 0 V
X3A3	V1V0F	PWR_OUT		1,0V FPGA supply **(generated on Board U20)**
X3A4	V1V0F	PWR_OUT		1,0V FPGA supply **(generated on Board U20)**
X3A5	PG_V1V0F	OC- PU		V1V0F Power Good logic output signal U20
X3A6	F_B15_IO0	I/O		FPGA user I/O Pin 0 BANK 15
X3A7	DGND	-		Ground 0 V
X3A8	F_B15_IO1P	I/O		FPGA user I/O Pin 1P BANK 15
X3A9	F_B15_IO1N	I/O		FPGA user I/O Pin 1N BANK 15
X3A10	F_B15_IO3P	I/O		FPGA user I/O Pin 3P BANK 15
X3A11	F_B15_IO3N	I/O		FPGA user I/O Pin 3N BANK 15
X3A12	DGND	-		Ground 0 V
X3A13	F_B15_IO5P	I/O		FPGA user I/O Pin 5P BANK 15
X3A14	F_B15_IO5N	I/O		FPGA user I/O Pin 5N BANK 15
X3A15	F_B15_IO7P	I/O		FPGA user I/O Pin 7P BANK 15
X3A16	F_B15_IO7N	I/O		FPGA user I/O Pin 7N BANK 15
X3A17	DGND	-		Ground 0 V
X3A18	F_B15_IO9P	I/O		FPGA user I/O Pin 9P BANK 15
X3A19	F_B15_IO9N	I/O		FPGA user I/O Pin 9N BANK 15
X3A20	F_B15_IO11P	I/O		FPGA user I/O Pin 11P BANK 15
X3A21	F_B15_IO11N	I/O		FPGA user I/O Pin 11N BANK 15
X3A22	DGND	-		Ground 0 V
X3A23	F_B15_IO13P	I/O		FPGA user I/O Pin 13P BANK 15
X3A24	F_B15_IO13N	I/O		FPGA user I/O Pin 13N BANK 15
X3A25	F_B15_IO15P	I/O		FPGA user I/O Pin 15P BANK 15
X3A26	F_B15_IO15N	I/O		FPGA user I/O Pin 15N BANK 15
X3A27	DGND	-		Ground 0 V
X3A28	F_B15_IO17P	I/O		FPGA user I/O Pin 17P BANK 15
X3A29	F_B15_IO17N	I/O		FPGA user I/O Pin 17N BANK 15
X3A30	F_B15_IO19P	I/O		FPGA user I/O Pin 19P BANK 15
X3A31	F_B15_IO19N	I/O		FPGA user I/O Pin 19N BANK 15
X3A32	DGND	-		Ground 0 V
X3A33	F_B15_IO21P	I/O		FPGA user I/O Pin 21P BANK 15
X3A34	F_B15_IO21N	I/O		FPGA user I/O Pin 21N BANK 15
X3A35	F_B15_IO23P	I/O		FPGA user I/O Pin 23P BANK 15
X3A36	F_B15_IO23N	I/O		FPGA user I/O Pin 23N BANK 15
X3A37	DGND	-		Ground 0 V

Table 7: Pinout of the FPGA Connector X3, Row A

Pin #	Signal	ST	Voltage Domain	Description
X3A38	F_B15_IO25	I/O		FPGA user I/O Pin 0 BANK 15
X3A39	F_PROGRAM_B	I		FPGA reset to configuration logic **active LOW signal**
X3A40	F_INIT_B	OC		indicates initialization of configuration **memory active LOW signal**
X3A41	F_DONE	I/O		indicates successful completion of config.
X3A42	F_GNDADC	-		FPGA XADC analog ground reference.
X3A43	DXN_0	I		FPGA Temperature-sensing diode pins
X3A44	DXP_0	I		FPGA Temperature-sensing diode pins
X3A45	F_VP	I		XADC dedicated differential analog input
X3A46	F_VN	I		XADC dedicated differential analog input
X3A47	DGND	I		Ground 0 V
X3A48	F_B14_IO3P	I/O		FPGA user I/O Pin 3P BANK 14
X3A49	F_B14_IO3N	I/O		FPGA user I/O Pin 3N BANK 14
X3A50	F_B14_IO5P	I/O		FPGA user I/O Pin 5P BANK 14
X3A51	F_B14_IO5N	I/O		FPGA user I/O Pin 5N BANK 14
X3A52	DGND	-		Ground 0 V
X3A53	F_B14_IO7P	I/O		FPGA user I/O Pin 7P BANK 14
X3A54	F_B14_IO7N	I/O		FPGA user I/O Pin 7N BANK 14
X3A55	F_B14_IO9P	I/O		FPGA user I/O Pin 9P BANK 14
X3A56	F_B14_IO9N	I/O		FPGA user I/O Pin 9N BANK 14
X3A57	DGND	-		Ground 0 V
X3A58	F_B14_IO11P	I/O		FPGA user I/O Pin 11P BANK 14
X3A59	F_B14_IO11N	I/O		FPGA user I/O Pin 11N BANK 14
X3A60	F_B14_IO13P	I/O		FPGA user I/O Pin 13P BANK 14
X3A61	F_B14_IO13N	I/O		FPGA user I/O Pin 13N BANK 14
X3A62	DGND	-		Ground 0 V
X3A63	F_B14_IO15P	I/O		FPGA user I/O Pin 15P BANK 14
X3A64	F_B14_IO15N	I/O		FPGA user I/O Pin 15N BANK 14
X3A65	F_B14_IO17P	I/O		FPGA user I/O Pin 17P BANK 14
X3A66	F_B14_IO17N	I/O		FPGA user I/O Pin 17N BANK 14
X3A67	DGND	-		Ground 0 V
X3A68	F_B14_IO19P	I/O		FPGA user I/O Pin 19P BANK 14
X3A69	F_B14_IO19N	I/O		FPGA user I/O Pin 19N BANK 14
X3A70	F_B14_IO21P	I/O		FPGA user I/O Pin 21P BANK 14
X3A71	F_B14_IO21N	I/O		FPGA user I/O Pin 21N BANK 14
X3A72	DGND	-		Ground 0 V
X3A73	F_B14_IO23P	I/O		FPGA user I/O Pin 23P BANK 14
X3A74	F_B14_IO23N	I/O		FPGA user I/O Pin 23N BANK 14

Table 7: Pinout of the FPGA Connector X3, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X3A75	F_B14_IO25	I/O		FPGA user I/O Pin 25 BANK 14
X3A76	F_B34_IO7N	I/O		FPGA user I/O Pin 7N BANK 34
X3A77	DGND	-		Ground 0 V
X3A78	NC			Not connected
X3A79	F_B34_IO9P	I/O		FPGA user I/O Pin 9P BANK 34
X3A80	F_B34_IO9N	I/O		FPGA user I/O Pin 9N BANK 34

Table 7: Pinout of the FPGA Connector X3, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X3B1	VCC_3V3	PWR_I		+3,3 V Supply when FPGA U18 is populated
X3B2	VCC_3V3	PWR_I		+3,3 V Supply when FPGA U18 is populated
X3B3	VCC_3V3	PWR_I		+3,3 V Supply when FPGA U18 is populated
X3B4	DGND	-		Ground 0 V
X3B5	V1V8F	PWR_OUT		1,8V FPGA supply **(generated on Board U21) (use pin X3B5/B6 onl for sensing the 1,8V)**
X3B6	V1V8F	PWR_OUT		1,8V FPGA supply **(generated on Board U21)**
X3B7	PG_V1V8F	OC- PU		V1V8F Power Good logic output signal U21
X3B8	VCCO_15F	PWR_I		Optional BANK15 1,5 supply **refer to J34**
X3B9	DGND	-		Ground 0 V
X3B10	F_B15_IO2P	I/O		FPGA user I/O Pin 2P BANK 15
X3B11	F_B15_IO2N	I/O		FPGA user I/O Pin 2N BANK 15
X3B12	F_B15_IO4P	I/O		FPGA user I/O Pin 4P BANK 15
X3B13	F_B15_IO4N	I/O		FPGA user I/O Pin 4N BANK 15
X3B14	DGND	-		Ground 0 V
X3B15	F_B15_IO6P	I/O		FPGA user I/O Pin 6P BANK 15
X3B16	F_B15_IO6N	I/O		FPGA user I/O Pin 6N BANK 15
X3B17	F_B15_IO8P	I/O		FPGA user I/O Pin 8P BANK 15
X3B18	F_B15_IO8N	I/O		FPGA user I/O Pin 8N BANK 15
X3B19	DGND	-		Ground 0 V
X3B20	F_B15_IO10P	I/O		FPGA user I/O Pin 10P BANK 15
X3B21	F_B15_IO10N	I/O		FPGA user I/O Pin 10N BANK 15
X3B22	F_B15_IO12P	I/O		FPGA user I/O Pin 12P BANK 15
X3B23	F_B15_IO12N	I/O		FPGA user I/O Pin 12N BANK 15
X3B24	DGND	-		Ground 0 V
X3B25	F_B15_IO14P	I/O		FPGA user I/O Pin 14P BANK 15
X3B26	F_B15_IO14N	I/O		FPGA user I/O Pin 14N BANK 15
X3B27	F_B15_IO16P	I/O		FPGA user I/O Pin 16P BANK 15
X3B28	F_B15_IO16N	I/O		FPGA user I/O Pin 16NBANK 15

Table 8: Pinout of the FPGA Connector X3, Row B

Pin #	Signal	ST	Voltage Domain	Description
X3B29	DGND	-		Ground 0 V
X3B30	F_B15_IO18P	I/O		FPGA user I/O Pin 18P BANK 15
X3B31	F_B15_IO18N	I/O		FPGA user I/O Pin 18N BANK 15
X3B32	F_B15_IO20P	I/O		FPGA user I/O Pin 20P BANK 15
X3B33	F_B15_IO20N	I/O		FPGA user I/O Pin 20N BANK 15
X3B34	DGND	-		Ground 0 V
X3B35	F_B15_IO22P	I/O		FPGA user I/O Pin 22P BANK 15
X3B36	F_B15_IO22N	I/O		FPGA user I/O Pin 22N BANK 15
X3B37	F_B15_IO24P	I/O		FPGA user I/O Pin 24P BANK 15
X3B38	F_B15_IO24N	I/O		FPGA user I/O Pin 24N BANK 15
X3B39	DGND	-		Ground 0 V
X3B40	F_TDI	I		FPGA JTAG data input
X3B41	F_TDO	O		FPGA JTAG data output
X3B42	F_TMS	I		FPGA JTAG mode select
X3B43	F_TCK	I		FPGA JTAG clock
X3B44	DGND	-		Ground 0 V
X3B45	F_VREFN	I		1.25V reference input **refer to J8**
X3B46	F_VREFP	I		1.25V reference GND reference **refer to J9**
X3B47	F_VCCBATT	I		FPGA Decryptor key memory backup supply **refer to J36**
X3B48	F_B14_IO0	I/O		FPGA user I/O Pin 0 BANK 14
X3B49	DGND	-		Ground 0 V
X3B50	F_B14_IO4P	I/O		FPGA user I/O Pin 4P BANK 14
X3B51	F_B14_IO4N	I/O		FPGA user I/O Pin 4N BANK 14
X3B52	F_B14_IO6N	I/O		FPGA user I/O Pin 6N BANK 14
X3B53	NC			not connected
X3B54	DGND	-		Ground 0 V
X3B55	F_B14_IO8P	I/O		FPGA user I/O Pin 8P BANK 14
X3B56	F_B14_IO8N	I/O		FPGA user I/O Pin 8N BANK 14
X3B57	F_B14_IO10P	I/O		FPGA user I/O Pin 10P BANK 14
X3B58	F_B14_IO10N	I/O		FPGA user I/O Pin 10N BANK 14
X3B59	DGND	-		Ground 0 V
X3B60	F_B14_IO12P	I/O		FPGA user I/O Pin 12P BANK 14
X3B61	F_B14_IO12N	I/O		FPGA user I/O Pin 12N BANK 14
X3B62	F_B14_IO14P	I/O		FPGA user I/O Pin 14P BANK 14
X3B63	F_B14_IO14N	I/O		FPGA user I/O Pin 14N BANK 14

Table 8: Pinout of the FPGA Connector X3, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X3B64	DGND	-		Ground 0 V
X3B65	F_B14_IO16P	I/O		FPGA user I/O Pin 16P BANK 14
X3B66	F_B14_IO16N	I/O		FPGA user I/O Pin 16N BANK 14
X3B67	F_B14_IO18P	I/O		FPGA user I/O Pin 18P BANK 14
X3B68	F_B14_IO18N	I/O		FPGA user I/O Pin 18N BANK 14
X3B69	DGND	-		Ground 0 V
X3B70	F_B14_IO20P	I/O		FPGA user I/O Pin 20P BANK 14
X3B71	F_B14_IO20N	I/O		FPGA user I/O Pin 20N BANK 14
X3B72	F_B14_IO22P	I/O		FPGA user I/O Pin 22P BANK 14
X3B73	F_B14_IO22N	I/O		FPGA user I/O Pin 22N BANK 14
X3B74	DGND			Ground 0 V
X3B75	F_B14_IO24P	I/O		FPGA user I/O Pin 24P BANK 14
X3B76	F_B14_IO24N	I/O		FPGA user I/O Pin 24N BANK 14
X3B77	F_B34_IO8P	I/O		FPGA user I/O Pin 8P BANK 34
X3B78	F_B34_IO8N	I/O		FPGA user I/O Pin 8N BANK 34
X3B79	DGND			Ground 0 V
X3B80	F_B34_IO10P	I/O		FPGA user I/O Pin 10P BANK 34

Table 8: Pinout of the FPGA Connector X3, Row B (continued)

3 Jumpers

For configuration purposes, the phyCORE-MPC5676/57xx has several solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while
Figure 6 and
Figure 7 indicate the location of the solder jumpers on the board. *Figure 5* below provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-MPC5676/57xx to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCORE-MPC5676/57xx.

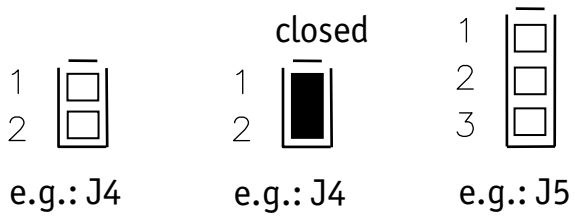

Figure 5: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

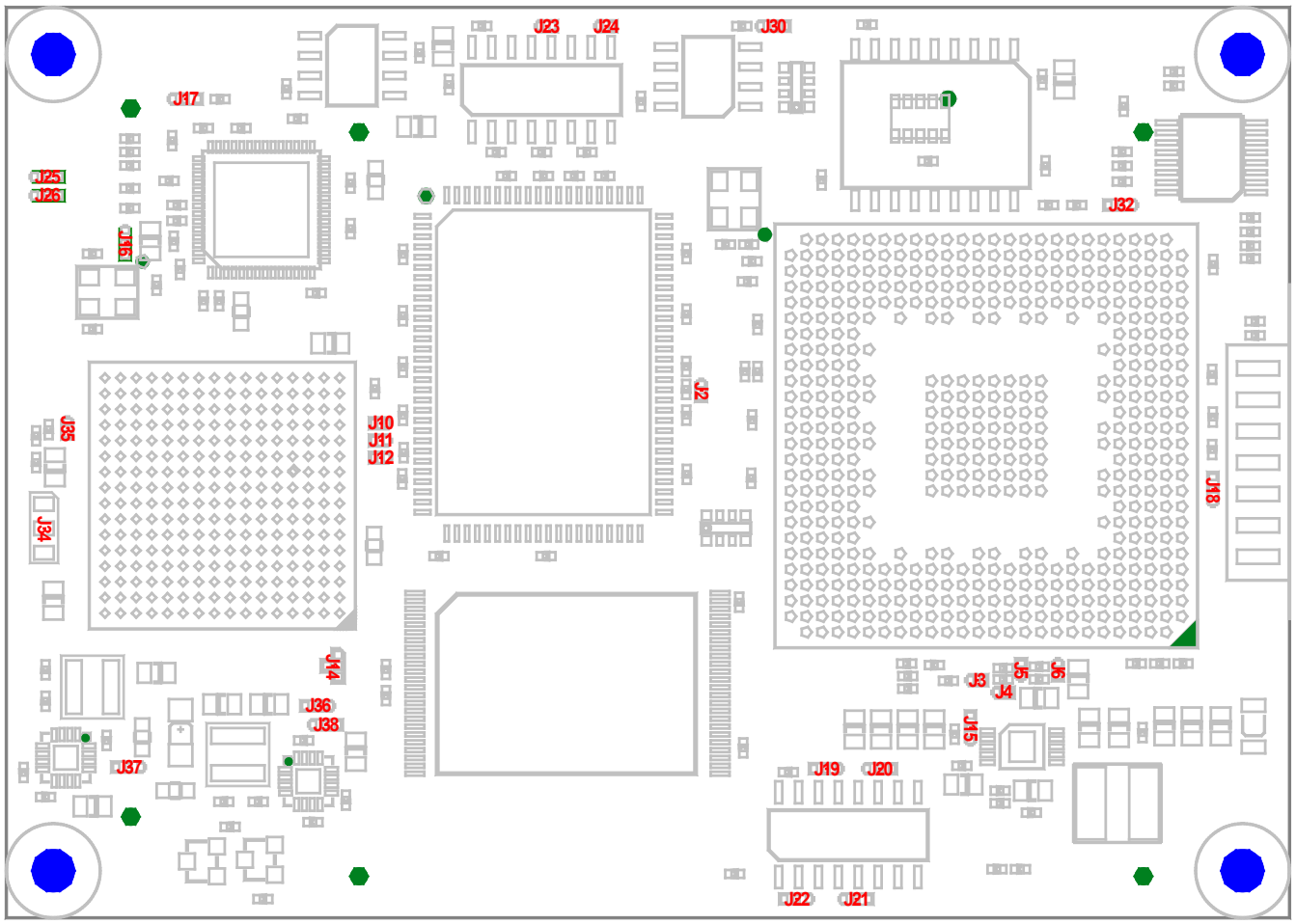

Figure 6: Jumper Locations (top view)

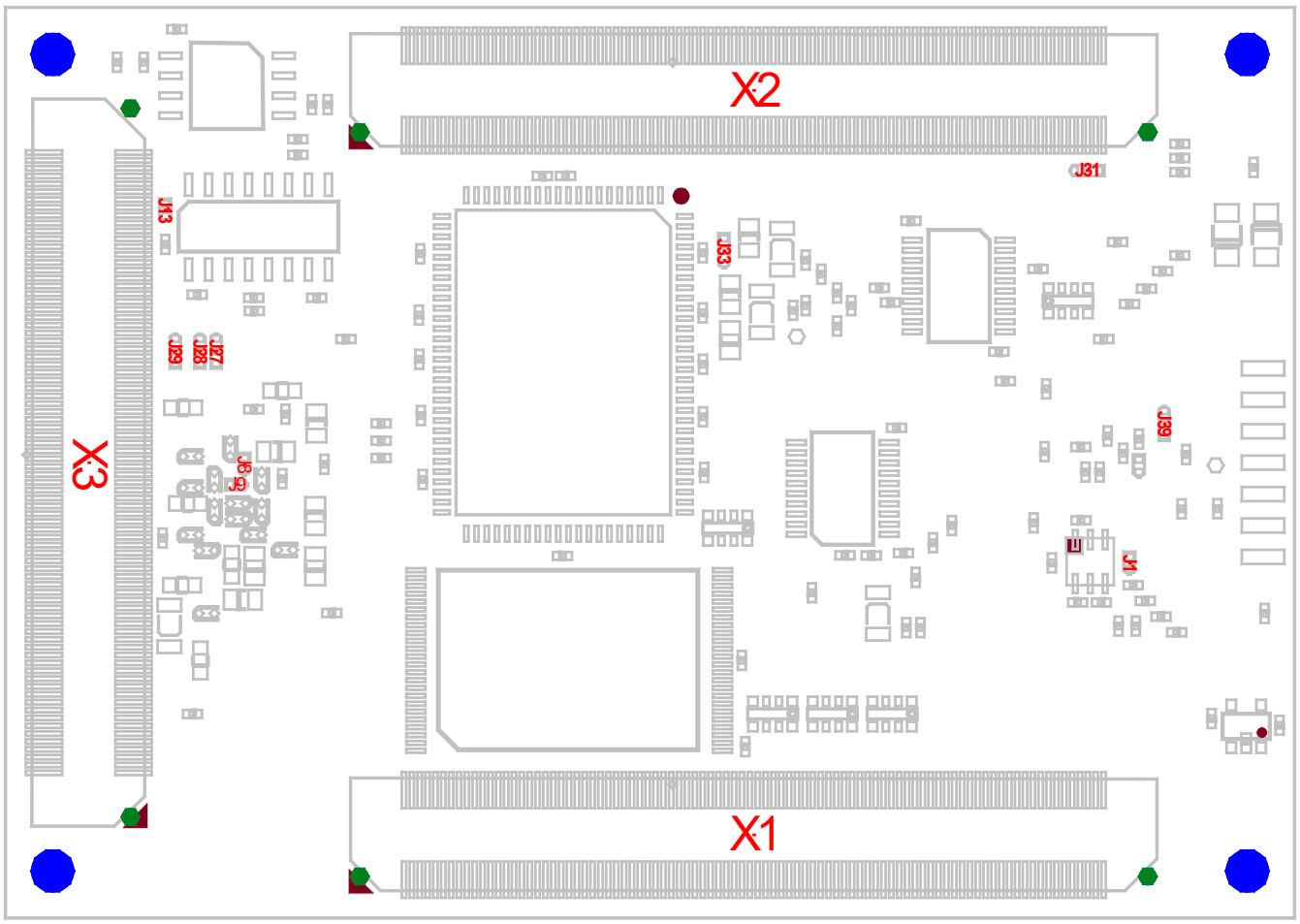

Figure 7: Jumper Locations (bottom view)

Please pay special attention to the “TYPE” column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc...). The jumpers are either 0805 package or 0402 package with a 1/8 W or better power rating.

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J1	Connects /CS0 directly /FL_CS	0 Ω (0402)	
closed	/CS0 directly connected to Flash (U5 must be unpopulated)		
open	/CS0 decoded with address A9 from MPC for generation of /FPGA_CS and /FL_CS		
J2	J2 connects the ZZ lines of SRAM memory devices U102-103 to the MPC GPIO460. ZZ is also connected to ball R2 of the FPGAU18B. This enables the phyCORE SRAM banks to be switched to an energy saving state via software. During this state, the memory cannot be read or written to. ZZ has a pull-down resistor.	0 Ω (0402)	
closed	Connects ZZ to the MPC GPIO460.		
open	Disconnects ZZ from the MPC GPIO460.		
J3	Connects ADC B Voltage reference high with ADC A Voltage reference high from MPC	0 Ω (0402)	
closed	EQADC_VRHA connected with EQADC_VRHB		
open	EQADC_VRHA not connected with EQADC_VRHB		
J4	Connects ADC B Voltage reference low with ADC A Voltage reference low from MPC	0 Ω (0402)	
closed	EQADC_VRLA connected with EQADC_VRLB		
open	EQADC_VRLA not connected with EQADC_VRLB		
J5	Connects VRL_A and VRL_B(J4) with AGND	0 Ω (0402)	
closed	EQADC_VRLA and EQADC_VRLB(J4) connected with AGND		
open	EQADC_VRLA and EQADC_VRLB(J4) of MPC must be connected extern from via phyCORE-Connector		

Table 9: Jumper Settings[1]

[1]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J6	Connects VDDA with EQADC_VRHA and EQADC_VRHB (J3)	0 Ω (0402)	
closed	EQADC_VRLA and EQADC_VRLB(J4) connected with VDDA		
open	EQADC_VRLA and EQADC_VRLB(J4) of MPC must be connected extern from phyCORE-Connector		
J7	Connects MPC_VSTBY to DGND (buffering of int. 48KB SRAM disabled)	0 Ω (0402)	
closed	MPC_VSTBY connected with DGND (buffering of int. 48KB SRAM disabled)		
open	MPC_VSTBY must be connected extern from phyCORE –Connector with 2V – 5V volts		
J8	Connects F_VREFN to F_GNDADC int. reference enabled	0 Ω (0402)	
closed			
open			
J9	Connects F_VREFP to F_GNDADC int. reference enabled	0 Ω (0402)	
closed	Connects F_VREFN to F_GNDADC int. reference enabled		
open			
J10	Connects GPIO452 of MPC to F_PROGRAMM_B of FPGA	0 Ω (0402)	
closed	GPIO452 connected to FPGAs F_PROGRAMM_B		
open	GPIO452 not connected to FPGAs F_PROGRAMM_B		

Table 9: Jumper Settings[2]

[2]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J11	Connects GPIO453 of MPC to F_INIT_B of FPGA	0 Ω (0402)	
closed	GPIO453 connected to FPGAs F_INIT_B		
open	GPIO453 not connected to FPGAs F_F_INIT_B		
J12	Connects GPIO454 of MPC to F_DONE of FPGA	0 Ω (0402)	
closed	GPIO454 connected to FPGAs F_DONE		
open	GPIO454 not connected to FPGAs F_DONE		
J13	Connects GPIO455 of MPC to multiplexer U14 select input	0 Ω (0402)	
closed	GPIO455 connected to to multiplexer U14 select input U14 select input		
open	GPIO455 not connected to to multiplexer U14 select input		
J14	J14 connects the memory bank address signal to the corresponding address lines of the processor. The configuration of these jumper is dependent on the memory size of the Synchronous Burst SRAM populating the module (U102 and U103). The factory setting of J14 is in accordance with the memory configuration of each individual module. The two memory banks are typically equipped with the same devices.	0 Ω (0402)	
1+2	A9: 32 MBit memory devices at U102/U103		
2+3	A11: 8 MBit memory devices at U102/U103		
2+4	A10: 16 MBit memory devices at U102/U103		

Table 9: Jumper Settings[3]

[3]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J15	Connects Enable Pin of U9 to DGND or VCC_3V3	0 Ω (0402)	
1+2	Voltage Regulator U9 is enabled		
2+3	Voltage Regulator U9 is disabled		
J16	Enables Auto-MDIX Ethernet U2 (int pull Up)	10k Ω (0402)	
1+2			
2+3			
J17	Connects GPIO461 or /RSTOUT of MPC to /Reset Input of Ethernet Controller LAN9221I	0 Ω (0402)	
1+2	/RSTOUT of MPC connected to /Reset Input		
2+3	GPIO461 of MPC connected to /Reset Input		
J18	Connects pull-UP or pull-DOWN to PLLCFG2 of MPC	4.7k Ω (0402)	
1+2	Pull-UP connected to PLLCFG2 of MPC (40Mhz crystal used)		
2+3	Pull-DOWN connected to PLLCFG2 of MPC		
J19	Connects pull-UP or pull-DOWN to PLLCFG1 of MPC	4.7k Ω (0402)	
1+2	Pull-UP connected to PLLCFG1 of MPC		
2+3	Pull-DOWN connected to PLLCFG1 of MPC		
J20	Connects pull-UP or pull-DOWN to PLLCFG0 of MPC	4.7k Ω (0402)	
1+2	Pull-UP connected to PLLCFG0 of MPC		
2+3	Pull-DOWN connected to PLLCFG0 of MPC		
J21	Connects pull-UP or pull-DOWN to BOOTCFG1 of MPC	4.7k Ω (0402)	
1+2	Pull-UP connected to BOOTCFG1 of MPC		
2+3	Pull-DOWN connected to BOOTCFG1 of MPC		
open	BOOTCFG1 must be pulled High or Low via phyCORE connector X1B5 for MPC Bootmode		

Table 9: Jumper Settings[4]

[4]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J22	Connects pull-UP or pull-DOWN to BOOTCFG0 of MPC	4.7k Ω (0402)	
1+2	Pull-UP connected to BOOTCFG0 of MPC		
2+3	Pull-DOWN connected to BOOTCFG0 of MPC		
open	BOOTCFG0 must be pulled High or Low via phyCORE connector X1B4 for MPC Bootmode		
J23,J24	J23 and J24 disconnect the receive lines of MPC UART from the RS-232 transceiver at U17. This makes the controller's SCI/UART TTL level signals available at pins X2B15 (RXDA) and X2A14 (RXDB). This is useful, for instance, for galvanic isolation of the RS-232 interface.	0 Ω (0402)	
open	The SCI/UART receive signals RXDA and RXDB are disconnected from the RS-232 transceiver.		
closed	The SCI/UART receive signals RXDA and RXDB are connected to the RS-232 transceiver.		
J25	Connects SPID_SOUT of MPC to F_SPI_DIN of FPGA	0 Ω (0402)	
1+2			
2+3	F_SPI_DOUT connected to F_SPI_DIN (for usage of FPGA Serial Slave Mode)		
J26	Connects pull-UP or pull-DOWN to PUDC_B of FPGA	4.7k Ω (0402)	
1+2	Pull-UP connected to PUDC_B (int. pull-UP disabled)		
2+3	Pull-DONW connected to PUDC_B (int. pull-UP enabled)		
J27,J28, J29	FPGA Configuration mode selection.	4.7k Ω (0402)	
1+2,2+3,2+3	FPGA Master SPI configuration Mode Configuration is loaded from SPI-Flash U19		

Table 9: Jumper Settings[5]

[5]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J30	Connects GPIO463 of MPC or pull-UP to write Protect input /WP of SPI EEPROM U6	0 Ω (0402)	
1+2	GPIO463 of MPC is connected to /WP of U6 U6 write protected until GPIO is set to high		
2+3	Pull-UP is connected to /WP of U6 U6 is NOT write protected		
J31	Connects ETH_LINK LED signal from Ethernet Controller U2 or Ball AC5 of MPC to phyCORE connector pin X2A86	0 Ω (0402)	
1+2	ETH_LINK is connected to phyCORE connector pin X2A86		
2+3	Ball AC5 of MPC is connected to phyCORE connector pin X2A86 (for future MPC devices)		
J32	Connects VCC_3V3 to Ball AC5 or makes Ball AC5 available at J31	0 Ω (0402)	
1+2	VCC_3V3 connected to MPC_AC5		
2+3	MPC_AC5 available at J31 (for future MPC devices)		
J33	Connects Ball AA23 with VCC_5V or VDDSYN (VCC_3V3)	0 Ω (0402)	
1+2	VDDSYN connected to MPC_AA23		
2+3	VCC_5V connected to MPC_AA23		
J34	3.3V or 1.5V IO Supply Voltage für BANK15 of FPGA	Ferrit 2A (0805)	
1+2	3.3V IO Supply Voltage for BANK15 of FPGA		
2+3	1.5V IO Supply Voltage for BANK15 of FPGA 1.5V must then be supplied via FPGA connector X3B8		

Table 9: Jumper Settings[6]

[6]: Default settings are in **bold blue** text

Jumper	Description	Type	Chapter
J35	Connects FPGAs F_EMCCLK14 to F_CCLK to enable SPI access to the SPI flash while the board is running in non-configuration mode EMCCLK14 pin is in tri-state mode during configuration	0 Ω (0402)	
open	EMCCLK14 not connected to F_CCLK		
close	EMCCLK14 connected to F_CCLK		
J36	Connects VCCBATT_0 of FPGA to 1.8V or FPGA connector X3B47 for external supply Description of VCCBATT_0: Decryptor key memory backup supply; this pin should be tied to the appropriate VCC or GND when not used.	0 Ω (0402)	
1+2	VCCBATT_0 is connected to 1.8V supply (Decryptor key memory not used)		
2+3	VCCBATT_0 can be connected via FPGA connector X3B47		
J37	Enable/Disable V1V0F Regulator U20	0 Ω (0402)	
1+2	V1V0F Regulator U20 enabled		
2+3	V1V0F Regulator U20 disabled		
J38	Enable/Disable V1V8F Regulator U21	0 Ω (0402)	
1+2	V1V8F Regulator U21 enabled		
2+3	V1V8F Regulator U21 disabled		
J39	Connects VCC_5V or VCC_3V3 VDDEH1 of MPC	0 Ω (0402)	
1+2	VCC_3V3 connected to VDDEH1 of MPC		
2+3	VCC_5V connected to VDDEH1 of MPC		

Table 9: Jumper Settings[7]

[7]: Default settings are in **bold blue** text

4 Power Requirements

The phyCORE-MPC5676/57xx must be supplied with two different supply voltages:

Supply voltage VCC_3V3 +3.3 V ± 5 % with tbdA **
Pins at Connector X2 A1, B1, B2
Pins at Connector X3 B1, B2,B3 (if FPGA is populated)

Supply voltage VDD5V +5 V ± 5 % with tbdA **
Pins at Connector X2 A4

** without external loads

Connect all +3.3 V VCC input pins to your power supply and at least the matching number of GND pins.
Corresponding GND: X2 A2, A7,B3,B8
Corresponding GND: X3 B4, B9,B14

Caution:
Both supply voltages are required for proper operation of the phyCORE-MPC5676/57xx. The module must never be put into operation whit only one of the supply voltages connected to the device! This might render the module inoperable.

Connect all power input pins to your power supply and at least the matching number of DGND pins neighboring the power pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

The load of the supplies depends on the external periphery attached to the phyCORE module.

Optional supply input VBAT **+3V**
Pin at Connector X2 A4

VBAT is the input pin that supplies the the Real-Time Clock U7 VBAT should be supplied from a 3 V source.

Optional supply input MPC_VSTBY **+2V to +5V**
Pin at Connector X2 B5

MPC_VSTBY is the power supply input that is used to maintain a portion of the contents of internal SRAM during power down.
If not used, tie VSTBY to VSS. (refer to J7 in Table 9)

Optional supply input F_VCCBATT **1.0V to 1.89V**
F_VCCBATT is Decryptor key memory backup supply;
this pin should be tied to the 1.8V or GND when not used (refer to J36 in *Table 9*)

On-board generated voltages: VDD1V5, VDDFPGA
VCC_1V2 5 MPC5676/57xx core voltage
V1V0F XILINX FPGA core voltage
V1V8F XILINX FPGA auxiliary/ VCCADC

4.1 Voltage Supervisor and Reset

The input voltages VCC_3V3 and VCC_5V as well as the on-board generated operation voltage VCC_1V2 are monitored by a voltage supervisor device at U10. This circuitry is responsible for generation of the system reset signal /RESET. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /RESET line will be inactive (high). /RESET connects to the processor reset input.

/RESET is a bi-directional (open-collector) signal that can be connected to more then one source. For instance, /RESET is also connected to the JTAG/OnCE connector of the phyCORE module. /RESET has a 10kOhm pull-up resistor.

5 System Configuration and Booting

Although most features of the MPC5676R microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The phyCORE- MPC5676/57xx supports the following start-up modes:

- Internal Flash Memory
- SCI UART
- FlexCAN

The phyCORE-MPC5676/57xx provides two boot configuration pins BOOT[1:0]. The setting of these pins configures the boot device which is selected by the microcontroller *Table 10* shows the possible settings of pins BOOTCFG0 and BOOTCFG1 and the resulting boot configuration of the MPC5676R.

BOOTCFG0 pinX1B4	BOOTCFG1 pinX1B5	Bootsource
0	0	Boot from internal flash memory
0	1	FlexCAN / eSCI boot

Table 10: Boot Modes of the phyCORE-MPC5676/57xx

6 System Memory

The system memory consist of internal MPC5676/57xx Flash memory, external standard Flash memory, Synchronous Burst SRAM, SPI-Flash (FPGA configuration) and a small non-volatile memory device:

- 6 MByte internal MPC5676R Flash
- 2 MByte to 8MByte asynchronous standard Flash
- 1 MByte to 8MByte synchronous SRAM
- SPI -EEPROM: 32 KByte
- SPI Flash (FPGA configuration Flash): 16 MB

The external Flash and sync. SRAM are connected to the MPC5676R 32-bit data bus.

The Flash is controlled by /CS0
The Synchronous Burst SRAM is controlled by /CS1

Communication with the small non-volatile memory device (EPROM) is established over the SPI bus. This memory device can be used for storage of system parameters or configuration data.

The following sections of this chapter detail each memory type used on the phyCORE-MPC5676/57xx.

6.1 External Standard Flash Memory (U100,U101)

The Flash memory devices used on the phyCORE- MPC5676/57xx operate in 16-bit mode and are organized in 32-bit data bus with. The device at U100 connects to the low data bus while device U101 connects to the high data bus.

Type	Size per device	Manufacturer	Device Code	Manufacturer Code
S29AL016J	2 MByte	Spansion	22C4	01

Table 11: Choice of Standard Flash Memory Devices and Manufacturers

The access speed depends on the MPC5676/57xx processor frequency and the speed grade of populated flash devices. The speed grade varies due to production deviations. To provide for a worst case scenario take the value for the highest access time into consideration. With assuming of tbd MHz processor frequency and tbd MHz bus speed take the following wait state values:

70 ns access time	tbd wait states

The external Flash controlled by /CS0 with 32-bit bus width (address/Data muxed mode).

When the FPGA is populated the 8MByte address space of /CS0 is shared between FPGA and external Flash as follows:

MPC /CS0 to FPGA	address space from 0x000000 to 3F.FFFF (size 4MByte)
MPC /CS0 to external Flash	address space from 0x400000 to 7F.FFFF (size 4MByte)

6.2 Synchronous Burst SRAM(U102,U103)

Use of synchronous Flow-Through Burst SRAM supports the fastest mode of the MPC5676R memory interface. The memory is organized in 32-bit width and consists of two banks. These banks appear to the processor as linear address spaces and do not require special activation. The memory is generally accessed via /CS1

The phyCORE-MPC5676R can be populated with memory devices of various capacities. Generally, each memory bank can only be populated with memory devices of a consistent size. Solder jumper J14 is used to configure the memory capacity and pre-installed at time of delivery.

Table 12 shows all of the possible memory configurations.

Capacity	Type	Device	J14
1 MByte	256k x 32/36-bit	U5	2+3
2 MByte	256k x 32/36-bit 512k x 32/36-bit	U5-6 U5	2+3 2+4
4 MByte	512k x 32/36-bit 1M x 32/36-bit	U5-6 U5	2+4 1+2
8 MByte	1M x 32/36-bit	U5-6	1+2

Table 12: Memory Options for the Synchronous Burst SRAM

The SRAM is controlled by /CS1 with 32-bit bus width (address/Data muxed mode)..

6.3 SPI EEPROM (U6)

The phyCORE-MPC5676/57xx is populated with a non-volatile 32 kB SPI[8] EEPROM at U6. This memory can be used to store configuration data or other general purpose data. This device is accessed through SPI "D" on the MPC5676R.
Write protection to the device is accomplished via jumper J30 and MPC GPIO463. Refer to *section 6.3.1* for further details.

6.3.1 EEPROM Write Protection Control (J30)

Jumper J30 connects the /WP pin of the EEPROM (U6) to a pull-up resistor or to GPIO463 of the MPC to control the write protection of the EEPROM from the MPC.

The following configurations are possible:

EEPROM Write Protection State	J30
Write access permanently allowed	2+3
Write protection controlled by GPIO463	**1+2**

Table 13: EEPROM write protection states via J30 and GPIO463[9]

6.4 SPI Flash Memory (U19))

The SPI Flash Memory of the phyCORE-MPC5676/57xx at U19 is the configuration memory for the XILINX FPGA.
The configuration file for the FPGA can be programmed in two way.

1.) programming the SPI Flash U19 indirect via JTAG interface of the XLINX FPGA
The JTAG Signals of the FPGA are available at the FPGA connector X3 pin B40 to B43

2.) programming the SPI Flash U19 directly from the MPC using SPID with SPID_CS2
In order to connect MPC SPI Signals to the SPI-Flash U19 via the multiplexer U14
GPIO455 must be programmed high.

[9]: See the manufacturer's data sheet for interfacing and operation.
[9]: Defaults are in **bold blue** text

7 FPGA System Logic Device U18

The phyCORE-MPC5676/57xx is populated with Xilinx Artix-7 “XC7A50T-XFTG256X” FPGA at U18 The FPGA is connected to the MPC External Data Adress Bus.

7.1 Addressing the FPGA from MPC

Due to the fact that chip selcts of the MPC are used in the default configuration of the phyCORE-MPC5676/57xx, the FPGA shares the address space of /CS0 with the populated external Flash U100/U101 via multiplexer U5.
The addresses space is are split as follows

MPC /CS0 to FPGA	address space from 0x000000 to 3F.FFFF (size 4MByte)
MPC /CS0 to external Flash	address space from 0x400000 to 7F.FFFF (size 4MByte)

7.2 Configuration of the FPGA

The FPGA configuration mode is master SPI (default). Refer to Jumper J27 to 29
For the FPGA configuration mode “master SPI mode” the phyCORE-MPC5676/57xx is equipped with a SPI Flash U19.
Refer to section 6.4

7.3 FPGA connector X3

The phyCORE-MPC5676/57xx provides 101 free usable I/Os from the FPGA on the FPGA-connector X3
(45 free I/Os BANK14 + free 50 I/Os BANK15 + free 6 I/Os BANK34 = 101 I/Os)
Furthermore the FPGA JTAG Signals and control Pins for the FPGA configuration are available at X3
Refer to Table 7 and Table 8 for the pinout of X3.

8 Serial Interfaces

8.1 Universal Asynchronous Interface

A dual-channel RS-232 transceiver is located on the phyCORE- MPC5676/57xx at U17. This device adjusts the signal levels of the TXDA/RXDA and TXDB/RXDB lines (MPC5676R eSCI UART). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXDA_RS232 or RXDB_RS232 line (X2B21/X2A24) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXDA_RS232 or TXDB_RS232 line (X2B22/X2A23) is connected to the RXD line of the COM port. The ground circuitry of the phyCORE- MPC5676/57xx must also be connected to the applicable ground pin on the COM port.

Furthermore it is possible to use the TTL signals of the eSCI UART channels externally. These signals are available at X2B15, X2B16 (RXDA, TXDA) and X2A14, X2A15 (RXDB, TXDB) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals or for connection of different interface standards (RS485 etc.). Using the solder jumpers J23 and J24, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines RXDA and RXDB. This is required so that the external transceiver does not drive signals against the on-board transceiver. The transmit lines TXDA / TXDB can be connected parallel to the transceiver input without causing any signal conflicts.

Pin #	Signal	ST	Volatge	Description
X2B22	TXDA_RS232	O	RS232	RS232 serial transmit signal
X2B21	RXDA_RS232	I	RS232	RS232 serial data receive signal
X2A23	TXDB_RS232	O	RS232	RS232 serial transmit signal
X2A24	RXDB_RS232	I	RS232	RS232 serial data receive signal
X2B16	SCIA_TX	O	TTL	serial transmit signal SCIA
X2B15	SCIA_RX	I	TTL	serial data receive signal SCIA
X2A15	SCIB_TX	O	TTl	serial transmit signal SCIB
X2A14	SCIB_RX	I	TTL	serial data receive signal SCIB

Table 14: Location of the UART Signals

8.2 CAN Interface

4x CAN Nodes (directly from MPC) are available at the phyCORE-connector X2 as shown in table 15

Pin #	Signal	ST	Voltage	Description
X2A16	CANA_TX	O	TTL	CAN A transmit
X2B17	CANA_RX	I	TTL	CAN A receive
X2A18	CANB_TX	O	TTL	CAN B transmit
X2A19	CANB_RX	I	TTL	CAN B receive
X2B19	CANC_TX	O	TTL	CAN C transmit
X2B20	CANC_RX	I	TTL	CAN C receive
X2A21	CAND_TX	O	TTL	CAN D transmit
X2A20	CAND_RX	I	TTL	CAN D receive

Table 15: Location of the UART Signals

8.3 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The MPC5676 provides up to five SPI interfaces that are available on the phyCORE-connector.

Note:
The phyCORE-MPC5676/57xx uses the SPI Interface SPID on board for the following devices:
SPI EEPROM U6 (SPID_/CS1)
SPI-RTC U7 (SPID_/CS0)
SPI-Flash (FPGA config. Flash) (SPID_/CS2)

9 LAN9221I Ethernet Controller

Connection of the phyCORE-MPC5676/57xx to the world wide web or a local network is possible if the optional LAN9221I 10/100 Mbit/s Ethernet controller populates the module at U2.
The LAN9221/LAN9221i includes an integrated Ethernet MAC and PHY

9.1.1 Ethernet Transformer

In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required termination resistors on the analog signals (ETH_TXN, ETH_TXP, ETH_RXN, ETH_RXP) are populated on the phyCORE-MPC5676/57xx, so there is no need to connect external termination resistors to these signals. Connection to an external Ethernet magnetics should be done using very short signal traces.
The ETH_TXN /TXP, ETH_RXN/RXP signals should be routed as 100 Ohm differential pairs. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

If you are using the applicable carrier board for the phyCORE-MPC5676/57xx (part number KSP-0180-B0), the external circuitry mentioned above is already integrated on the board (refer to *section 14.3.7*).

Caution!
Please see the datasheet of the Ethernet Controller when designing the Ethernet transformer circuitry.

9.1.2 Addressing the Ethernet Controller e

The Ethernet device LAN9221I is controlled by the MPC Chip Select signal /CS3. Prior to accessing the LAN device the Chip Select has to be initialized by the application software. The Ethernet device is accessed via 16Bit external Data Bus
(16bit address/data muxed mode)

9.1.3 Software Reset of the Ethernet Controller

The Ethernet Controller at U2 can be reset by software if Jumper J17=2+3 (default).
With J17=2+3 the reset input of the Ethernet is permanently connected to GPIO461
of the MPC5676R.

9.1.4 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC5676/57xx is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

Pin #	Signal	ST	Description
X2A16	ETH_TXP	ETH_O	Positive transmit output of Ethernet controller LAN9221I (U2)
X2B17	ETH_TXN	ETH_O	Negative transmit output of Ethernet controller LAN9221I (U2)
X2A18	ETH_RXP	ETH_I	Positive receive input of Ethernet controller LAN9221I (U2)
X2A19	ETH_RXN	ETH_I	Negative receive input of Ethernet Controller LAN9221I (U2)

Table 16: Location of the Ethernet Signals

10 Real-Time Clock M41T93 (U7)

On the phyCORE-MPC5676/57xx the Real-Time Clock M41T93 is populated at U7
Communication between MPC and RTC is done via SPID Interface and /CS0 from MPC

11 JTAG/OnCE/Nexus Debufg Interface

The MPC5676 offers an on-chip JTAG/OnCE/Nexus debug interface. This interface allows external debug access to the controller without requiring a service software or firmware, such as a Monitor program, running on the chip. This internal debug interface also contains hardware features supporting use with common cross development systems and debug environments, such as Metrowerks' CodeWarrior. For instance, the MPC5676 features internal breakpoint registers enabling debugging in Flash memory.

A reduced set of the on-chip JTAG/OnCE/Nexus interface extends from the MPC5676 to a 14-pin connector X8 (card edge) at which an external interface signal converter circuitry can be attached. Such signal converters enable connection of the MPC5676 to a host-PC for debugging purposes.
The footprint of X8 is designed for a 14-pin header with 2.0 mm pin spacing. The pin assignment is shown in *Table 17*. Pin header X8 is not installed on the standard phyCORE-MPC5676/57xx module.

phyCORE Pin X2	Signal		JTAG/OnCE Connector		Signal	phyCORE Pin X2
B70	NEX_TDI	1	o o	2	DGND	B68, B73, A72
A71	NEX_TDO	3	o o	4	DGND	B68, B73, A72
A73	NEX_TCK	5	o o	6	DGND	B68, B73, A72
-	NC	7	o o	8	NC	-
A8	/RESET	9	o o	10	NEX_TMS	B71
B1, B2...	VCC_3V3	11	o o	12	DGND	B68, B73, A72
B72	NEX_/RDY	13	o o	14	NEX_JCOMP	A70

Table 17: 14-Pin JTAG/OnCE Connector (X8) and Corresponding Pins on the phyCORE-Connector (X2)

In order to connect a true Nexus port, an external 38-pin connector must be located on the customer application board. The PHYTEC phyCORE-MPC5676/57xx Development Board (part number KSP-0180-B0) features such Nexus connector at X10 and can be used as an example.

12 Technical Specifications

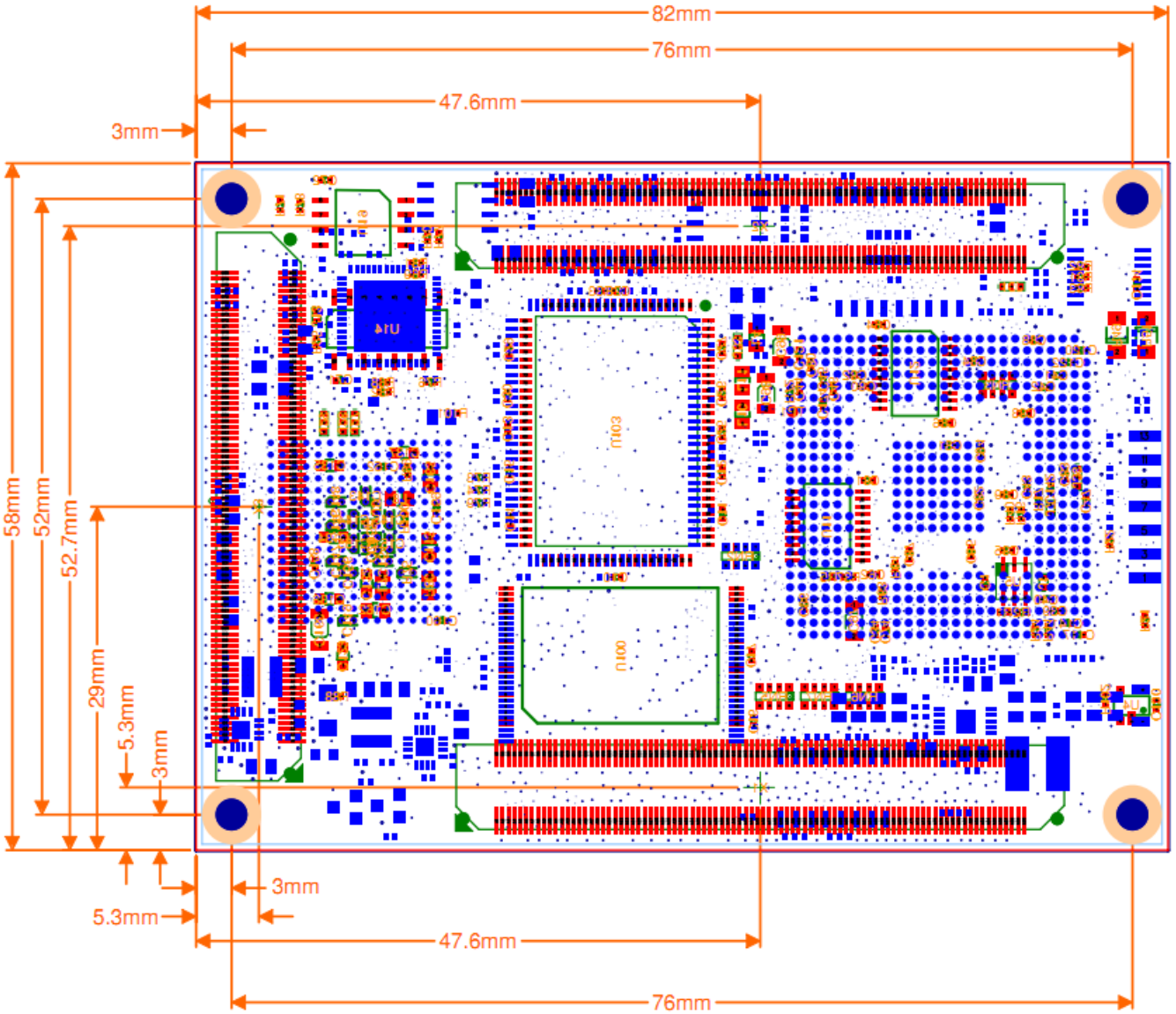

Figure 8: Physical Dimensions (top view)

The physical dimensions of the phyCORE-MPC5676/57xx are represented in *Figure 8*. The module's profile is max. 10 mm thick, with a maximum component height of 3.0 mm on the bottom (connector) side of the PCB and approximately 5.0 mm on the top (microcontroller) side. The board itself is approximately 1.5 mm thick.

Additional specifications:

Dimensions:	58 mm x 82 mm
Weight:	32g
Storage temperature:	-40°C to +125°C
Operating temperature:	0°C to +70°C (commercial) -40°C to +85°C (industrial) -40°C to +125°C (automotive)
Humidity:	95% r.F. not condensed
Operating voltage:	VCC 3.3 V +/- 5% VCC 5 V +/- 5%
Power consumption:	TBD

These specifications describe the standard configuration of the phyCORE-MPC5676/57xx as of the printing of this manual.

Connectors on the phyCORE-MPC5676/57xx:

Manufacturer	Samtec
	phyCORE-Connector X1 / X2:
Number of pins per contact rows	180 pins (2 rows of 90 pins each)
Samtec part number (lead free)	REF-177858-01
	FPGA -Connector X3:
Number of pins per contact rows	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	REF-178708-03

The following list shows the receptacle sockets that correspond to the connectors populating the underside of the phyCORE—MPC5676R. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the bottom side of the phyCORE must be subtracted.

Connector height 5 mm

Manufacturer	Samtec
Number of pins per contact row	180 pins (2 rows of 90 pins each)
Samtec part number (lead free)	REF-177863-03
PHYTEC part number (lead free)	VM248

Manufacturer	Samtec
Number of pins per contact row	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	REF-178709-03
PHYTEC part number (lead free)	VM245

Please refer to the corresponding data sheets and mechanical specifications provided by Samtec (*www.samtec.com*).

13 Hints for Integrating and Handling the phyCORE-MPC5676/57xx

13.1 Integrating the phyCORE-MPC5676/57xx

Besides this hardware manual much information is available to facilitate the integration of the phyCORE-MPC5676/57xx into customer applications.

1. the design of the standard phyCORE Carrier Board can be used as a reference for any customer application
2. many answers to common questions can be found at
   http://www.phytec.de/de/support/faq/faq-phyCORE-MPC56xx_57xx.html, or
   http://www.phytec.eu/europe/support/faq/faq-phyCORE-MPC56xx_57xx.html

13.2 Handling the phyCORE-MPC5676/57xx

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For maximum EMI performance we recommend as a general design rule to connect all GND pins to a solid ground plane. But at least all GND pins neighboring signals which are being used in the application circuitry should be connected to GND.

14 The phyCORE- MPC5676R on the phyCORE Carrier Board

PHYTEC phyCORE Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC System on Module (SOM) modules. phyCORE Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC System on Module in laboratory environments prior to their use in customer designed applications.

The phyCORE Carrier Board supports the following features for the phyCORE-MPC5676/57xx modules:

- Power supply circuits to supply the phyCORE-MPC5676/57xx and the peripheral devices of the carrier board
- 5V Power Supply Input (X9)
- all Signals of X1/X2/3 phyCORE-MPC5676/57xx are available on expansion connector
  X1A, X1B and X1B1, X1B2 for phyCORE-connector signals X1
  X2A, X2B and X2B1, X2B2 for phyCORE-connector signals X2
  X2, X3 for FPGA-Connector X3
- Switch (BOOTCFG1) to configure the boot mode of the MPC5676R
- 2 x DB9-Female (P2) for RS232 Interface (SCIA bottom/ SCI B top)
- 2 x DB9-male (P1) for High integrated CAN Interface (CANA bottom/ CANB top)
- 10/100Mbit Ethernet interface (L3)
- 4 x user LEDs (D1-D4) connected to MPC GPIOs
- 1 x user push button (S1) connected to IRQ of MPC
- 1x Resesitor (Poti) (RT1) connected to a Analog Input of MPC
- 1 x Reset push button (RESET1)
- 1x 38-pin MICTOR connector for Nexus Trace (X10)
- JTAG interface for programming and debugging MPC
- JTAG_FPGA interface for programming and debugging FPGA

14.1 Concept of the phyCORE Carrier Board

The phyCORE Development Board KSP-0180-B0 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC5676/57xx System on Module (SOM). The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

The following sections contain specific information relevant to the operation of the phyCORE-MPC5676/57xx mounted on the phyCORE Development Board PCM-979.

14.2 Overview of the phyCORE Carrier Board Peripherals

The phyCORE Carrier Board is depicted in *Figure 9*. It is equipped with the components and peripherals listed in *Table 18, Table 19, Table 20* and *Table 21.* For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. The following figures highlight the location of each peripheral for easy identification.

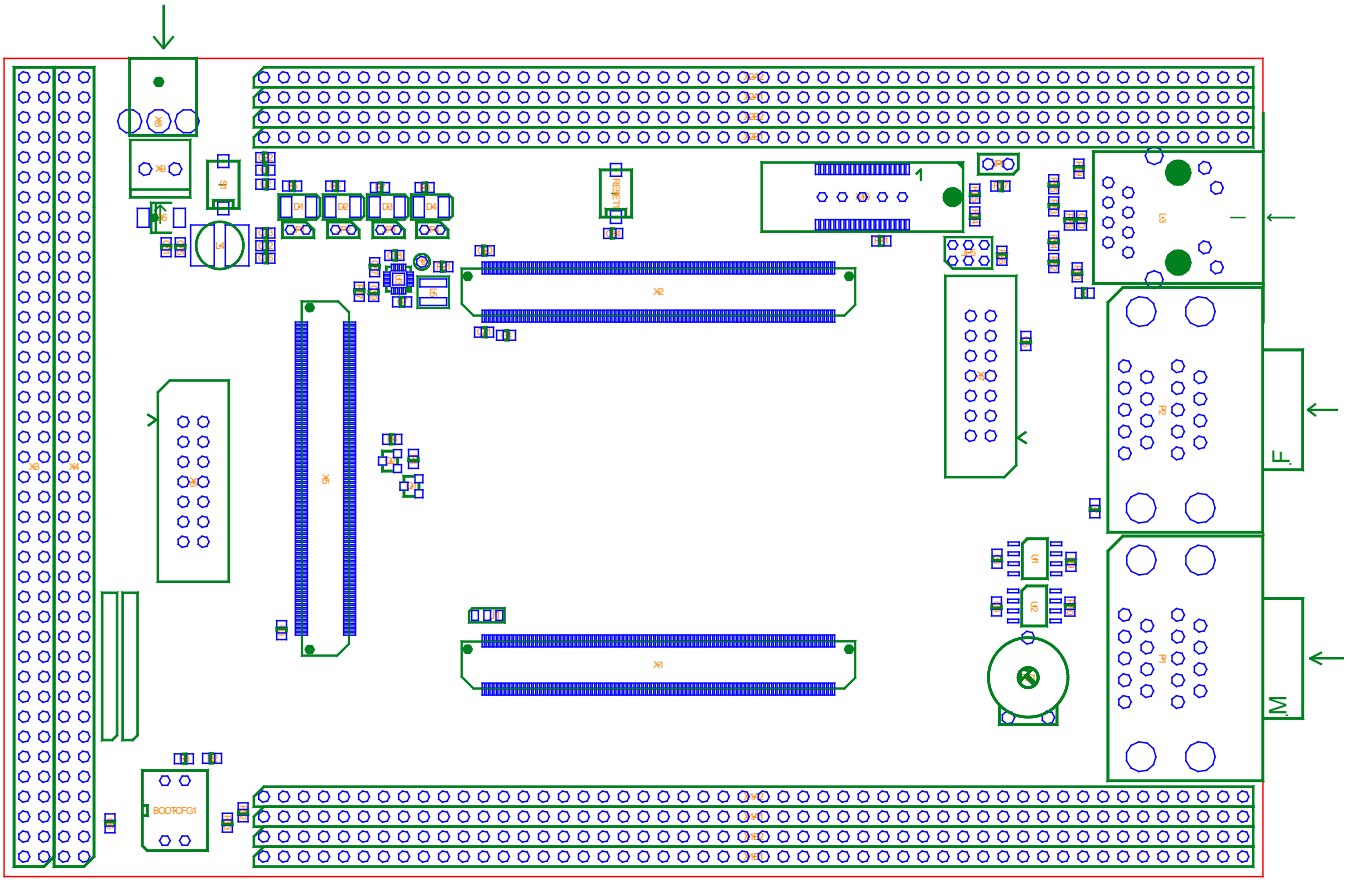

Figure 9: phyCORE Carrier Board Overview of Connectors, LEDs and Buttons (top view)

14.2.1 Connectors and Pin Header

Table 18 lists all available connectors on the phyCORE Carrier Board. *Figure 9* highlights the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	phyCORE-Connector for mounting the phyCORE-MPC5676/57xx	
X2	phyCORE-Connector for mounting the phyCORE-MPC5676/57xx	
X3	Expansion connector with signals from FPGA Connector	
X4	Expansion connector with signals from FPGA Connector	
X5	FPGA-Connector for mounting the phyCORE-MPC5676/57xx	
X6	FPGA JTAG Connector	
X7	MPC JTAG Connector	
X8	5V Wall-Adapter Input	
X9	Optional 5V Power input connector	
X10	38-pin MICTOR connector for Nexus Trace	
L3	RJ45 Input Jack 10/100 Mbit Ethernet Interface	
P2	RS232 interface, DB-9F	
P1	CAN interface, DB-9M	
X1A2, X1A1, X1B2, X1B1	Expansion connector with signals from phyCORE-Connector X1	
X2A2,X2A1, X2B2, X2B1	Expansion connector with signals from phyCORE-Connector X2	

Table 18: phyCORE Carrier Board Connectors and Pin Headers

Caution!
Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

14.2.2 Switches

The phyCORE Carrier Board is populated with some switches which are essential for the operation of the phyCORE-MPC5676/57xx module on the carrier board. *Figure* 9 shows the location of the switches and push buttons.

Button	Description	See Section
S1	user push button (S1) connected to IRQ of MPC	
RESET1	System Reset Button – system reset signal generation	
BOOTCFG1	DIP-switch – boot mode selection	

Table 19: phyCORE Carrier Board Push Buttons Descriptions

S1 Pressing this button will toggle the EMIOS14_IRQ0 pin (X2A28) of the phyCORE microcontroller LOW and a interrupt can be detected

RESET1 Issues a **system reset** signal. Pressing this button will toggle the /RESET pin (X2A8) of the phyCORE microcontroller LOW, causing the controller to reset.

S3 This DIP-switch allows to change the booting mode of the phyCORE-MPC5676/57xx.

14.2.3 LEDs

The phyCORE Carrier Board is populated with numerous LEDs to indicate the status of the various USB-Host interfaces, as well as the different supply voltages. *Figure 9* shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	See Section
D1	red	user LEDs connected to MPC GPIO179	
D2	red	user LEDs connected to MPC GPIO180	
D3	red	user LEDs connected to MPC GPIO181	
D4	red	user LEDs connected to MPC GPIO182	

Table 20: phyCORE Carrier Board LEDs Descriptins

14.2.4 Analog Input Potentiometer

The Analog Input Potentiometer RT1 enables variation of a Volatge (0V-5V),
that can be measured with MPC Analog Input EQADC_ANB1 pin X1A49 of the phyCORE-Connector

The Poti is connected with
EQADC_VRHB = 5V pin X1A50 of the phyCORE-Connector
EQADC_VRLB = 0V pin X1A51 of the phyCORE-Connector

14.2.5 Jumpers

The phyCORE Carrier Board comes pre-configured with removable jumpers (JP) and solder jumpers (J). The jumpers allow the user flexibility of configuring a limited number of features for development constraint purposes. *Table 21* below lists the jumpers, their default positions, and their functions in each position. *Figure 10* depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board. *Figure 11*provides a detailed view of the phyCORE Carrier Board jumpers and their default settings. In these diagrams a beveled edge indicates the location of pin 1.

Before making connections to peripheral connectors it is advisable to consult the applicable section in this manual for setting the associated jumpers.

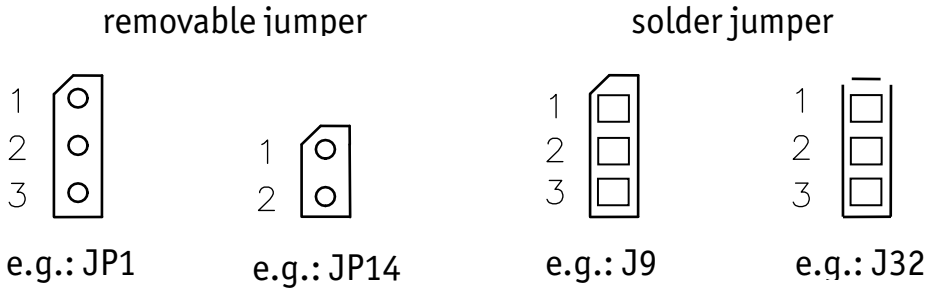

Figure 10: Typical Jumper Numbering Scheme

Table 21 provides a comprehensive list of all carrier board jumpers. The table only provides a concise summary of jumper descriptions. For a detailed description of each jumper see the applicable chapter listing in the right hand column of the table.

If manual modification of the solder jumpers is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

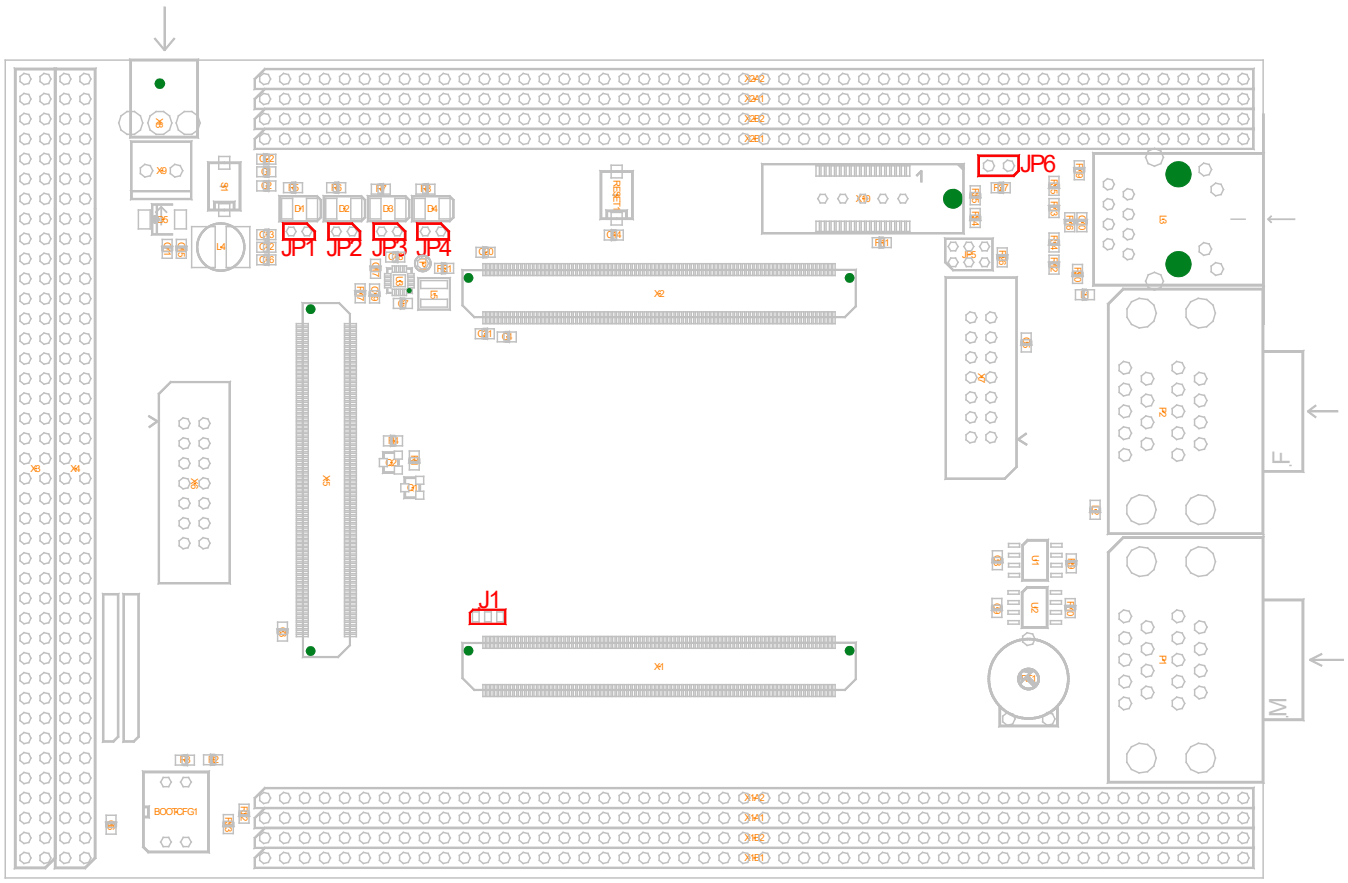

Figure 11: phyCORE Carrier Board Jumper Locations (top view)

The following conventions *are used in the Jumper column of jumper Table 21.*

- J = solder jumper
- JP = removable jumper

Jumper/ Setting	Description	See Section
JP1	Connects red user LED1 to MPC GPIO179	
1+2	**Connects red user LED1 to MPC GPIO179**	
open	LED1 not connected to MPC GPIO179	
JP2	Connects red user LED2 to MPC GPIO180	
1+2	**Connects red user LED2 to MPC GPIO180**	
open	LED2 not connected to MPC GPIO180	
JP3	Connects red user LED3 to MPC GPIO181	
1+2	**Connects red user LED3 to MPC GPIO181**	
open	LED3 not connected to MPC GPIO181	
JP4	Connects red user LED4 to MPC GPIO182	
1+2	**Connects red user LED4 to MPC GPIO182**	
open	LED4 not connected to MPC GPIO182	
JP6	Connects pull down to NEX_/EVTO	
1+2	**Pull down conneted to NEX_/EVTO** **Enables "Baud Rate Detection serial boot mode"**	
Open	NEX_/EVTO not connected to pull down	
J1	Connection of Clock for 38-PinMictor Connector X10_6	
1+2	ENGCLK from MPC is connected to X10_6	
2+3	CLKOUT from MPC is connected to X10_6	

Table 21: phyCORE Carrier Board Jumper Descriptions

Note:
Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

14.3 Functional Components on the phyCORE Carrier Board

This section describes the functional components of the phyCORE Carrier Board supporting the phyCORE-MPC5676/57xx. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

14.3.1 phyCORE- MPC5676R SOM Connectivity (X1, X2, X3)

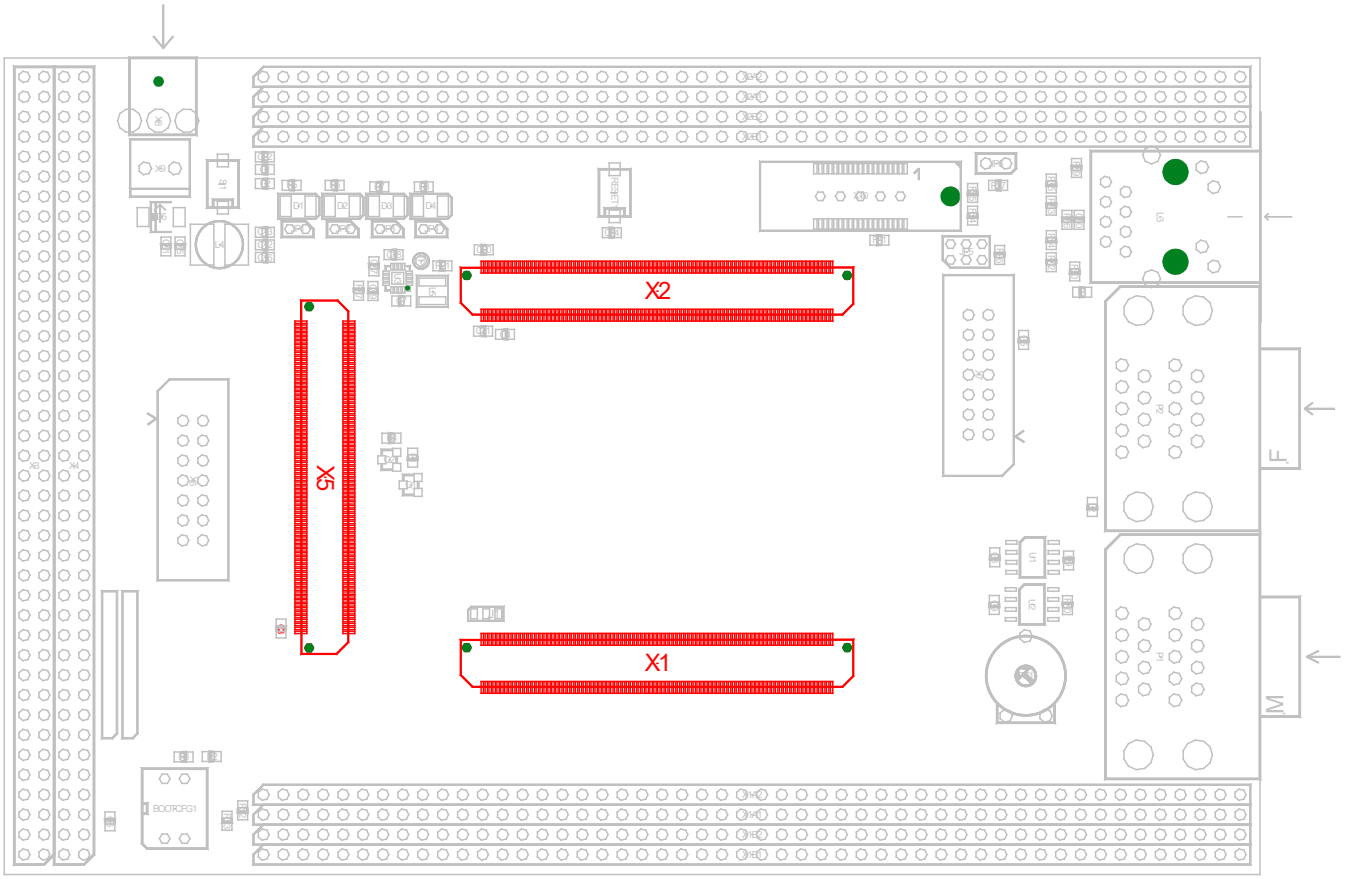

Figure 12: phyCORE- MPC5676R SOM Connectivity to the Carrier Board

Connectors X1 , X2 and X5 on the carrier board provide the phyCORE System on Module connectivity. The connector is keyed for proper insertion of the SOM.

Figure 12 above shows the location of connectors X1 , X2, X5 along with the pin numbering scheme as described in *section 2*.

Caution!
Samtec connectors guarantee optimal connection and proper insertion of the phyCORE-MPC5676R. Please make sure that the phyCORE-MPC5676/57xx is fully plugged into the matting connectors of the carrier board. Otherwise individual signals may have a bad, or no contact.

14.3.2 Power (X8, X9)

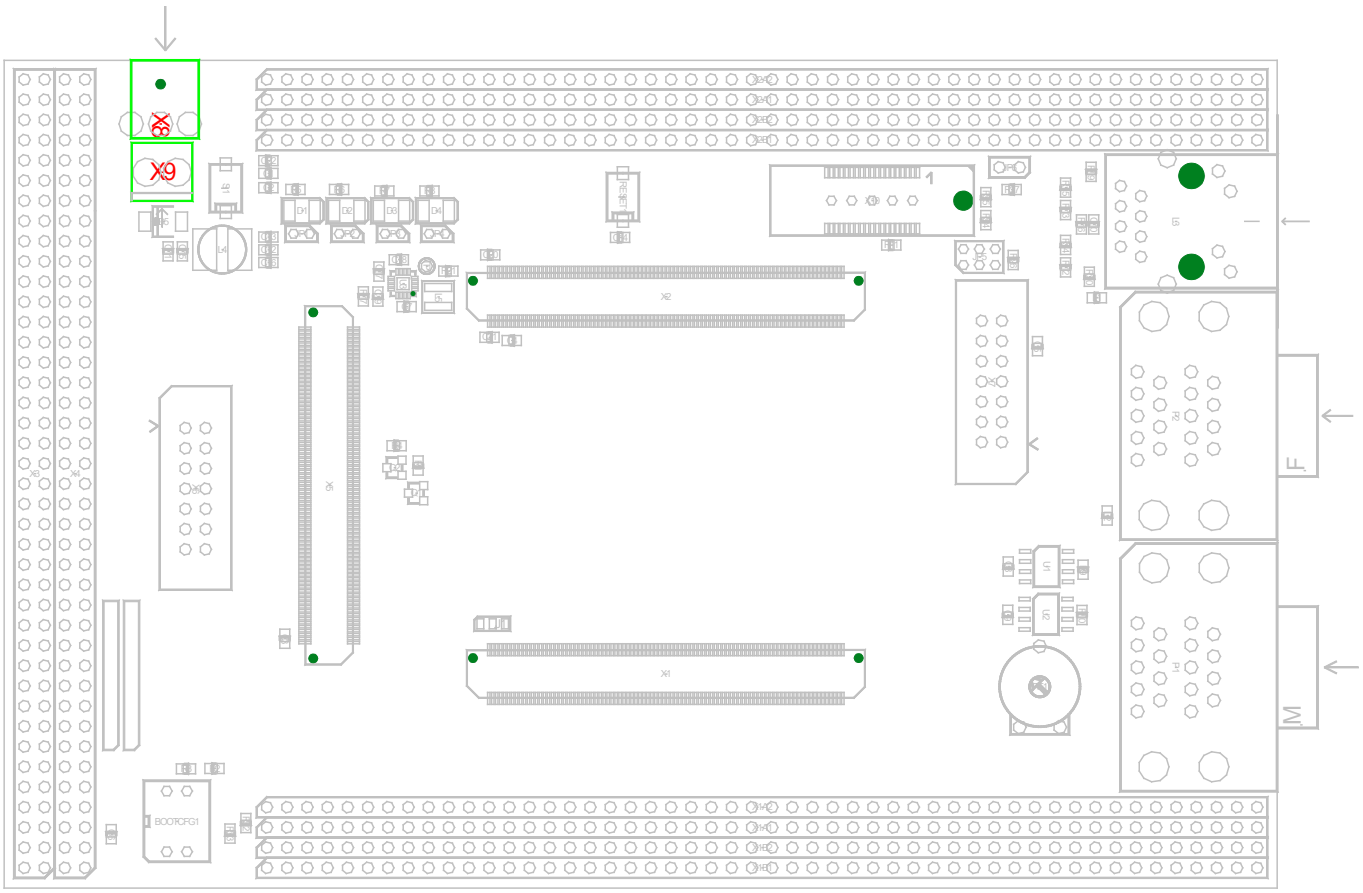

Figure 13: Powering Scheme

The primary input power of the phyCORE-MPC5676/57xx Carrier Board comes from either the wall adapter jack X8 (+5 V @3A), or connector X9 (+5V input current @3A).

The phyCORE MPC5676/57xx and and periphery components are supplied with 5V from X8 or X9 and 3.3V. The 3.3 are generated from an Switching regulator U3 on the carrier board.

14.3.2.1 Wall Adapter Input (X8)

Caution!
Do not use a laboratory adapter to supply power to the carrier board! Power spikes during power-on could destroy the phyCORE module mounted on the carrier board! Do not change modules or jumper settings while the carrier board is supplied with power!

Permissible input voltage at X8: 5 V DC regulated (3A).

The required current load capacity of the power supply depends on the specific configuration of the phyCORE mounted on the carrier board An adapter with a minimum supply of 3A is recommended.

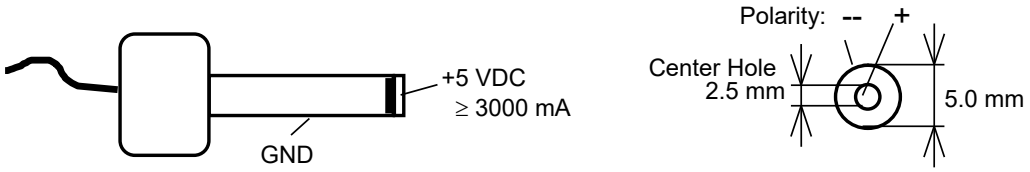

Figure 14: Power Connector corresponding to Wall Adapter Input X12

14.3.3 First Serial Interface at Socket P2A

Socket P2A is the bottom socket of the double DB-9 connector at P2. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the first serial interface.

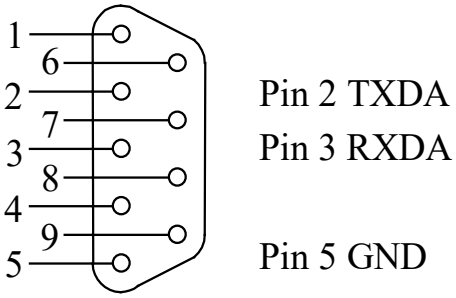

Figure 15: Pin Assignment of P2A as First RS-232 (Front View)

14.3.4 Second Serial Interface at Socket P2B

Socket P2B is the top socket of the double DB-9 connector at P2.

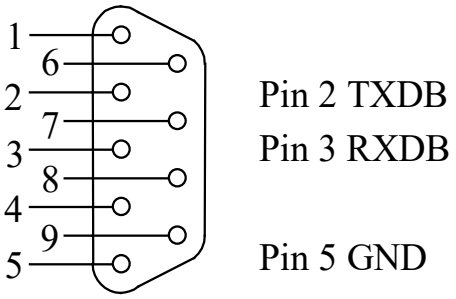

Figure 16: Pin Assignment of P2B as Second RS-232 (Front View)

14.3.5 First CAN Interface at Plug P1A

Plug P1A is the bottom plug of the double DB-9 connector at P1.
P1A is connected to the first FlexCAN interface (FlexCAN A)

The carrier Board is populated with the CAN transceiver for FlexCAN A

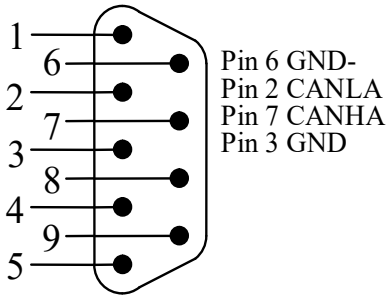

Figure 17: Pin Assignment of the DB-9 Plug P1A (CAN Transceiver on carrier Board, Front View)

14.3.6 Second CAN Interface at Plug P1B

Plug P1B is the upper plug of the double DB-9 connector at P1.
P1B is connected to the second FlexCAN interface (FlexCAN B)

The carrier Board is populated with the CAN transceiver for FlexCAN B

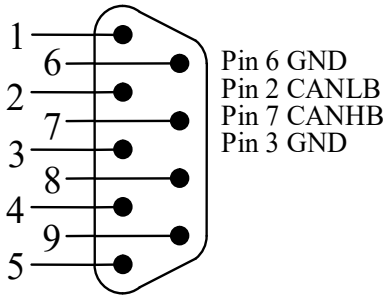

Figure 18: Pin Assignment of the DB-9 Plug P1B (CAN Transceiver on carrier Board, Front View).

14.3.7 Ethernet Connectivity (X28)

The Ethernet interface of the phyCORE is accessible at the RJ-45 connector (L3) on the carrier board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector.

14.3.8 User programmable LEDs

The phyCORE Carrier Board provides 4 red user programmable LEDs.

The following table lists all user programmable LEDs.

LED	Color	Description
D1	red	User LED connected to MPC GPIO179 (see JP1, *Table 21*)
D2	red	User LED connected to MPC GPIO180 (see JP1, *Table 21*)
D3	red	User LED connected to MPC GPIO181 (see JP1, *Table 21*)
D4	red	User LED connected to MPC GPIO182 (see JP1, *Table 21*)

Table 22: User Programmable LEDs on the Carrier Board

14.3.9 Boot Mode Selection (BOOTCFG1)

The boot mode DIP Switch BOOTCFG1 is provided to configure the boot mode of the phyCORE-MPC5676/57xx after reset. This DIP Switch allows choosing different boot sources. The following table gives an overview of the different boot sources. Refer to *section 5* for more information on the boot configuration.

Note:
The following table describes only settings suitable for the phyCORE-MPC5676/57xx. Other settings must not be used with the phyCORE-MPC5676/57xx.

DIP Switch	BOOTCFG0 pinX1B4	BOOTCFG1 pinX1B5	Bootsource
1=ON;2=ON	0	0	Boot from internal flash memory
1=ON;2=OFF	0	1	FlexCAN / eSCI boot

Table 23: phyCORE Carrier Board DIP Switch S3 Descriptions[10]

[10]: Default settings are in **bold blue** text

14.3.10 System Reset Button (RESET1)

The phyCORE Carrier Board is equipped with a system reset button RESET1.
Pressing this button will toggle the /RESET pin (X2A8) of the phyCORE microcontroller LOW, causing the controller to reset.

14.3.11 FPGA_JTAG Connector

The development board KSP-0180-Bx provides a JTAG 14-pin connector X6 for the XILINX FPGA on the phyCORE-MPC5676/57xx.

Signal	Pin Number	JTAG FPGA Connector		Signal
DGND	1	o o	2	VCC_3V3
DGND	3	o o	4	F_TMS
DGND	5	o o	6	F_TCK
DGND	7	o o	8	F_TDO
DGND	9	o o	10	F_TDI
DGND	11	o o	12	NC
DGND	13	o o	14	NC

Table 24: Pin Assignment of the JTAG_FPGA connector X6

14.3.12 JTAG/Once/Nexus Debug Interface

The development board KSP-0180-Bx provides two debug connectors.

X7 - reduced JTAG/OnCE/Nexus port to a 14-pin header connector (2.54 mm pin spacing)
X10 - full JTAG/OnCE/Nexus port to a 38-pol Mictor AMP 767054-1

14.3.13 Reduced JTAG/OnCE/NEXUS Pin Header Connector X

The 14-pin header connector at X7 on the Development Board enables connection of a simple external debug interface device (e.g. P&E Wiggler).

Signal	Pin Number	JTAG/OnCE Connector		Signal
NEX_TDI	1	o o	2	DGND
NEX_TDO	3	o o	4	DGND
NEX_TCK	5	o o	6	DGND
NC	7	o o	8	NC
/RESET	9	o o	10	NEX_TMS
VCC_3V3	11	o o	12	DGND
NEX_/RDY	13	o o	14	NEX_JCOMP

Table 25: Pin Assignment of the Reduced JTAG/OnCE/Nexus Pin Header X7

14.3.14 Full JTAG/OnCE/NEXUS Pin Header Connector X10

The pin header connector at X3 supports a standard 38-pin NEXUS debug connection (connector type AMP 767054-1) to various emulator probes (e.g. iSystem IC3000)

MPC Signal	Pin Number	Pin Number	MPC Signal
NEX_MDO12	1	2	NEX_MDO13
NEX_MDO14	3	4	NEX_MDO15
NEX_MDO9	5	6	ENGCLK refer to Jumper J1
Vendor	7	8	NEX_MDO8
/RESET	9	10	NEX_/EVTI
NEX_TDO	11	12	VCC_3V3
NEX_MDO10	13	14	NEX_/RDY
NEX_TCK	15	16	NEX_MDO7
NEX_TMS	17	18	NEX_MDO6
NEX_TDI	19	20	NEX_MDO5
NEX_JCOMP	21	22	NEX_MDO4
NEX_MDO11	23	24	NEX_MDO3
Vendor	25	26	NEX_MDO2
NC	27	28	NEX_MDO1
NC	29	30	NEX_MDO0
NC	31	32	NEX_/EVTO
NC	33	34	NEX_MCKO
NC	35	36	NEX_/MSEO 1
NC	37	38	NEX_/MSEO 0

Table 26: Pin Assignment of the Full JTAG/OnCE/Nexus Pin Header X10

14.3.15 phyCORE-MPC5676/57xx Expansion Connector

Most of the phyCORE-MPC5676/57xx Signals are available at the Expansion Connector of the The Development Board KSP-0180-B0.

The Expansion connectors on the Devolpment Board are (see *Figure 19*):

X1A2, X1A1, X1B2, X1B1 Expansion connector with signals from phyCORE-Connector X1
X2A2,X2A1, X2B2, X2B1 Expansion connector with signals from phyCORE-Connector X2
X3,X4 Expansion connector with signals from FPGA Connector

Please refer to section *14.3.16* for the Pin Assignment of the Expansion connectors

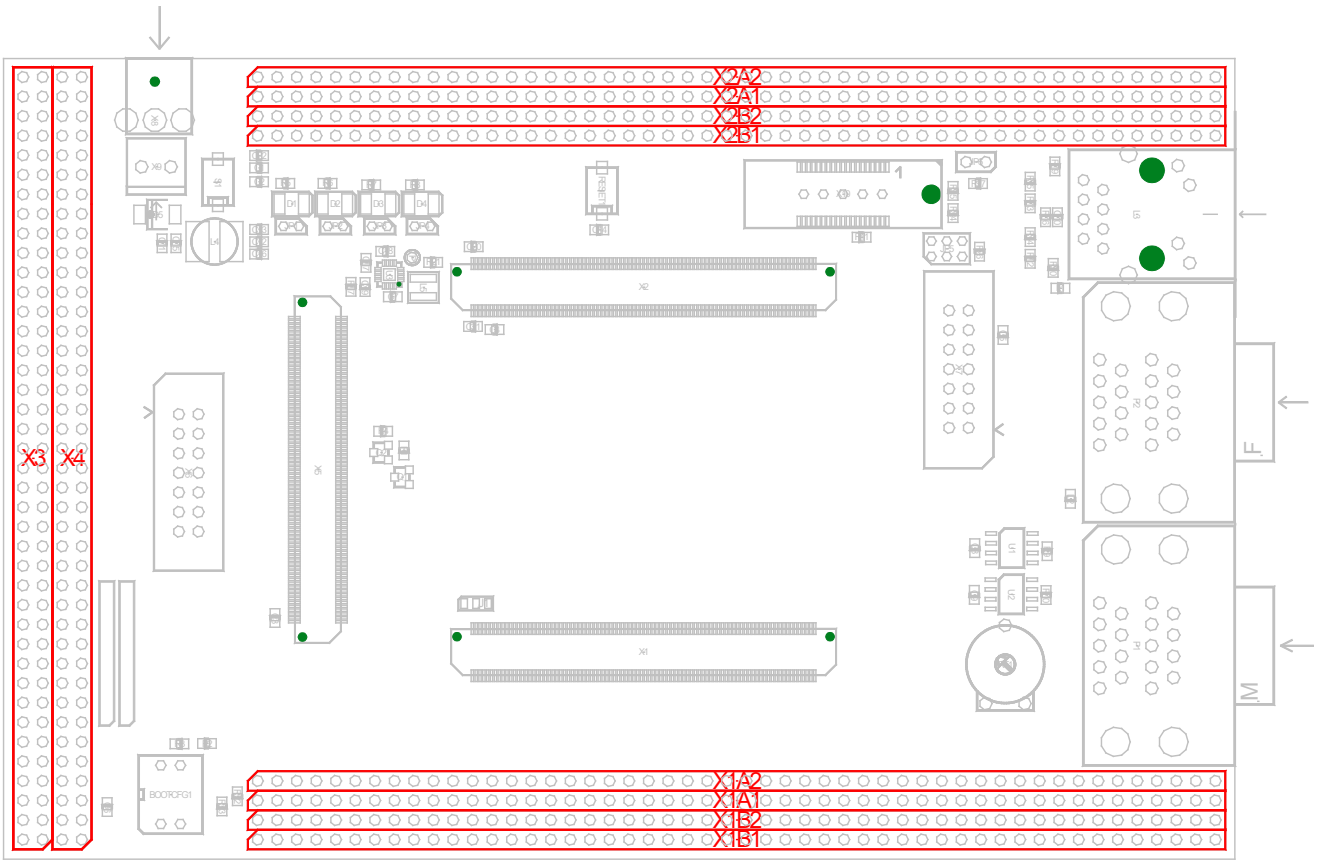

Figure 19: Expansion Connector location on the Development Board KSP-0150-B0

14.3.16 Schematic of Carrier Board KSP-0180-Bx

This section shows the schematic of the Development Board KSP-0150-B0.

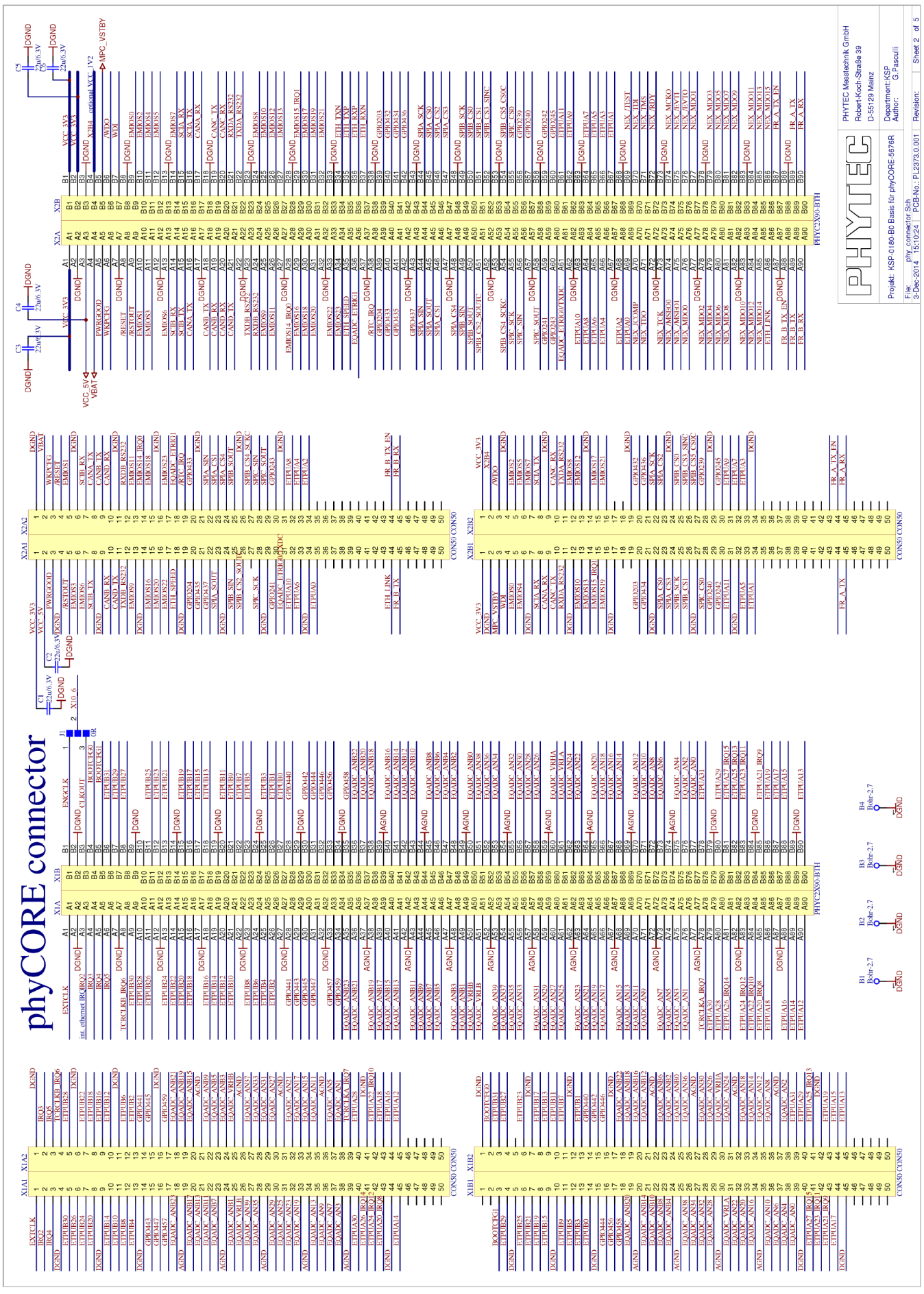

Figure 20: page 2/5 of KSP-0150-B0 schematic

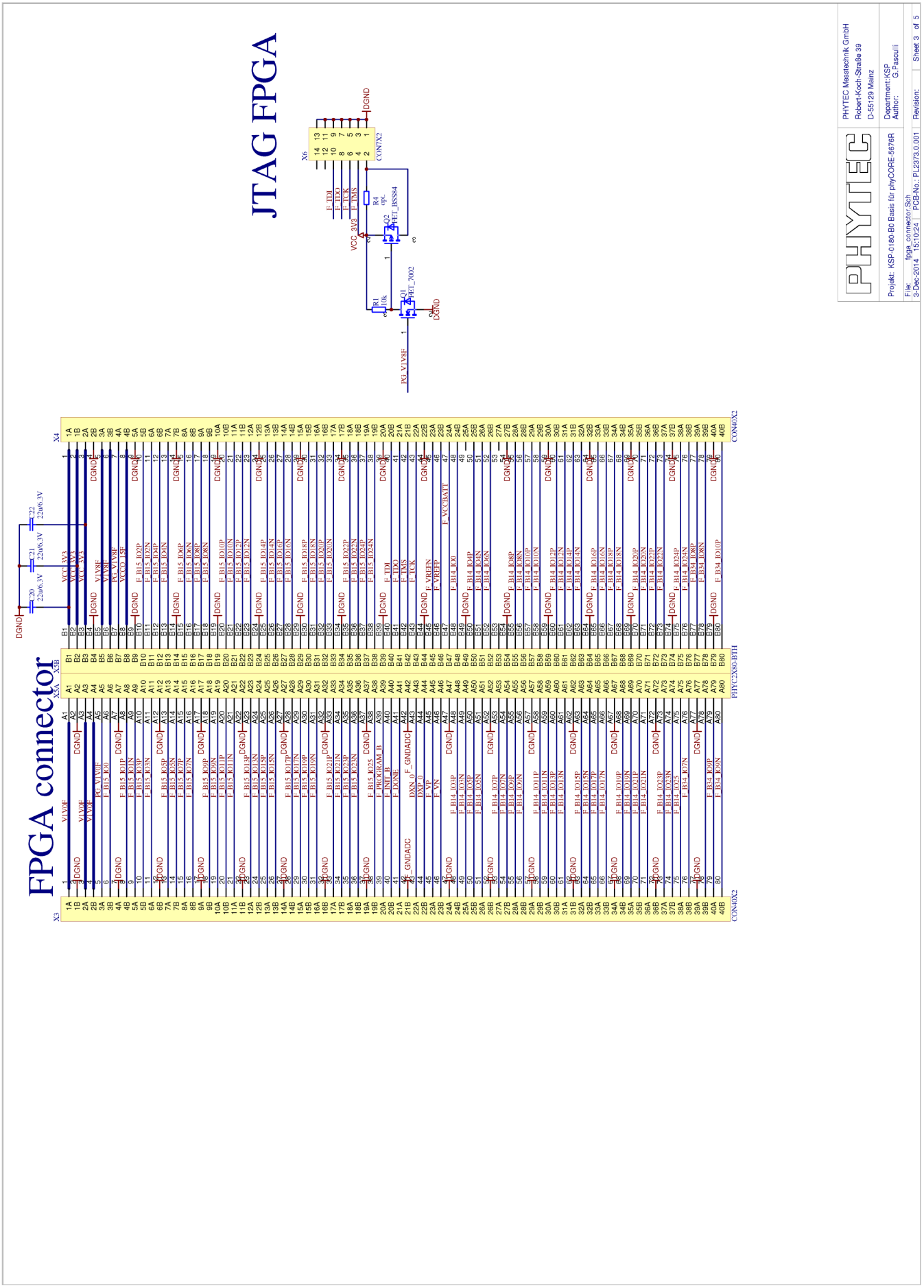

Figure 21: page 3/5 of KSP-0150-B0 schematic

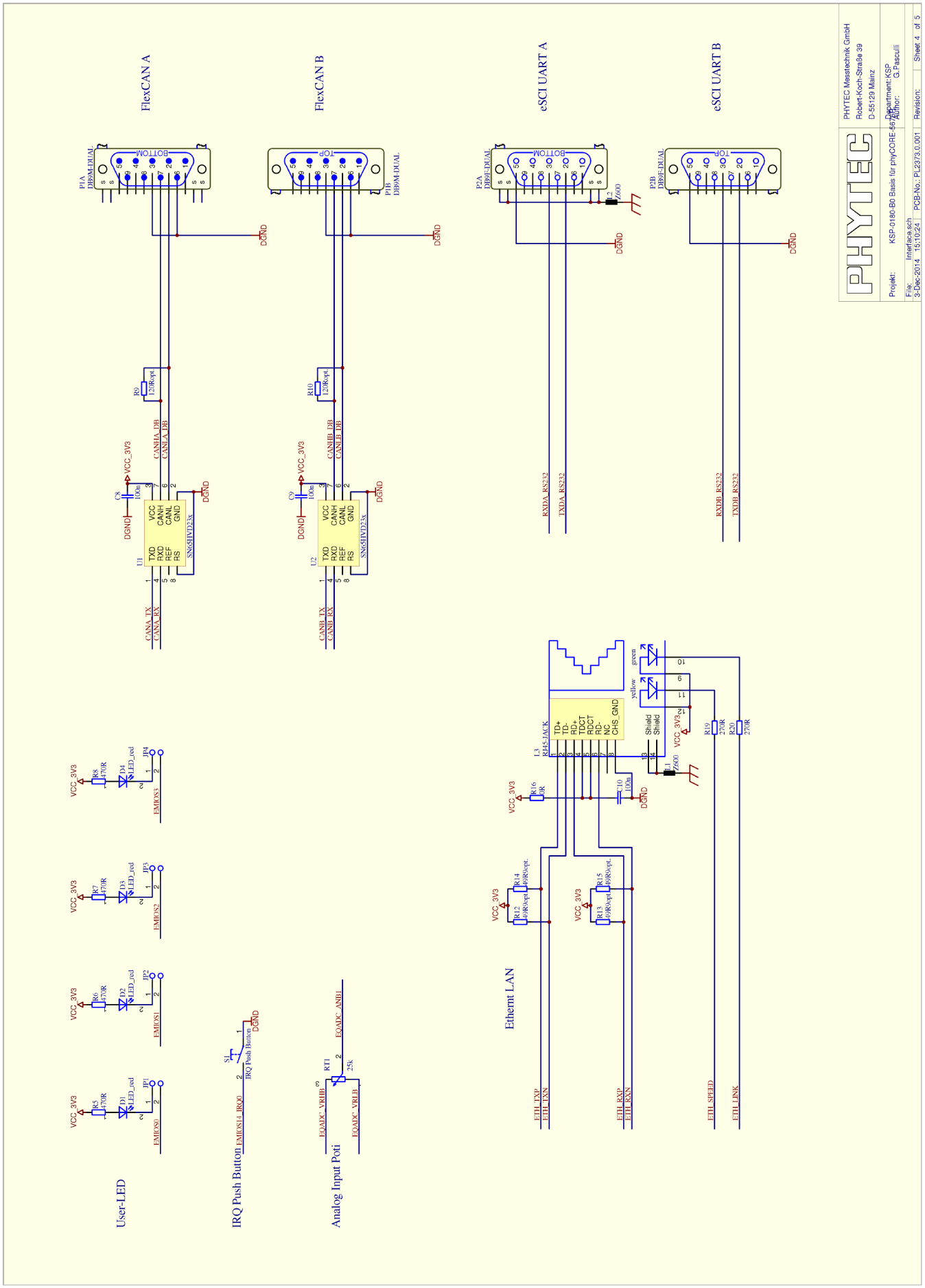

Figure 22: page 4/5 of KSP-0150-B0 schematic

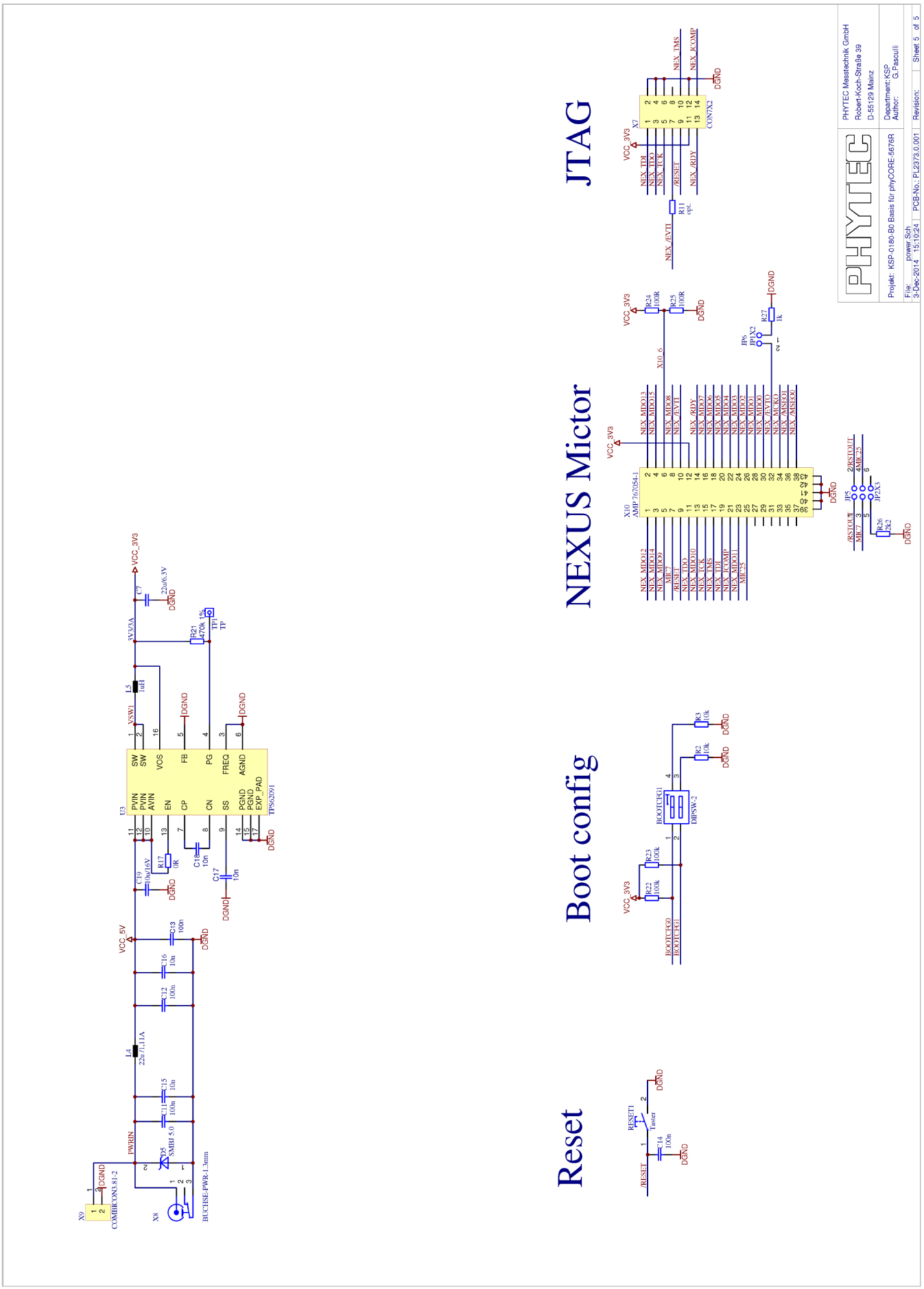

Figure 23: page 5/5 of KSP-0150-B0 schematic

15 Revision History

Date	Version numbers	Changes in this manual
09.03.2015	Manual L-807e_0	First draft, Preliminary documentation. Describes the phyCORE-MPC5676/57xx with phyCORE Carrier Board.
06.05.19	L-807e.A1	Pin Description Tables Updated

Index

V

W

X

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Return to:

PHYTEC Messtechnik GmbH
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

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