phyCORE-MPC5200B tiny

Hardware Manual

Edition December 2006

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2nd Edition December 2006

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Preface

This phyCORE-MPC5200B tiny Hardware Manual describes the board's design and functions. Precise specifications for the Freescale MPC5200B microcontroller series can be found in the enclosed MPC5200B microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC5200B tiny

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC5200B tiny is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and numerous 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user’s target design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC5200B tiny belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC5200B tiny is a subminiature (53 x 57 mm) insert-ready Single Board Computer populated with Freescale’s PowerPC MPC5200B microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MPC5200B controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC5200B tiny.

The phyCORE-MPC5200B tiny offers the following features:

- Single Board Computer in subminiature form factor (53 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 100-pin Molex connectors
- processor: Freescale embedded PowerPC MPC5200B
- single 3.3 V (max. 1.2 A) supply voltage

Internal Features of the MPC5200B:

- e300 core
  - 760 MIPS at 400 MHz (-40 to +85 °C)
  - 32 k instruction cache, 32 k data cache
  - Double precision FPU
  - Instruction and data MMU
- SDRAM / DDR SDRAM memory Interface
  - up to 132 MHz operation
  - SDRAM and DDR SDRAM support
  - 256 MByte addressing range per CS, two CS available
- Flexible multi-function external bus interface
- Peripheral component interconnect (PCI) controller
- ATA controller
- BestComm DMA subsystem

- 6 programmable serial controllers (PSC), configurable for the following functions:
- Fast Ethernet controller (FEC)
  - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII
- Universal serial bus controller (USB)
  - USB revision 1.1 host
- Two inter-integrated circuit interfaces (I2C)
- Serial peripheral interface (SPI)
- Dual CAN 2.0 A/B controller (MSCAN)
- J1850 byte data link controller (BDLC)
- Test/debug features
- JTAG (IEEE 1149.1 test access port)
- Common on-chip processor (COP) debug port

Memory Configuration[1]:

- DDR SDRAM: 64 MByte to 128 MByte
- Flash: 16 MByte Intel Strata Flash memory, 16-bit memory width, only asynchronous (J3) devices are supported
- I^2C memory: 4 kByte EEPROM

Other Board-Level Features:

- Two UART ports, RS-232 interfaces (RxD/TxD)
- One 10/100Mbit Ethernet port via optional Micrel PHY
- I^2C Real-Time Clock with calendar and alarm function
- Optional industrial temperature range (-40…+85°C)

1: Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

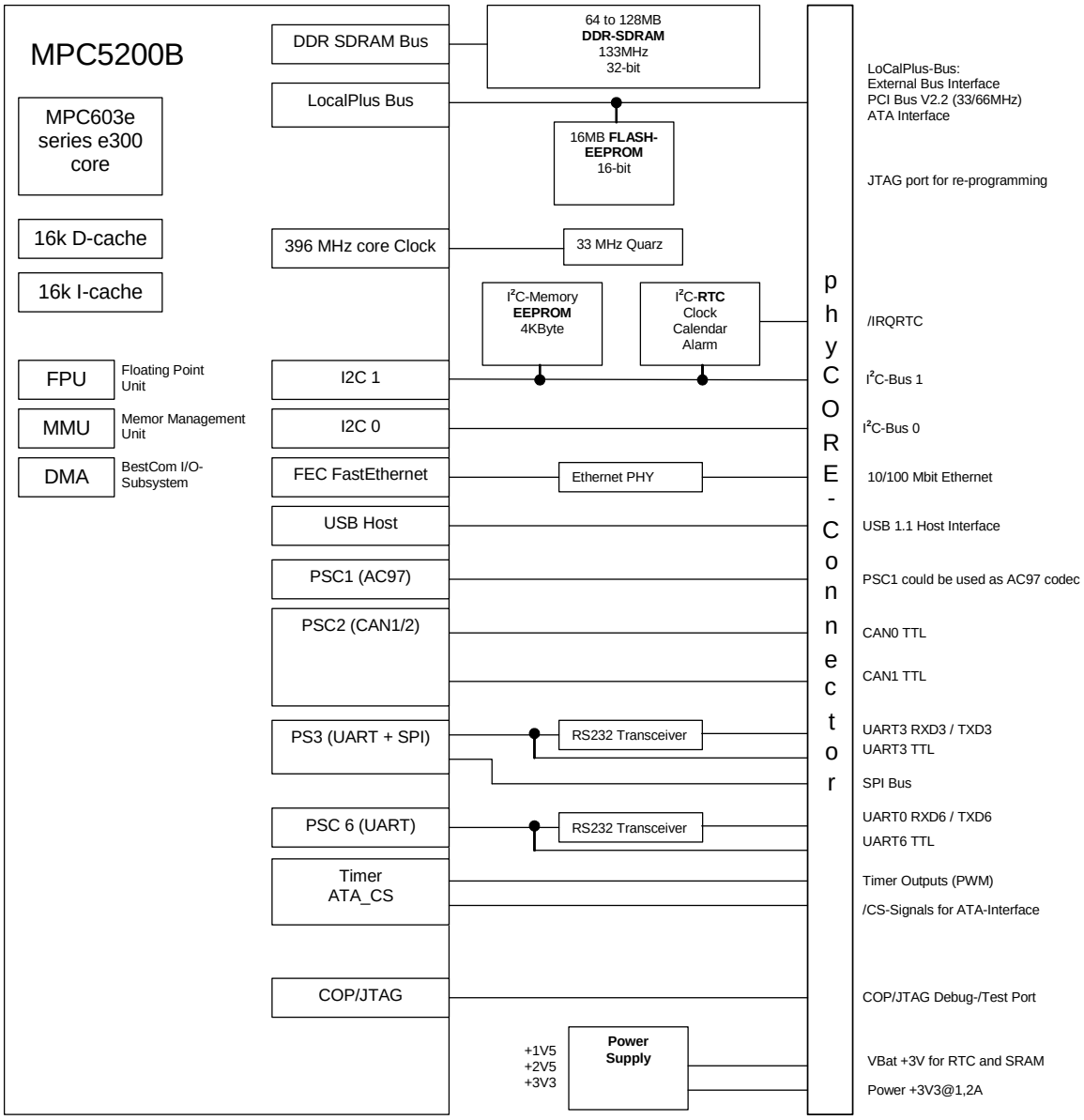


Figure 1: Block Diagram phyCORE-MPC5200B tiny

1.2 View of the phyCORE-MPC5200B tiny

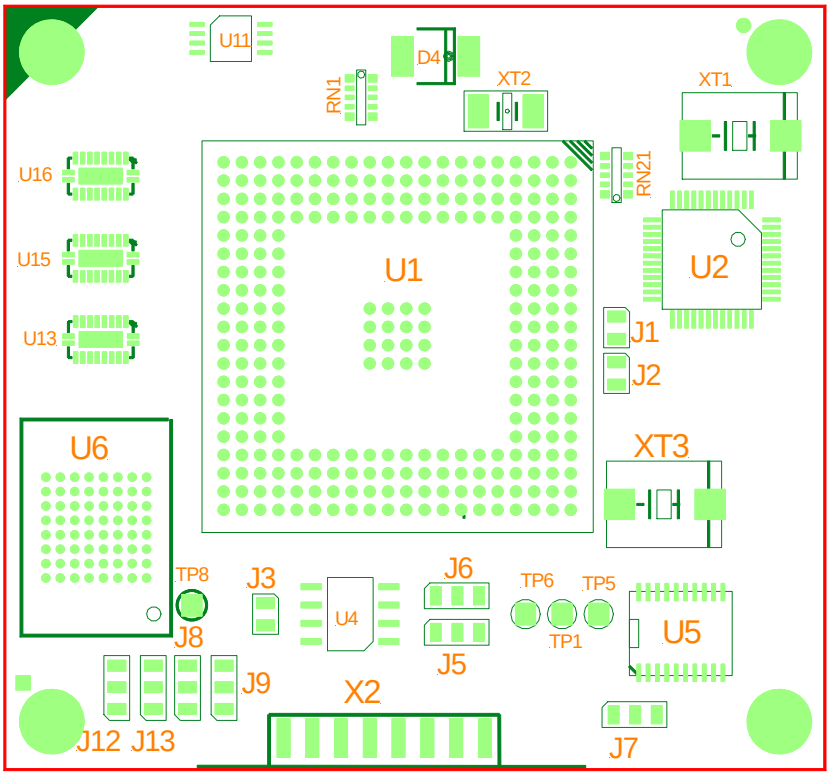


Figure 2: View of the phyCORE-MPC5200B tiny PCB Rev. 1245.1

1.3 Minimum Requirements to Operate the phyCORE-MPC5200B tiny

Basic operation of the phyCORE-MPC5200B tiny only requires supply of a +3V3 input voltage and the corresponding GND connection.

These supply pins are located at the phyCORE-connector X1:

+3V3	X1	1C, 2C, 4C, 5C, 1D, 2D
GND	X1	3C, 3D, 7C, 9D, 12C, 14D

Caution:
We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-MPC5200B tiny and at least the matching number of GND pins neighboring the +3 V3 pins.

In addition, proper implementation of the phyCORE module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to section 4 for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Many of the phyCORE-MPC5200B tiny pins offer alternative functions. These alternative functions must be activated by configuring the applicable controller registers prior to their use. Certain controller functions are pre-configured based on the module's design and are shown in *Table 1*. Signals that are routed directly from the CPU to the Molex connectors can configured to any available alternative function desired by the user. In contrast, signals that are used on the phyCORE-MPC5200 tiny as listed in *Table 1* can only be used if a special module configuration was purchased (e.g. SBC version without on-board RS-232 transceivers. Please contact PHYTEC for more details.

Note:
The following sections of this manual assume use of the port pins according to configuration listed in *Table 1*.

CPU Port	Function	Port_conf Register Bits	Used on phyCORE SBC
PSC1	AC97_1	01x [29:31]	No
PSC2	CAN 1/2	001 [25:27]	No
PSC3	UART3/SPI	1100 [20:23]	Yes
USB	USB	01 [18:19]	No
Ethernet	Ethernet w/ MD	0101 [12:15]	Yes
Timer	ATA_CS	00_11 [2:3_6:7]	No
I2C	I2C1 / I2C2	default	Yes (I2C1 available)
PSC6	UART6	101 [9:11]	Yes

Table 1: Default Port Configuration

As *Figure 3* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector; *refer to section 2*). This allows the phyCORE-MPC5200B tiny to be plugged into any target application like a "big chip".

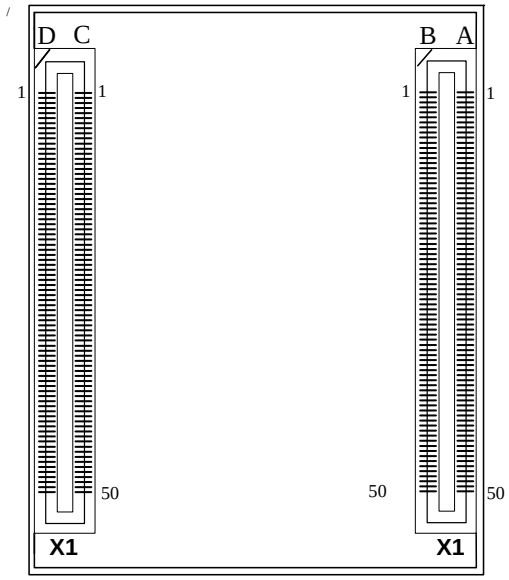


Figure 3: Pinout of 0the phyCORE-MPC5200B tiny (Bottom View)

Table 2 provides an overview of the pinout of the phyCORE-connector.

Please refer to the Freescale MPC5200B User Manual/Data Sheet for details on the functions and features of controller signals and port pins.

Pin Number	Signal	I/O	Comments
Pin Row X1A			
1A	NC	-	Not connected
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A	GND	-	Ground 0 V
3A	/IRQ3	I	Interrupt input 3 of the processor.
4A	/IRQ0	I	Interrupt input 0 of the processor.
			LocalPlus Bus control signals
5A	/LP_CS1	O	Chip Select 1
6A	/LP_ALE	O	Address Latch Enable
8A	/LP_RD#WR	O	Read, not Write
29A	/LP_Ts	O	Transfer Start
30A	/LP_Cs4	O	Chip Select 4
31A	/LP_Cs6	O	Chip Select 6 (PSC3 is UART3)
		I/O	***LocalPlus Address/Data Signals***
9A	EXT_AD1		
10A	EXT_AD2		
11A	EXT_AD4		
13A	EXT_AD7		
14A	EXT_AD9		
15A	EXT_AD10		
16A	EXT_AD12		
18A	EXT_AD15		
19A	EXT_AD17		
20A	EXT_AD18		
21A	EXT_AD20		
23A	EXT_AD23		
24A	EXT_AD25		
25A	EXT_AD26		
26A	EXT_AD28		
28A	EXT_AD31		
33A	ETH_TXD3	O	Already used by the MII interface between CPU and Ethernet PHY. Could be used as ***J1850_TX*** signal, if the PHY is not populated or in "isolation mode". The pin state is latched by the CPU after reset and used as "byte lane swap" configuration. *Refer to section 5, "System Start-Up Configuration"*. There is a 10kOhm pull-down resistor on this signal..
			ATA Interface Signals
34A	ATA_CS_0	O	Timer Port configured as ATA_CS (Timer0)
35A	ATA_CS_1	O	Timer Port configured as ATA_CS (Timer1)
36A	ATA_IOCHRDY		ATA negated to extend transfer
38A	/ATA_IOR	O	ATA read
39A	ATA_INTRQ	I	ATA interrupt request

Pin Number	Signal	I/O	Comments
			Dedicated PCI Signals
40A	/PCI_RESET	O	Reset output (open drain)
41A	/PCI_GNT	O	Bus grant
43A	/PCI_CBE_3	O	Command byte enable 3
44A	/PCI_CBE_2	O	Command byte enable 2
45A	/PCI_IRDY	O	Initiator (HOST) ready
46A	/PCI_DEVSEL	O	Device select
48A	/PCI_PERR	O	Parity error
49A	/PCI_SERR	O	System Error (open drain)
50A	/PCI_CBE_1	O	Command byte enable 1

Pin Number	Signal	I/O	Comments
Pin Row X1B			
1B	RTC_CLKOUT	O	Clock output of the I²C RTC U5
2B	/IRQ1	I	Interrupt input 1 of the processor
3B	/IRQ2	I	Interrupt input 2 of the processor
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 41B, 44B, 49B	GND		Ground 0 V
			LocalPlus Bus Signals
5B	/LP_CS2	O	Chip Select 2
6B	/LP_CS3	O	Chip Select 3
7B	/LP_Oe	O	Output Enable
28B	LP_Ack		Acknowledge
30B	/LP_CS5	O	Chip Select 5
31B	/LP_CS7	O	Chip Select 7 (PSC3 is UART3)
		I/O	***LocalPlus Address/Data Signals***
8B	EXT_AD0		
10B	EXT_AD3		
11B	EXT_AD5		
12B	EXT_AD6		
13B	EXT_AD8		
15B	EXT_AD11		
16B	EXT_AD13		
17B	EXT_AD14		
18B	EXT_AD16		
20B	EXT_AD19		
21B	EXT_AD21		
22B	EXT_AD22		
23B	EXT_AD24		
25B	EXT_AD27		
26B	EXT_AD29		
27B	EXT_AD30		
32B	Test_Sel_1	I/O	Input in CPU production test. Can be configured as LocalPlus-Bus TSIZ bit *Refer to section 7.3.2.1.1 in the MPC5200 controller User's Manual.*
33B	ETH_RXD1	I	Already used by the MII interface between CPU and Ethernet PHY. Can be used as ***J1850_RX*** signal, if the PHY is not populated or in "isolation mode".
			ATA Interface Signals
35B	ATA_DRQ	I	ATA DMA request
36B	/ATA_IOW	O	ATA write
37B	ATA_Isolation	O	ATA write enable for PCI bus sharing
38B	/ATA_DACK	O	ATA DMA acknowledge

Pin Number	Signal	I/O	Comments
			Dedicated PCI Signals
40B	PCI_CLOCK	O	PCI and external peripheral clock
42B	/PCI_REQ	O	PCI bus request
43B	PCI_IDSEL	O	Initial device select
45B	/PCI_FRAME	O	Frame start
46B	/PCI_TRDY	I	Target ready
47B	/PCI_STOP	O	Transition stop
48B	PCI_PAR	O	Bus parity
50B	/PCI_CBE_0	O	Command byte enable 0

Pin Number	Signal	I/O	Comments
Pin Row X1C			
1C, 2C, 4C, 5C	+3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C	GND	-	Ground 0 V
6C	VBAT	I	Connection for external battery (+) 2.4 - 3.3 V to supply (backup) the RTC U5
8C	ETH_TXD1	O	Already used by the MII-Interface between CPU and Ethernet PHY. The pin state is latched by the CPU after reset and used as "boot high" configuration. Refer to section 5 "System Start-Up Configuration". A 10kOhm pull-up resistor is connected to this signal.
9C	GPIO_WKUP_6	I/O	Dedicated GPIO with wakeup capability **Note: This is a 2.5V based GPIO!!!**
10C	/SRESET	I/O	External SRESET is an open drain signal which is connected to a 10 kOhm pull-up resistor on the module. Assertion of SRESET causes assertion of the internal soft reset. Internal soft reset is actually an interrupt that takes the same exception vector as HRESET. In particular, this means that SRESET cannot abort a hung XLB operation, and no device should use SRESET in a way that interferes with any bus operation in progress. SRESET can also be asserted by internal sources. When SRESET is asserted internally, external SRESET is also asserted.
11C	/HRESET	I/O	HRESET is a bi-directional signal with a Schmitt-trigger input and an open drain output. The HRESET signal is connected a 10 kOhm pull-up resistor on the module. Assertion of external HRESET causes external HRESET and SRESET as well as internal hard and soft resets to be asserted for at least 4096 reference clock cycles. During PORRESET or HRESET the reset configuration word is sampled to establish the initial state of various vital internal MPC5200B functions. The reset configuration word is latched internally when PORRESET or HRESET is released.
			AC97 Codec Signals (PSC1)
13C	AC97_1_RES	O	Reset signal to the external AC97 device
14C	AC97_1_SYNC	O	Frame sync, or start-of-frame (SOF)
15C	AC97_1_BITCLK	I	Driven by the external serial bit-clock
16C	AC97_1_SDATA_IN	I	Receiver serial data input
18C	CAN2_TX	O	CAN transmit output of the second CAN interface (PSC2)
19C	UART6_RXD_TTL	I	PSC6 receive data signal
20C	UART6_TXD_TTL	O	PSC6 transmit data signal

Pin Number	Signal	I/O	Comments
21C	RXD6_232	I	RxD input on the RS-232 transceiver for the MPC UART (PSC6)
23C	TXD6_232	O	TxD output on the RS-232 transceiver for the MPC UART (PSC6)
Pin Row X1C			
24C	/UART6_RTS_TTL	I	PSC6 request to send signal
25C	/UART6_CTS_TTL	O	PCS6 clear to send signal
			Second I²C Interface
26C	I2C2_CLK	I/O	Clock (SCL)
28C	I2C2_IO	I/O	Data (SDA)
29C	Timer4	I/O	Timer 4 signal of the MPC5200B
30C	Timer5	I/O	Timer 5 signal of the MPC5200B
31C	I2C1_CLK	I/O	Clock for first I2C-Interface (SCL)
			10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are NC)
33C	ETH_LINK	O	Link/Activity LED (L=link; toggle=act)
34C	ETH_SPEED	O	Speed LED (H=10 Mbit/s, L=100 Mbit/s)
35C	ETH_RX-	I	Differential receive input
36C	ETH_TX-	O	Differential transmit output
38C	/ETH_PD	I	Power down
41C	ET_NWAYEN	O	Collision LED (H = no collision)
			JTAG Interface
39C	/COP_TRST	I	JTAG reset input. Via logic OR connected to /PORRESET resulting in /CPU_TRST signal.
40C	CK_STOP	O	Scan enable, clock stop
43C	PSC2_4	I/O	Freely available GPIO with wakeup function
44C	Timer6	I/O	Timer 6 signal of the MPC5200B
			USB1 (Host)
45C	USB1_OVRCRNT	I	Over current
46C	USB1_SUSPEND	O	Suspend
48C	USB1_RXN	I	Receive negative
49C	USB1_TXN	O	Transmit negative
50C	/USB1_OE	O	Output enable
Pin Row X1D			
1D, 2D	+3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D	GND	-	Ground 0 V
4D, 5D	NC	-	Not connected
6D	VCC_SRAM	O	VCC_SRAM supply voltage is generated by VBAT or +3V3 using a battery backup circuit (MAX6364). VCC_SRAM serves as supply voltage for the Real-Time Clock.
7D	RESOUT	O	Reset output of the voltage supervisor circuit
8D	/PHYReset	I	A low on this pin forces only the PHY into reset state

Pin Number	Signal	I/O	Comments
10D	/RESIN	I	Reset input signal of the MPC5200B tiny. It could be asserted via connection to a reset push button. Signal connected to +3V3 via 10 kOhm pull-up resistor.
11D	GPIO_WKUP_7	I/O	Dedicated GPIO with wakeup capability
12D	Timer2	I/O	Timer 2 signal of the MPC5200
13D	Timer3	I/O	Timer 3 signal of the MPC5200

Pin Number	Signal	I/O	Comments
Pin Row X1D			
			AC97 codec signal (PSC1)
15D	AC97_SDATA_OUT	O	Receiver serial data output
16D	UART3_RXD_TTL	I	PSC3 receive data signal
17D	UART3_TXD_TTL	O	PSC3 transmit data signal
18D	CAN2_RX	I	CAN receive of the second CAN interface (PSC2)
20D	CAN1_RX	I	CAN receive of the first CAN interface (PSC2)
21D	CAN1_TX	O	CAN transmit of the first CAN interface (PSC2)
22D	RXD3-232	I	RxD input on the RS-232 transceiver for UART3 (PSC3).
23D	TXD3-232	O	TxD output on the RS-232 transceiver for UART3 (PSC3).
25D	/UART3_RTS_TTL	I	PSC3 request to send signal
26D	/UART3_CTS_TTL	O	PCS3 clear to send signal
			SPI Interface (PSC3)
27D	SPI_MOSI	I/O	SPI master out slave in
28D	SPI_MISO	I/O	SPI master in slave out
30D	SPI_CLK	I/O	SPI clock
31D	SPI_SS	O	SPI slave select
32D	I2C1_IO	I/O	Data line of first I2C interface (SDA)
33D	/IRQ_RTC	O	Interrupt from the on-board RTC U5. Interrupt can be programmed to occur to a specific time or date.
			10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are* NC0*)
35D	ETH_RX+	I	Differential receive input
36D	ETH_TX+	O	Differential transmit output
37D	/ETH_INT	O	MII interface interrupt
			MPC5200B JTAG interface
38D	CPU_TCK	I	Clock
40D	CPU_TDI	I	Data in
41D	CPU_TDO	O	Data out
42D	CPU_TMS	I	Mode select
43D	Timer7	I/O	Timer 7 signal of the MPC5200B
			USB1 (host)
45D	USB1_PORTPWR	O	Enable/disable port power
46D	USB1_SPEED	O	Speed select
47D	USB1_RXD	I	Receive data
48D	USB1_RXP	I	Receive positive
50D	USB1_TXP	O	Transmit positive

Table 2: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-MPC5200B tiny has 10 solder jumpers, some of which have been installed prior to delivery. *Figure 4* illustrates the numbering of the jumper pads, while *Figure 5* indicates the location of the jumpers on the board.

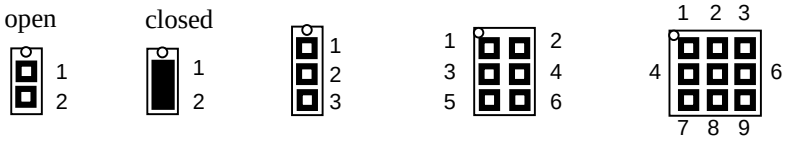


Figure 4: Numbering of the Jumper Pads

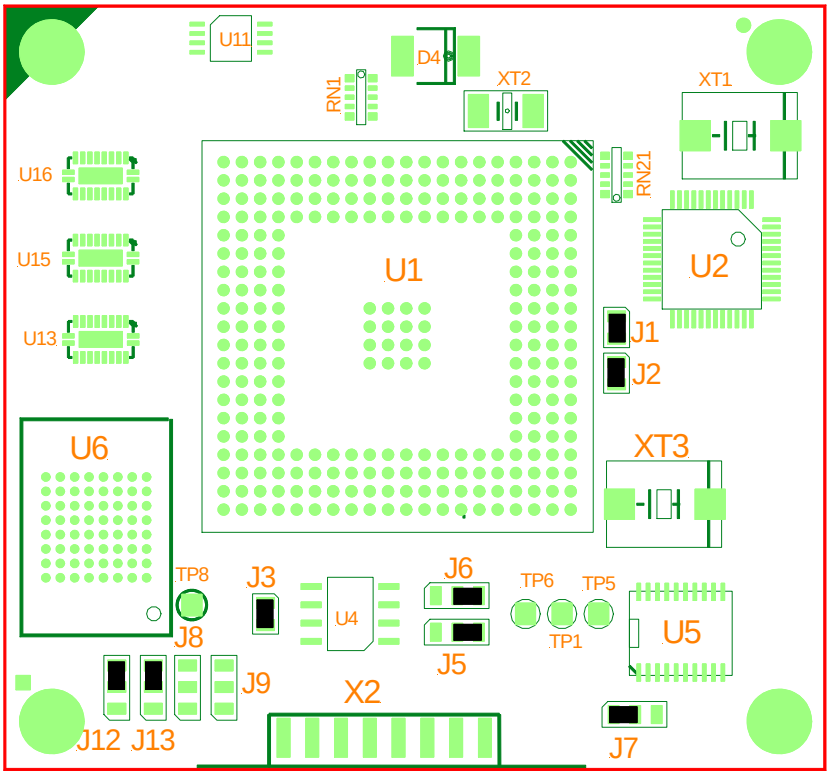


Figure 5: Location of the Jumpers (Controller Side)
(phyCORE-MPC5200B tiny Standard Version)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1, J2		J1 and J2 disconnect the receive lines (UART3_RXD_TTL and UART6_RXD_TTL) of the MPC5200B PSC3 and PSC6 from the RS-232 transceiver at U3. This makes the controller's TTL signals available at pins X1D16 (UART3_RXD_TTL) and X1C19 (UART6_RXD_TTL). This is useful, for instance, for optical isolation of the RS-232 interface.
open		The UART receive signals UART3_RXD_TTL and UART6_RXD_TTL are disconnected from the RS-232 transceiver.
closed	X	The UART receive signals UART3_RXD_TTL and UART6_RXD_TTL are connected to the on-board RS-232 transceiver.
Package Type		0R in SMD 0805
J3		J3 connects pin 7 of the serial memory at U4 to 3V3. On many memory devices pin 7 enables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-MPC5200B tiny will have this write protection function. *Please refer to the corresponding memory data sheet for more detailed information.*
open	X	
closed		
Package Type		0R in SMD 0805
J5, J6		J5 and J6 define the slave addresses (A1 and A2) of the serial memory U4 on the I^2C2 bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. A0 is tied to GND. It must be noted that the RTC at U5 is also connected to the I^2C bus. The RTC has the address 0xA2/0xA3 which cannot be changed.
1 + 2, 2 + 3	X	A2= 0, A1= 0, A0= 0 (0xA0 / 0xA1) I^2C slave address 0xA0 for write operations and 0xA1 for read access.
1 + 2, 1 + 2		A2= 1, A1= 0, A0= 0 (0xA8 / 0xA9)
2 + 3, 2 + 3		A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5)
2 + 3, 1 + 2		A2= 1, A1= 1, A0=0 (0xAC / 0xAD)
Package Type		0R in SMD 0805

Jumper	Default	Comment	
J7		Enables or disables the clock output of the I²C RTC U5 RTC clockout is connected to X1B1.	
1 + 2	X	RTC clockout disabled	
2 + 3		RTC clockout enabled	
Package Type		0R in SMD 0805	
J12 **J13**		Pll_cfg3 = 1 Pll_cfg2 = 1	These jumpers define the core PLL configuration. *Refer to the "MPC5200B controller User's Guide"*. The default configuration 0x08 defines a bus-to-core clock ratio of 1:3.
1 + 2	X	Logic 1	
2 + 3		Logic 0	
Package Type		**10 kOhm resistor** in SMD 0805	
J8, J9	-	These jumpers are reserved for factory settings!	
		Do not change these jumper settings!	

Table 3: Jumper Settings

4 Power Requirements

The phyCORE-MPC5200B tiny must be supplied with one supply voltage only:

Supply voltage: +3.3 V ±10 % with 1.2 A load

Caution:
Connect all +3V3 input pins to your power supply and at least the matching number of GND pins neighboring the +3V3 pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

Optional Supply Input VBAT

VBAT is the input pin that supplies the Real-Time Clock (U5). The MAX6364 battery supervisor IC (U12) senses the 3.3 V main supply and VBAT and switches to the voltage with the higher level. VBAT should be supplied from a 3 V source (i.e. lithium battery).

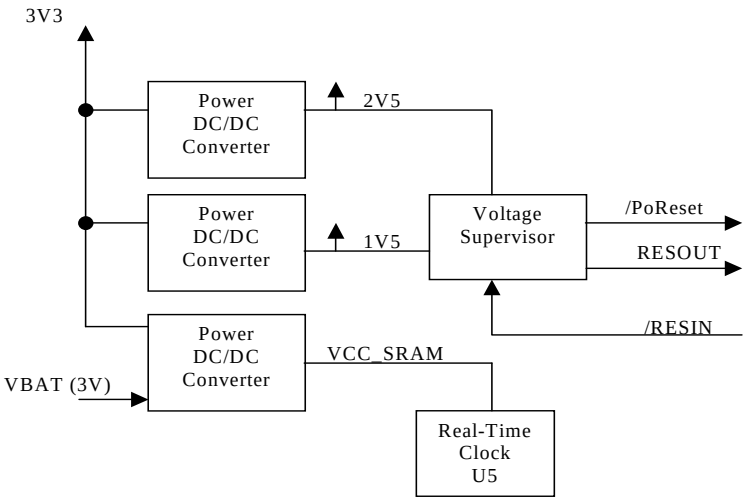


Figure 6: Power Supply Diagram

Internally generated voltages: 1V5, 2V5

- 3 V3 PowerPC I/O, Flash memory
- 2 V5 DDR SDRAM and Ethernet PHY
- 1 V5 PowerPC Core

4.1 Voltage Supervision and Reset

The input voltage 3V3 as well as the on-board generated operation voltages 2V5 and 1V5 are monitored by a voltage supervisor device at U11. This circuitry is responsible for generation of the system reset signal /PoReset. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /PoReset line will be inactive (high). /PoReset connects to the processor reset input.

/PoReset is combined via the diodes D5 and D6 with /COP_TRST to a logic OR with /CPU_TSRT (JTAG controller reset) as output. This logic connection is used to ensure a proper reset of the CPU internal debug interface by /PoReset or by the COP signal /COP_TRST.

The voltage supervisor's master reset input /RESIN can be connected to an external signal or switch to release a asynchronous reset manually.

5 System Start-Up Configuration

During the reset cycle the MPC5200B processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitry (pull-up or pull-down resistors) is located on the phyCORE module.

The system start-up configuration includes:

- Clock configuration
- Basic LocalPlus characteristic for boot memory configuration

Note:
Since most of these signal lines are routed to the phyCORE connector care must be taken not to overwrite the startup configuration accidentally when connecting these signals to external devices.
-

The following default configuration is read by the processor with the rising edge of the reset line /PoReset. The logic level of the signals written in *italic style* could be configured via solder jumpers on-board *(refer to section 3)*

Signal Name	Register Bit	Logic Level	Description
/LP_Ale LP_RD/WR */ATA_low* */ATA_lor* /ATA_Dack	PPC_pll_cfg [0..4]	0 1 0 0 0	Bus clock ratio XLB: core clock = 1:3 132 MHz * 3 = 396 MHz
/LP_Ts	xlb_clk_sel	0	Bit=0: XLB_CLK = fsystem / 4 Bit=1: XLB_CLK = fsystem / 8
USB1_TXN	sys_pll_cfg0	0	Bit =0: fsystem = 16x SYS_XTAL_IN Bit =1: fsystem = 12x SYS_XTAL_IN
USB1_TXP	sys_pll_cfg1	0	Bit=0: fvcosys = fsystem Bit=1: fvcosys = 2 x fsystem
ETH_TXEN	boot_rom_mg	0	Bit=0: No boot in most graphics mode 1 Bit=1: Boot in most graphics mode
ETH_TXD1	ppc_msrip	1	Bit=0: 0000_0100 (hex) boot address Bit=1: FFF0_0100 (hex) boot address
ETH_TXD2	boot_rom_wait	1	Bit=0: 4 PCI bus clocks of wait state Bit=1: 48 PCI bus clocks of wait state
ETH_TXD3	boot_rom_swap	0	Bit=0: no byte lane swap, same endian ROM image Bit=1: byte lane swap, different endian ROM image
ETH_TXERR	boot_rom_size	0	Boot ROM address is max 25 significant bits during address tenure. Bit=0: 16-bit ROM data bus Bit=1: 32-bit ROM data bus
ETH_MDC	boot_rom_type	1	Bit=0: non-muxed boot ROM bus, single tenure transfer. 1 Bit=1: muxed boot ROM bus, with address and data tenures, ALE and TS active. 1
ETH_TXD0	large_flash_sel	0	Bit=0: No boot in large Flash mode 1 Bit=1: Boot in large Flash mode 1,3,4

Table 4: System Start-Up Configuration

6 System Memory

The system memory consist of Flash memory, DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) and a small non-volatile memory device:

- 16 MByte Intel Strata Flash memory (1x 16-bit, multiplexed mode)
- 64 MByte DDR SDRAM (2x 16-bit)
- 4 kByte serial memory (EEPROM)

The Flash memory is connected to the PowerPC LocalPlus bus and is controlled by /CS0. This Chip-Select signal is used for boot operation.

The DDR SDRAM is connected to the special SDRAM interface of the MPC5200B processor and operates at the maximum frequency (132 MHz).

Communication to the small non-volatile memory device (EPROM) is established over the processor's I^2C bus. This memory device holds the boot loader (U-Boot) environment variables in its first two kilobytes and can be used for parameter storage.

6.1 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-MPC5200B tiny provides an easily reprogrammable means of code storage.

- 16 MByte Intel Strata Flash memory
- 16-bit bus width
- Only asynchronous operation is possible

The Flash memory bank supports the following Intel memory devices:

Type	Size	Manufacturer	Device Code	Manufacturer Code
Asynchronous Devices				
28F128J3	16 MByte	Intel	0x0018	0x0089

Table 5: Choice of Flash Memory Devices and Manufacturers[1]

The organization of the Flash memory bank is 16-bit. The Flash memory bank is controlled by the processor Chip Select signal /CS0. This Chip Select signal is the dedicated control signal for boot purposes.

The MPC5200B's LocalPlus bus can be configured for many different bus modes. For /CS0 the 25-bit address / 16-bit data multiplexed mode was chosen because it offers the largest address space without interfering the ATA or PCI bus. With 25 address lines a total of 32 MByte of data/code can be addressed. It is possible to use different bus modes on other available Chip Select signals.

The Flash memory bank 0 starts at address 0x0000_0100 or 0xFFFF_0100 depending on the startup configuration and relative to the base address of the processor's Chip Select signal /CS0.

The access speed depends on the equipped memory device. The LocalPlus Bus clock cycle is determined by the PCI clock which is configured by the PCI clock divider. A typical configuration selects 66 MHz. The resulting basic cycle time is 15.15 ns.

[1]: Flash types in the shaded lines are the preferred parts for the phyCORE-MPC5200B tiny.

The MPC5200B processor multiplexed read or write is divided into a address tenure and a data tenure. Because the Chip Select signal is generated with the start of the data tenure only this period is of interest for access time calculation.

The equation for access time calculation is: $(2+WS) * t_{PCICK} - 8.5$ ns

To support all memory speed grades up to 75 ns at least 4 wait states must be added for /CS0.

- 4 wait states for /CS0 (supports 66 MHz PCI clock)

No additional voltages are needed for in-system programming. As of the printing of this manual, Flash devices generally guarantee at least 100,000 erase/programming cycles. *Refer to the applicable INTEL data sheet for detailed description of the erasing and programming procedure.*

6.2 DDR SDRAM

The phyCORE-MPC5200B tiny is equipped with fast **D**ouble **D**ata **R**ate **S**ynchronous **D**ynamic **R**andom **A**ccess **M**emory (DDR SDRAM) devices. This memory is connected to a dedicated SDRAM interface provided by the MPC5200B processor.

The DDR SDRAM memory bank consist of two 16-bit data port devices connected in parallel to support the 32-bit bus width of the processor. The memory bank is controlled by Chip Select signal /SD_CS0 of the processor's DDR SDRAM controller.

Table 6 shows all possible memory configurations.

Available Capacity	Device Organization	Devices (two)
32 MByte	128 MBit 2 MBit x 16 x 4 banks	MT46V8M16 TSOP66 packaging
64 MByte	256 MBit 4 MBit x 16 x 4 banks	MT46V16M16 TSOP66 packaging
128 MByte	512 MBit 8 MBit x 16 x 4 banks	MT46V32M16 TSOP66 packaging

Table 6: DDR SDRAM Device Selection

6.3 Serial Memory

The phyCORE-MPC5200B tiny features a non-volatile memory device (EEPROM) with a serial I^2C interface. This memory can be used for storage of configuration data or operating parameters that must be maintained in the event of a power interruption. The available capacity is 4 kByte.

Note:
The first 2 kilobytes section of the EEPROM is already used for storing the boot manager (U-Boot) environment variables. This portion must not be used by user data.

The MPC5200B processor provides two on-chip I^2C interfaces. The memory device is connected to I²C interface #2.

Table 7 gives an overview of the possible devices for use at U4 as of the printing of this manual.

Type	Size	I^2C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	4 kBytes	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32	CATALYST

Table 7: Serial Memory Options for U4

It is important to note that the RTC U5 is also connected to the I^2C #2 bus. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I^2C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using solder jumpers J5 (A1) and J6 (A2) to avoid bus collision. The address input A0 is hard-wired to GND.

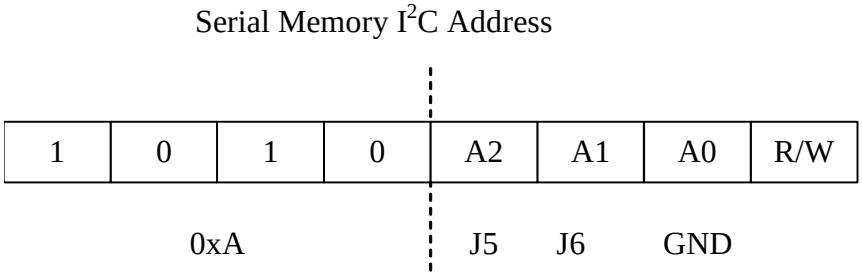


Figure 7: Serial Memory I²C Slave Address

Possible configuration options are shown below:

I²C Address	**J5 A1**	**J6 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 8: Serial Memory I²C Address (Examples)

Address lines A1 and A2 are not always made available with certain serial memory types. This should be noted when configuring the I²C bus slave address.

7 Serial Interfaces

7.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC5200B tiny at U3. This device adjusts the signal levels of the UART3_RXD/TXD_TTL and UART6_RXD/TXD_TTL lines (MPC5200B PSC3/PSC6). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXD3-232 or RXD6-232 line (X1D22/X1C21) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXD3-232 or TXD6-232 line (X1D23/X1C23) is connected to the RXD line of the COM port. The Ground circuitry of the phyCORE-MPC5200B tiny must also be connected to the applicable Ground pin on the COM port.

The processor's on-chip UART supports handshake signal communication. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore it is possible to use the TTL signals of both of the UART channels externally. These signals are available at X1D16, X1D17 (UART3_RXD_TTL, UART3_TXD_TTL) and X1C19, X1C20 (UART6_RXD_TTL, UART6_TXD_TTL) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals. Using solder jumpers J1 and J2, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines UART3_RXD_TTL and UART6_RXD_TTL. This is required so that the external transceiver does not drive signals against the on-board transceiver. The transmit lines UART3_TXD_TTL / UART6_TXD_TTL can be connected parallel to the transceiver input without causing any signal conflicts.

7.2 Ethernet Interface

Connection of the phyCORE-MPC5200B tiny to the world wide web or a local network (LAN) is possible over the integrated FEC (Fast Ethernet Controller) of the Freescale processor. The FEC operates with a data transmission speed of 10 or 100 Mbit/s.

7.2.1 PHY Physical Layer Transceiver

The phyCORE-MPC5200B tiny has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED monitoring signals extends to phyCORE-connector X1. In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module.

If you are using the applicable Development Board for the phyCORE-MPC5200B tiny (part number PCM-997 + EAD-003-MPC5200), the external circuitry mentioned above is already integrated on the board (*refer to section 14*).

The default PHY address configured with the boot-strapping option is 0x1.

Table 9 shows the interface signals for the Ethernet channel.

FEC Channel PHY U2	Pin Function	Location at phyCORE-Connector
ETH_RX+	Differential positive receive input signal	X1D35
ETH _RX-	Differential negative receive input signal	X1C35
ETH _TX+	Differential positive transmit output signal	X1D36
ETH _TX-	Differential negative transmit output signal	X1C36
ETH _LED0	Link/activity LED output "H"/LED off no link "L"/LED on link "toggle"/LED toggle activity	X1C33
ETH _LED1	Speed LED output "H"/LED off 10BT "L"/LED on 100BT	X1C34
ETH_LED3	Collision LED output "H"/LED off no collision "L"/LED on collisions	X1C41

Table 9: Signal Definition PHY Ethernet Port (U2)

7.2.2 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC5200B is located on the bar code sticker attached to the module. This number is a 12-position HEX value.

7.3 USB 1.1 Host Interface

The MPC5200B integrates a USB 1.1 compliant host interface with two ports. This interface supports full-speed (12 Mbit/s) transmission rates. The USB 1.1 controller is integrated in the MPC5200B processor. The physical layer transceiver unit must be connected externally, it is **not** populated on the phyCORE module.

For additional information of the USB 1.1 controller refer to the MPC5200B Reference Manual as well as the USB 1.1 bus specification provided by www.usb.org.

8 The U-Boot Boot Loader

"U-Boot" is a universal boot loader firmware based on GPL (Gnu Public License). Its main function is initializing the system hardware following a reset followed by starting application software such as an operating system.

Furthermore, U-Boot provides various functions to query system information and to change the start-up behavior of the target system. For example U-Boot allows to choose from different boot sources (such as Ethernet, etc.). It also provides functions to download application code into Flash.

The serial interface is used to communicate with U-Boot on the target system. The U-Boot for phyCORE-MPC5200B tiny uses PSC3 with 115,200 Baud, 8, N, 1. The U-Boot boot messages can be viewed within a terminal program running on a host PC using the above mentioned communication settings.

Note:
PHYTEC delivers all phyCORE-MPC5200B tiny modules with a pre-installed U-Boot allowing the user immediate startup. The U-Boot software project is subject to continuous maintenance and improvements. Firmware updates will occur without special notification. Should you require a specific version of U-Boot pre-installed at time of delivery please contact PHYTEC's sales department.

If U-Boot is used as boot loader firmware and basic component of the system software, the user should be familiar with the following topics in order to ensure proper function:

- U-Boot default system configuration
- system resources required by U-Boot
- modifying the U-Boot loader

8.1 U-Boot Default System Configuration

The U-Boot boot loader changes the following default settings to different than the reset values of the controller on the phyCORE-MPC5200B tiny:

Clock:

Core = 396 MHz, IPB=132 MHz, PCI=66 MHz

Memory Base Address Register (MBAR):

0xF0000000

DDR-RAM:

Automatic storage size detection; start address 0x0

Flash:

Chip Select = /CSBoot, 16-bit data bus width, 25 address lines, multiplexed mode, 4 wait states; 16 MByte starting at address 0xFF000000

PSC2:

CAN1&2

PSC3 :

UART, 115200 baud, 8,N,1 ; SPI

PCI :

disabled

Ethernet :

100 Mbit/s with MD

I²C_2: EEPROM at address 0x52, RTC at address 0x51

8.2 System Resources Required by U-Boot

U-Boot is located at address 0xFFF0 0000 in the module's Flash and occupies two sectors (2x 128kByte). The boot loader itself makes sure that these sectors are protected using the Flash's "locked sector" mechanism. This makes accidental erasure of U-Boot almost impossible. Following a system start at address 0xFFF0 0100 (high boot), U-Boot first initializes the DDR-RAM interface, then copies itself to the upper end of the RAM memory space and transfers program execution to this address. As a result U-Boot now runs out of RAM which allows for reprogramming itself in Flash (firmware update).

So called environment variables are used to configure U-Boot. Such variables define the IP number as well as the MAC address using Ethernet configuration as example. The variables are saved in the module's EEPROM (U4) and occupy the first 2 kByte.

When using the RAM memory, care should be taken to not overwrite the U-Boot code as well as the trap table which is located in the lower portion of the RAM. Among other factors, the size of the U-Boot stack determines how much memory at the upper end of the RAM memory range is occupied by U-Boot. As U-Boot is used the stack size is growing and more memory space is required. It is recommended to reserve a sufficient RAM portion to be used for the stack beginning at the stack start address.

8.2.1 The "Backup" U-Boot

In the event the "original" U-Boot at address 0xFFF0 0000 becomes corrupted (e.g. by overwriting the loader with a wrong version) a second U-Boot loader at address 0xF000 0000 is available as an "emergency" backup version providing the same functionality as the original copy. This backup U-Boot can be started by connecting a 4.7 kOhm pull down resistor at pin X1-C8 during a hardware reset cycle.

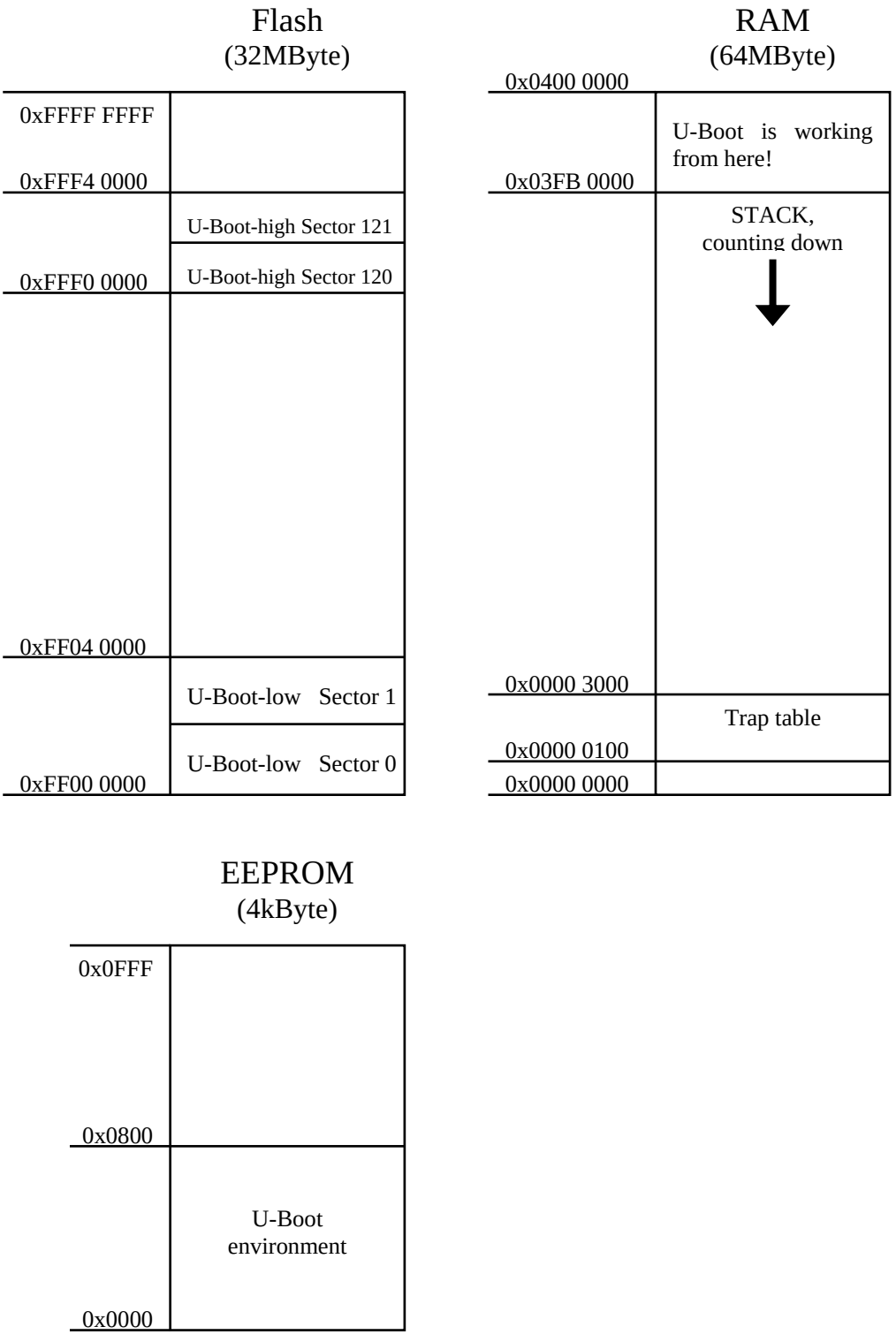


Figure 8: U-Boot Memory Map

8.3 Modifying the U-Boot Loader

Changing the U-Boot should always be compared to recompiling the program code and updating the Flash contents. A detailed description of each individual step would by far exceed the scope of this Hardware Manual. Please refer to the Application Note "Configuring and Updating the Boot Loader", document number LAN-044 for more details.

9 JTAG Interface

The MPC5200B CPU provides a JTAG interface for connecting to debuggers, emulators and boundary scan. The JTAG interface signals extend to the module's phyCORE-connector. Furthermore, there is an on-board JTAG connector (X2) located at the edge of the module, which has the standard COP-Interface pinout but uses a 2.0 mm pin pitch instead of 2.54 mm. The connector is not populated on the standard version of the phyCORE-MPC5200B. You can order a specific debug version of the module (denoted by the –D part number extension) or populate a 2*8-pin header connector at space X2. The numbering scheme is depicted on the phyCORE-MPC5200B. The pinout of the JTAG interface at X2 is described in the following table.

Signal	Pin Row		Signal
	Bottom	**Top**	
TDO	1	2	NC (quack)
TDI	3	4	/TRST
NC (/halted)	5	6	3V3
TCK	7	8	NC
TMS	9	10	NC
/SReset	11	12	GND
/HReset	13	14	NC (key)
CK_Stop	15	16	GND

Table 10: JTAG Interface

10 Technical Specifications

The physical dimensions of the phyCORE-MPC5200B tiny are represented in *Figure 9.*

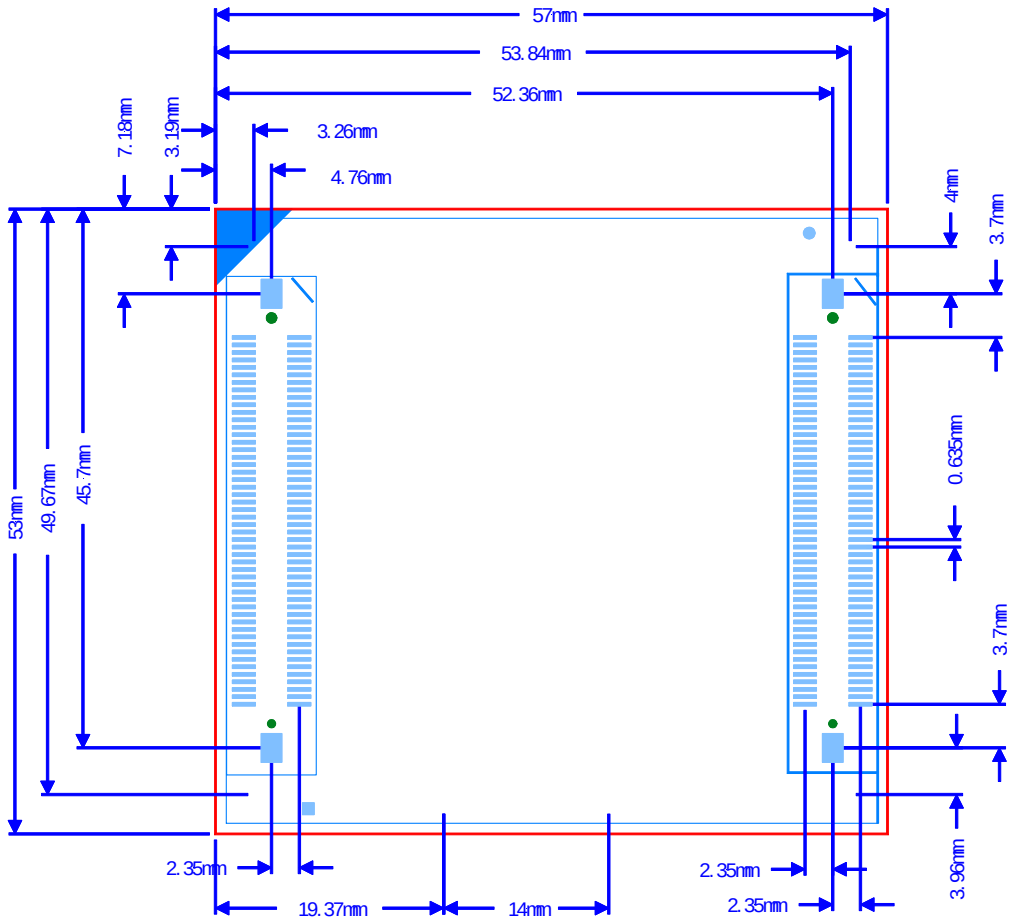


Figure 9: Physical Dimensions (Top View)

The height of all components on the top side of the PCB is ca. 2.5 mm. The PCB itself is approximately 1.6 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 2.5 mm.

Additional Technical Data:

Parameter	**Condition**	**Characteristics**
Dimensions		57 mm x 53 mm
Weight		approximately 25g with all optional components mounted on the circuit board
Storage Temp. Range		-40°C to +90°C
Operating Temp. Range: Extended		 -25°C to +85°C
Humidity		max. 95 % r.F. not condensed
Operating voltages: Voltage 3.3V		 3.3 V ±5 %
Operating Power Consumption: Voltage 3.3 V	(depending on load)	 Max. 4 watts

Table 11: Technical Data

These specifications describe the standard configuration of the phyCORE-MPC5200B tiny as of the printing of this manual.

Connectors on the phyCORE-MPC5200B tiny:

Manufacturer	Molex
Number of pins per contact rows	100 (2 rows of 50 pins each)
Molex part number (lead free)	52760-1009 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-PXA255. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2,5 mm) on the underside of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	100 (2 rows of 50 pins each)
Molex part number (lead free)	55091-1079 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number (lead free)	53553-1079 (header)

Please refer to the coresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

11 Hints for Handling the Module

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-MPC5200B tiny into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected

12 Real-Time Clock RTC-8564 (U5)

For real-time or time-driven applications, the phyCORE-MPC5200B tiny is equipped with a RTC-8564 Real-Time Clock at U5. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2
- Power consumption

  Bus active (400 kHz): < 1 mA

  Bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I^2C bus (address 0xA2 / 0xA3). Since the MPC5200B is equipped with an internal I^2C controller, the I^2C protocol is processed very effective without extensive processor action (*refer also to section 6.3)*

The Real-Time Clock also provides an interrupt output that extends to the /IRQRTC signal X1D33. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

If the RTC interrupt is to be used as a software interrupt via a corresponding interrupt input of the processor, the signal /IRQRTC must be connected externally with a processor interrupt input.

The RTC_CLKOUT signal can be programmed to various frequencies e.g. 1Hz. The RTC_CLKOUT output must be enabled via solder jumper J7.

For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.

Note:
After connection of the supply voltage the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

13 The phyCORE-MPC5200B tiny on the phyCORE Development Board HD200

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

13.1 Concept of the phyCORE Development Board HD200

The phyCORE Development Board HD200 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC5200B tiny Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.
This modular development platform concept is depicted in *Figure 10* and includes the following components:

- The actual **Development Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **serial interfaces** (3) of the SBC module at DB-9 connectors (depending on the module, up to two RS-232 interfaces and up to two RS-485 or CAN interfaces).
- All of the signals from the SBC module mounted on the Development Board extend to two mating receptacle connectors. A strict 1:1 signal assignment is consequently maintained from the phyCORE-connectors on the module to these expansion connectors. Accordingly, the pin assignment of the **expansion bus** (4) depends entirely on the pinout of the SBC module mounted on the Development Board.

- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Development Boards, we are able to offer various **expansion boards** (5) that attach to the Development Board at the expansion bus connectors. These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Development Board.
- All controller and on-board signals provided by the SBC module mounted on the Development Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Development Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 10 illustrates the modular development platform concept:

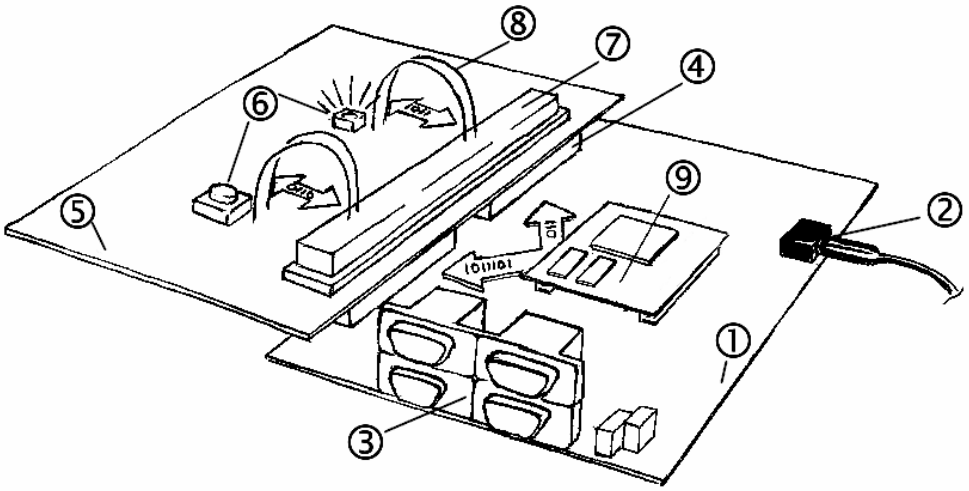


Figure 10: Modular Development and Expansion Board Concept with the phyCORE-MPC5200B tiny

The following sections contain specific information relevant to the operation of the phyCORE-MPC5200B tiny mounted on the phyCORE Development Board HD200. *For a general description of the Development Board, please refer to the corresponding Development Board Hardware Manual.*

13.2 Development Board HD200 Connectors and Jumpers

13.2.1 Connectors

As shown in *Figure 11*, the following connectors are available on the phyCORE Development Board HD200:

X1- low-voltage socket for power supply connectivity
X2- mating receptacle for expansion board connectivity
P1- dual DB-9 sockets for serial RS-232 interface connectivity
P2- dual DB-9 connectors for CAN or RS-485 interface connectivity
X4- voltage supply for external devices and subassemblies
X5- GND connector (for connection of GND signal of measuring devices such as an oscilloscope)
X6- phyCORE-connector enabling mounting of applicable phyCORE modules
X7- interface for Ethernet transformer module EAD-003
U9/U10- space for an optional silicon serial number chip
BAT1- receptacle for an optional battery

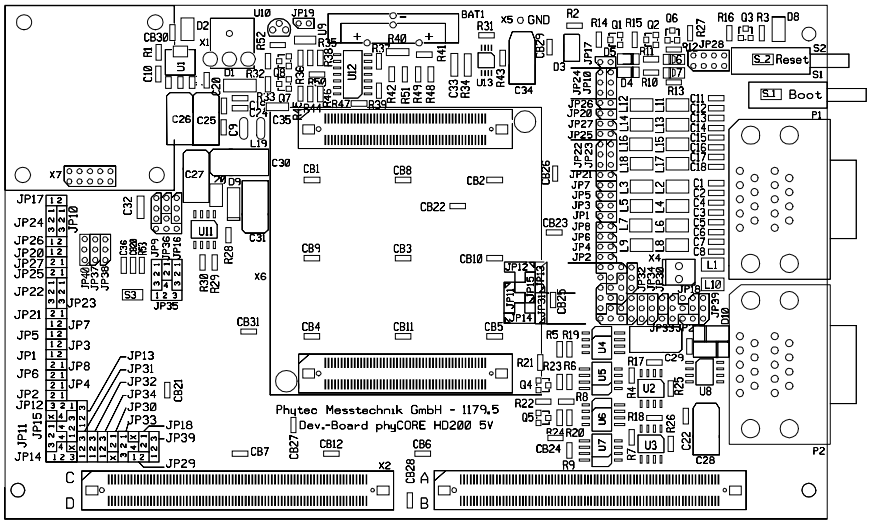


Figure 11: Location of Connectors on the phyCORE Development Board HD200

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

13.2.2 Jumpers on the phyCORE Development Board HD200

Peripheral components of the phyCORE Development Board HD200 can be connected to the signals of the phyCORE-MPC5200B tiny by setting the applicable jumpers.

The Development Board's peripheral components are configured for use with the phyCORE-MPC5200B tiny by means of removable jumpers. If no jumpers are set, no signals connect to the DB-9 connectors, the control and display units and the CAN transceivers. The Reset input on the phyCORE-MPC5200B tiny directly connects to the Reset button (S2). *Figure 12* illustrates the numbering of the jumper pads, while *Figure 13* indicates the location of the jumpers on the Development Board.

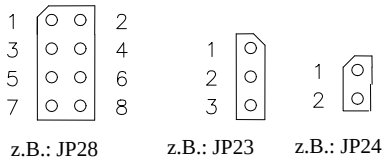


Figure 12: Numbering of Jumper Pads

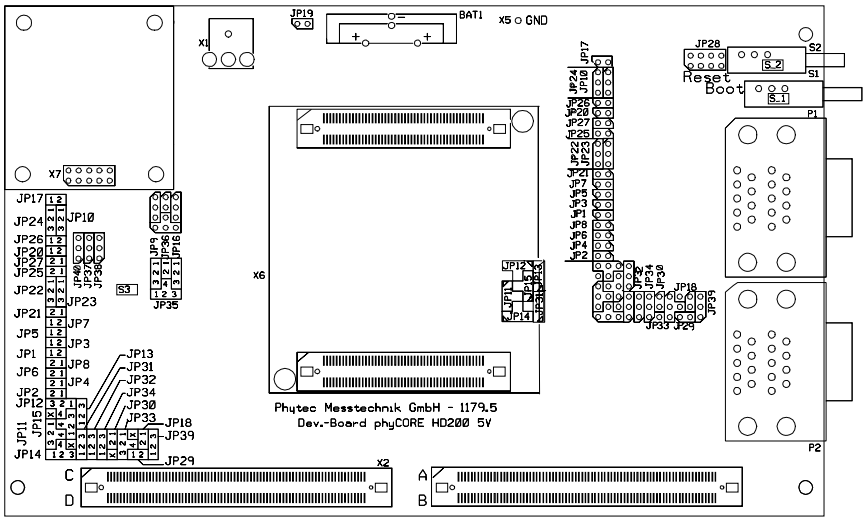


Figure 13: Location of the Jumpers (View of the Component Side)

Figure 14 shows the factory default jumper settings for operation of the phyCORE Development Board HD200 with the standard phyCORE-MPC5200B tiny (standard = MPC5200B controller, use of first and second RS-232, both CAN interfaces and LED D3 on the Development Board). Jumper settings for other functional configurations of the phyCORE-MPC5200B tiny module mounted on the Development Board are described in *section 13.3*.

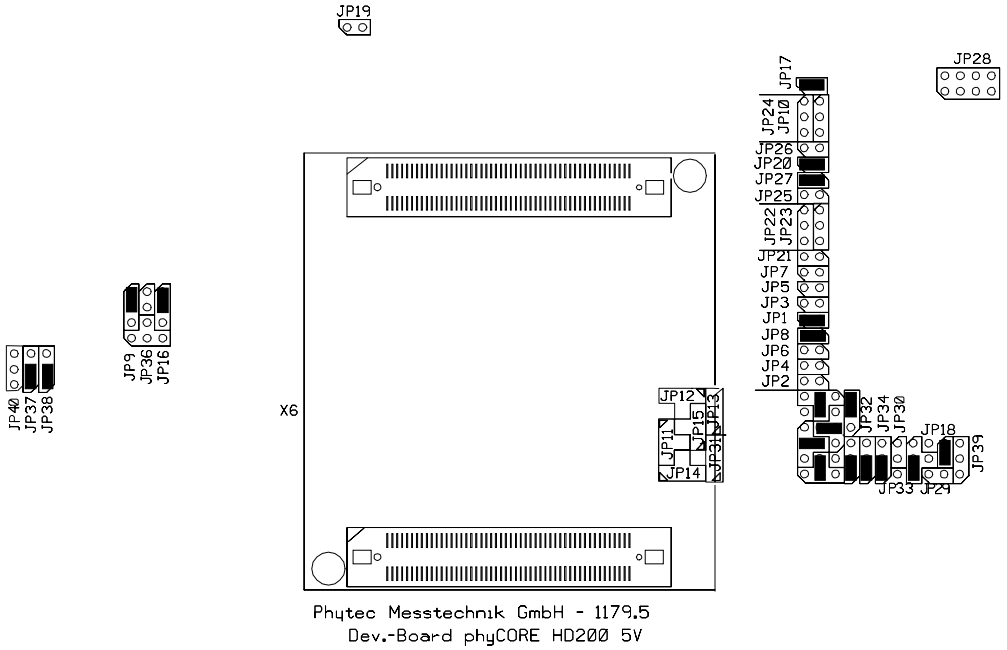


Figure 14: Default Jumper Settings of the phyCORE Development Board HD200 with phyCORE-MPC5200B tiny

13.2.3 Unsupported Features and Improper Jumper Settings

The following table contains improper jumper settings for operation of the phyCORE-MPC5200B tiny on a phyCORE Development Board HD200. Functions configured by these settings are not supported by the phyCORE module.

No RS-485 interface:

DB-9 plug P2B on the Development Board can be configured as RS-485 interface as an alternative to the second CAN interface. The phyCORE-MPC5200B tiny does not support an RS-485 interface. For this reason the corresponding jumper settings must never be used.

Jumper	Setting	Description
JP30	closed	TxD signal for second serial interface routed to pin 8 on the DB-9 plug P2B
JP33	1 + 2	RxD signal for second serial interface routed to pin 2 on the DB-9 plug P2B

Table 12: Improper Jumper Setting for JP30/33 on the Development Board

No Boot-input:

Jumper JP28 can connect the Boot//Boot signal directly to VCC (3.3 V). Since the phyCORE-MPC5200B tiny has a 2.5 V based I/O pin GPIO6 at the corresponding phyCORE-connector this jumper setting must never be used.

Jumper	Setting	Description
JP28	4 + 6	2.5 V based GPIO6 connected permanently with VCC

Table 13: Improper Jumper Setting for JP28 on the Development Board

13.3 Functional Components on the phyCORE Development Board HD200

This section describes the functional components of the phyCORE Development Board HD200 supported by the phyCORE-MPC5200B tiny and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MPC5200B tiny module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 14* and enable alternative or additional functions on the phyCORE Development Board HD200 depending on user needs.

13.3.1 Power Supply at X1

Caution:
Only use the included power adapter to supply power to the Development Board! Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +/-5 V DC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MPC5200B tiny mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 1.2 A is recommended.

Jumper	Setting	Description
JP9	1 + 2	3.3 V primary main supply voltage to the phyCORE-MPC5200B tiny
JP16	1 + 2	3.3 V as secondary main supply voltage to the phyCORE-MPC5200B tiny

Table 14: JP9, JP16 Configuration of the Main Supply Voltages VCC / VCC2

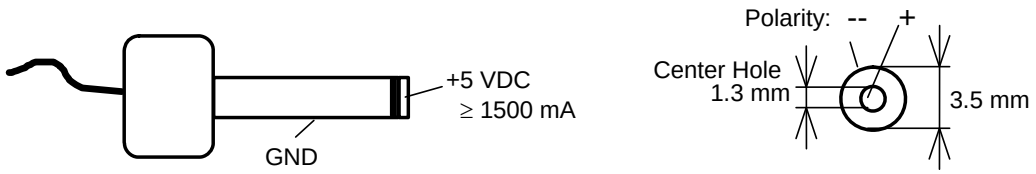


Figure 15: Connecting the Supply Voltage at X1

Caution:
When using this function, the following jumper settings are not allowed:

Jumper	Setting	Description
JP9	2 + 3	5 V as primary main supply voltage for the phyCORE-MPC5200B tiny
	open	phyCORE-MPC5200B tiny not connected to primary main supply voltage
JP16	2 + 3	5 V as secondary main supply voltage for the phyCORE-MPC5200B tiny
	open	phyCORE-MPC5200B tiny not connected to secondary main supply voltage

Table 15: JP9, JP16 Improper Jumper Settings for the Main Supply Voltages

Setting Jumper JP9 to position 2+3 configures a primary main power supply to the phyCORE-MPC5200B tiny of 5 V which could destroy the module. Setting Jumper JP16 to position 2+3 configures a secondary main power supply to the phyCORE-MPC5200B tiny of 5 V which also can damage the module. If Jumper JP9 and JP16 remain open, no primary and secondary main power supply is connected to the phyCORE-MPC5200B tiny. These jumper settings should therefore not be used.

13.3.2 First Serial Interface at Socket P1A

Socket P1A is the lower socket of the double DB-9 connector at P1. P1A is connected via jumpers to the serial interface PSC3 of the phyCORE-MPC5200B tiny.

Jumper	Setting	Description
JP20	closed	Pin 2 of DB-9 socket P1A connected with RS-232 signal TxD3-232 of the phyCORE-MPC5200B tiny
JP21	open	Pin 9 of DB-9 socket P1A not connected
JP22	open	Pin 7 of DB-9 socket P1A not connected
JP23	open	Pin 4 of DB-9 socket P1A not connected
JP24	open	Pin 6 of DB-9 socket P1A not connected
JP25	open	Pin 8 of DB-9 socket P1A not connected
JP26	open	Pin 1 of DB-9 socket P1A not connected
JP27	closed	Pin 3 of DB-9 socket P1A connected with RS-232 signal RxD3-232 from the phyCORE-MPC5200B tiny

Table 16: Jumper Configuration for the First RS-232 Interface

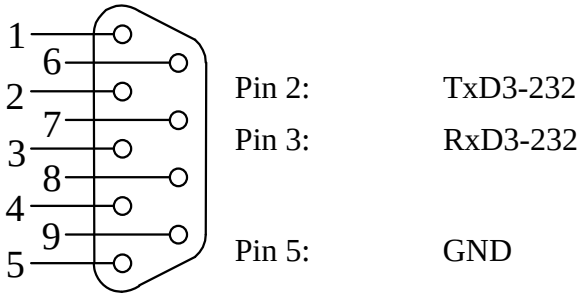


Figure 16: Pin Assignment of the DB-9 Socket P1A as RS-232 (PSC3) (Front View)

Caution:
When using the DB-9 socket P1A as RS-232 interface on the phyCORE-MPC5200B tiny the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP20	open	Pin 2 of DB-9 socket P1A not connected, no connection to TxD3-232 signal from phyCORE-MPC5200B tiny
JP21	closed	Pin 9 of DB-9 socket P1A connected with SPI_CLK from phyCORE-MPC5200B tiny
JP22	1 + 2	Pin 7 of DB-9 socket P1A connected with UART3_CTS_TTL from phyCORE-MPC5200B tiny
	2 + 3	Pin 7 of DB-9 socket P1A connected with reset input circuitry used on other phyCORE modules
JP23	1 + 2	Pin 4 of DB-9 socket P1A connected with SPI_MOSI signal from phyCORE-MPC5200B tiny
	2 + 3	Pin 4 of DB-9 socket P1A connected with bootstrap activation circuitry used on other phyCORE modules
JP24	1 + 2	Pin 6 of DB-9 socket P1A connected with SPI_MISO signal from phyCORE-MPC5200B tiny
	2 + 3	Pin 6 of DB-9 socket P1A connected with VOUT from Development Board HD200
JP25	closed	Pin 8 of DB-9 socket P1A connected with UART3_RTS_TTL from phyCORE-MPC5200B tiny
JP26	closed	Pin 1 of DB-9 socket P1A connected with SPI_SS from phyCORE-MPC5200B tiny
JP27	open	Pin 3 of DB-9 socket P1A not connected, no connection to RxD3-232 signal from phyCORE-MPC5200B tiny

Table 17: Improper Jumper Settings for DB-9 Socket P1A as First RS-232

If an RS-232 cable is connected to P1A, the voltage level on the RS-232 lines could destroy the phyCORE-MPC5200B tiny.

13.3.3 Optional Power Supply to External Devices via Socket P1A

The phyCORE Development Board HD200 can be populated by additional components that provide a supply voltage of 5 V at pin 6 of DB-9 socket P1A. This allows for easy and secure supply of external devices connected to P1A. This power supply option especially supports connectivity to analog and digital modems. Such modem devices enable global communication of the phyCORE-MPC5200B tiny over the Internet or a direct dial connection.

The following figure shows the location of these components on the Development Board:

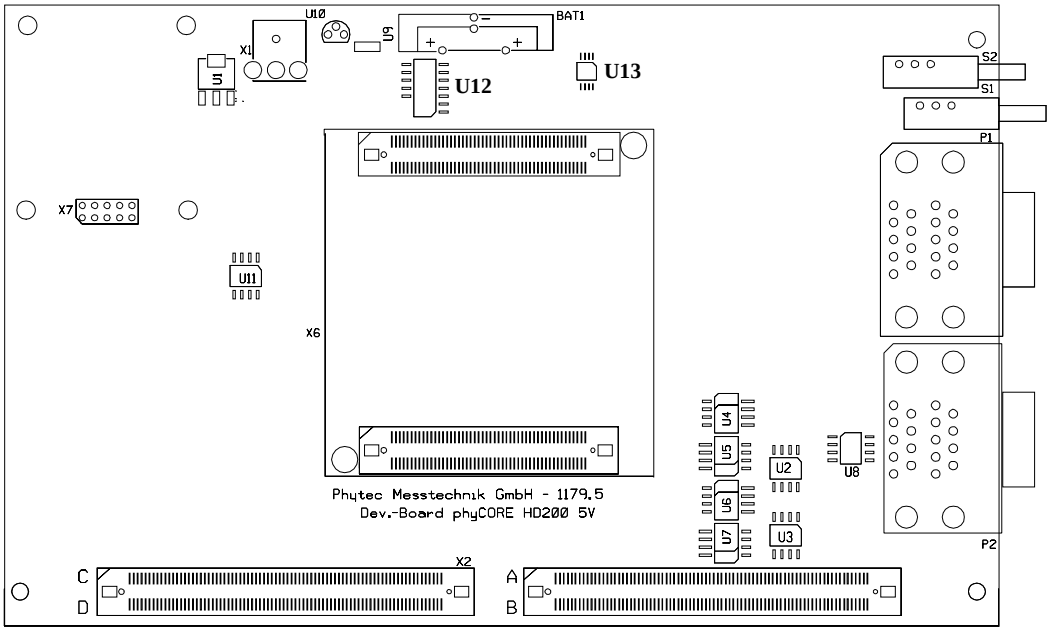


Figure 17: Location of Components at U12 and U13 for Power Supply to External Subassemblies

The components at U12 and U13 guarantee electronic protection against overvoltage and excessive current draw at pin 6 of P1A; in particular:

- Load detection and controlled voltage supply switch-on:

  In order to ensure clear detection of the switch-on condition, the connected device should cause a current draw of at least 10 mA at pin 6. The controlled voltage supply switch-on prevents voltage drop off on the phyCORE Development Board HD200.

- Overvoltage Protection:

  If the voltage at pin 6 exceeds the limiting value that can be provided by the phyCORE Development Board HD200, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board HD200 as well as connected modules and expansion boards.

- Overload Protection:

  If the current draw at pin 6 exceeds the limiting value of approximately 150 mA, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board HD200 and its power adapter caused by current overload.

This configuration option provides the following possibility:

Jumper	Setting	Description
JP24	2 + 3	Electronically protected 5 V at pin 6 for supply of external devices connected to P1A

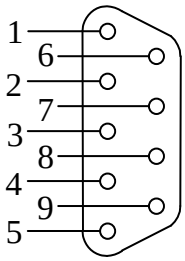
Table 18: JP24 Power Supply to External Devices Connected to P1A on the Development Board

13.3.4 Second Serial Interface at Socket P1B

Socket P1B is the upper socket of the double DB-9 connector at P1. P1B is connected via jumpers to the serial interface PSC6 of the phyCORE-MPC5200B tiny.

Jumper	Setting	Description
JP1	closed	Pin 2 of DB-9 socket P1B connected with RS-232 signal TxD6_RS232 of the phyCORE-MPC5200B tiny
JP2	open	Pin 9 of DB-9 socket P1B not connected
JP3	open	Pin 7 of DB-9 socket P1B not connected
JP4	open	Pin 4 of DB-9 socket P1B not connected
JP5	open	Pin 6 of DB-9 socket P1B not connected
JP6	open	Pin 8 of DB-9 socket P1B not connected
JP7	open	Pin 1 of DB-9 socket P1B not connected
JP8	closed	Pin 3 of DB-9 socket P1B connected with RS-232 signal RxD6_RS232 of the phyCORE-MPC5200B tiny

Table 19: Jumper Configuration of the DB-9 Socket P1B (PSC6)



Pin 2: TxD6_RS232
Pin 3: RxD6_RS232
Pin 5: GND

Figure 18: Pin Assignment of the DB-9 Socket P1B as Second RS-232 (Front View)

Caution:
When using the DB-9 socket P1B with the configuration of the phyCORE-MPC5200B tiny as described above the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP1	open	Pin 2 of DB-9 socket P1B not connected, no connection to TxD6_RS232 signal from phyCORE-MPC5200B tiny
JP2	closed	Pin 9 of DB-9 socket P1B connected with Timer4 from phyCORE-MPC5200B tiny
JP3	closed	Pin 7 of DB-9 socket P1B connected with UART6_CTS_TTL from phyCORE-MPC5200B tiny
JP4	closed	Pin 4 of DB-9 socket P1B connected with I2C2_CLK from phyCORE-MPC5200B tiny
JP5	closed	Pin 6 of DB-9 socket P1B connected with I2C2_IO signal from phyCORE-MPC5200B tiny
JP6	closed	Pin 8 of DB-9 socket P1B connected with port UART6_RTS_TTL from phyCORE-MPC5200B tiny
JP7	closed	Pin 1 of DB-9 socket P1B connected with Timer5 from phyCORE-MPC5200B tiny
JP8	open	Pin 3 of DB-9 socket P1B not connected, no connection to RxD6_232 signal from phyCORE-MPC5200B tiny

Table 20: Improper Jumper Settings for DB-9 Socket P1B (Second RS-232)

If an RS-232 cable is connected to P1B by mistake, the voltage level on the RS-232 lines could destroy the phyCORE-MPC5200B tiny.

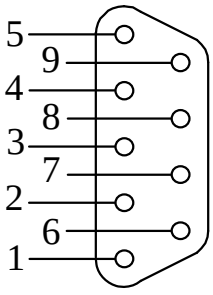
13.3.5 First CAN Interface at Plug P2A

Plug P2A is the lower plug of the double DB-9 connector at P2. P2A is connected to the first CAN interface (CAN1) of the phyCORE-MPC5200B tiny via jumpers. There are no CAN transceivers available on the phyCORE-MPC5200B tiny therefore the transceivers on the Development Board must be used. Depending on the configuration of the CAN transceivers and their power supply, the following two configurations are possible:

1. CAN signals generated by the Development Board CAN transceiver (U2) extend to connector P2A **w/o galvanic separation:**

Jumper	Setting	Description
JP31	1 + 2	Pin 2 of the DB-9 plug P2A is connected to CAN_L1 from transceiver on the Development Board HD200
JP32	1 + 2	Pin 7 of the DB-9 plug P2A is connected to CAN_H1 from transceiver on the Development Board HD200
JP11	2 + 4	Input at opto-coupler U4 on the phyCORE Development Board HD200 connected with CAN1_TX of the phyCORE-MPC5200B tiny
JP12	2 + 4	Output at opto-coupler U5 on the phyCORE Development Board HD200 connected with CAN1_RX of the phyCORE-MPC5200B tiny
JP13	2 + 3	CAN transceiver and opto-coupler on the Development Board connected with 5 V supply voltage
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 21: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board HD200



Pin 3: GND (Development Board Ground)
Pin 7: CAN_H1 (no galvanic separation)
Pin 2: CAN_L1 (no galvanic separation)
Pin 6: GND (Development Board Ground)

Figure 19: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board)

Caution:
When using the DB-9 connector P2A as CAN interface and the CAN transceiver on the Development Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of DB-9 plug P2A connected with CAN1_RX of the phyCORE-MPC5200B tiny
JP32	2 + 3	Pin 7 of DB-9 plug P2A connected with CAN1_TX of the phyCORE-MPC5200B tiny
JP11	1 + 2	Input at opto-coupler U4 on the Development Board is connected to SPI_MISO of the phyCORE-MPC5200B tiny
	2 + 3	Input at opto-coupler U4 on the Development Board is connected to EXT_AD30 of the phyCORE-MPC5200B tiny
	open	Input at opto-coupler U4 on the Development Board not connected
JP12	1 + 2	Output at opto-coupler U5 on the Development Board is connected to SPI_MOSI of the phyCORE-MPC5200B tiny
	2 + 3	Output at opto-coupler U5 on the Development Board is connected to EXT_AD29 of the phyCORE-MPC5200B tiny
	open	Output at opto-coupler U5 on the Development Board not connected
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 connector P2A
JP39	*see Table 24*	CAN bus supply voltage reduction for CAN circuitry

Table 22: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on the Development Board)

2. CAN signals generated by the CAN transceiver (U2) on the Development Board extend to connector P2A **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP31	1 + 2	Pin 2 of the DB-9 plug P2A is connected to CAN_L1 from transceiver on the Development Board HD200
JP32	1 + 2	Pin 7 of the DB-9 plug P2A is connected to CAN_H1 from transceiver on the Development Board HD200
JP11	2 + 4	Input at opto-coupler U4 on the phyCORE Development Board HD200 connected with CAN1_TX of the phyCORE-MPC5200B tiny
JP12	2 + 4	Output at opto-coupler U5 on the phyCORE Development Board HD200 connected with CAN1_RX of the phyCORE-MPC5200B tiny
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP18	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A
JP39	*see Table 24*	CAN bus supply voltage reduction for CAN circuitry

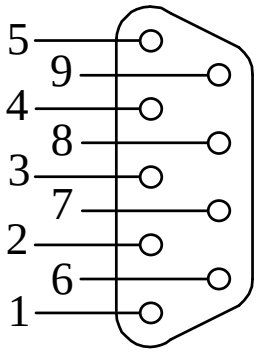
Table 23: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board with Galvanic Separation

CAN Bus Voltage Supply Reduction via JP39:

Depending on the voltage level that is supplied over the CAN bus at P2A or P2B (VCAN_IN1+) JP39 must be configured in order to routed the applicable voltage to the CAN voltage regulator at U8 on the Development Board:

VCAN_IN+	**JP39**
7 V..18 V	1 + 2
18 V..23 V	2 + 3
23 V..28 V	open

Table 24: JP39 CAN Bus Voltage Supply Reduction



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN_H1 (galvanic separation)
Pin 2: CAN_L1 (galvanic separation)
Pin 6: VCAN-

Figure 20: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

Caution:
When using the DB-9 plug P2A as CAN interface and the CAN transceiver on the Development Board with galvanic separation the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of DB-9 plug P2A connected with CAN1_RX of the phyCORE-MPC5200B tiny
JP32	2 + 3	Pin 7 of DB-9 plug P2A connected with CAN1_TX of the phyCORE-MPC5200B tiny
JP11	1 + 2	Input at opto-coupler U4 on the Development Board is connected to SPI_MISO of the phyCORE-MPC5200B tiny
	2 + 3	Input at opto-coupler U4 on the Development Board is connected to EXT_AD30 of the phyCORE-MPC5200B tiny
	open	Input at opto-coupler U4 on the Development Board not connected
JP12	1 + 2	Output at opto-coupler U5 on the Development Board is connected to SPI_MOSI of the phyCORE-MPC5200B tiny
	2 + 3	Output at opto-coupler U5 on the Development Board is connected to EXT_AD29 of the phyCORE-MPC5200B tiny
	open	Output at opto-coupler U5 on the Development Board not connected
JP13	2 + 3	Supply voltage for CAN transceiver and opto-coupler derived from local supply circuitry on the phyCORE Development Board HD200
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	see *Table 24*	Incorrect CAN bus supply voltage reduction for CAN circuitry

Table 25: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

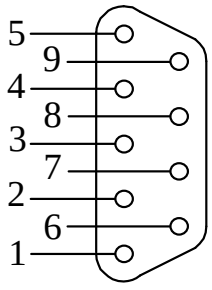
13.3.6 Second CAN Interface at Plug P2B

Plug P2B is the upper plug of the double DB-9 connector at P2. P2B is connected to the second CAN interface (CAN2) of the phyCORE-MPC5200B tiny via jumpers. There are no CAN transceivers available on the phyCORE-MPC5200B tiny therefore the transceivers on the Development Board must be used. Depending on the configuration of the CAN transceivers and their power supply, the following two configurations are possible:

1. CAN signals generated by the Development Board CAN transceiver (U3) extend to connector P2B **w/o galvanic separation:**

Jumper	Setting	Description
JP33	2 + 3	Pin 2 of the DB-9 plug P2B is connected to CAN_L2 of CAN transceiver U3 of the Development Board HD200
JP34	1 + 2	Pin 7 of the DB-9 plug P2B is connected to CAN_H2 of CAN transceiver U3 of the Development Board HD200
JP14	2 + 4	Input at opto-coupler U6 on the Development Board connected to CAN2_TX of the phyCORE-MPC5200B tiny
JP15	2 + 4	Output at opto-coupler U7 on the Development Board connected to CAN2_RX of the phyCORE-MPC5200B tiny
JP13	2 + 3	CAN transceiver and opto-coupler on the Development Board connected with 5 V supply voltage
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 26: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board HD200



Pin 3: GND (Development Board Ground)
Pin 7: CAN_H2 (no galvanic separation)
Pin 2: CAN_L2 (no galvanic separation)
Pin 6: GND (Development Board Ground)

Figure 21: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board)

Caution:
When using the DB-9 connector P2B as second CAN interface and the CAN transceiver on the Development Board the following jumper settings are not functional and could damage the module:

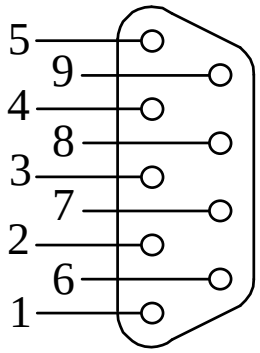
Jumper	Setting	Description
JP30	closed	Pin 8 at P2B is connected with TXD6-232 from the phyCORE-MPC5200B tiny
JP33	1 + 2	Pin 2 at P2B is connected with RxD6-232 from the phyCORE-MPC5200B tiny
	2 + 4	Pin 2 at P2B is connected with CAN2_RX from the on-board CAN transceiver on the phyCORE-MPC5200B tiny
JP34	2 + 3	Pin 7 at P2B is connected with CAN2_TX from the on-board CAN transceiver on the phyCORE-MPC5200B tiny
JP14	1 + 2	Input at opto-coupler U6 on the Development Board is connected to SPI_SS of the phyCORE-MPC5200B tiny
	2 + 3	Input at opto-coupler U6 on the Development Board is connected to EXT_AD31 of the phyCORE-MPC5200B tiny
	open	Input at opto-coupler U6 on the Development Board not connected
JP15	1 + 2	Output at opto-coupler U7 on the Development Board is connected to SPI_CLK of the phyCORE-MPC5200B tiny
	2 + 3	Output at opto-coupler U7 on the Development Board is connected to EXT_AD28 of the phyCORE-MPC5200B tiny
	open	Output at opto-coupler U7 on the Development Board not connected
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 connector P2A
JP39	see *Table 24*	CAN bus supply voltage reduction for CAN circuitry

Table 27: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on the Development Board)

2. CAN signals generated by the CAN transceiver (U3) on the Development Board extend to connector P2B **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP33	2 + 3	Pin 2 of the DB-9 plug P2B is connected to CAN_L2 of CAN transceiver U3 of the Development Board HD200
JP34	1 + 2	Pin 7 of the DB-9 plug P2B is connected to CAN_H2 of CAN transceiver U3 of the Development Board HD200
JP14	2 + 4	Input at opto-coupler U6 on the Development Board connected to CAN2_TX of the phyCORE-MPC5200B tiny
JP15	2 + 4	Output at opto-coupler U7 on the Development Board connected to CAN2_RX of the phyCORE-MPC5200B tiny
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP18	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A
JP39	*see Table 24*	CAN bus supply voltage reduction for CAN circuitry

Table 28: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board with Galvanic Separation



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN-H2 (galvanic separation)
Pin 2: CAN-L2 (galvanic separation)
Pin 6: VCAN-

Figure 22: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

Caution:
When using the DB-9 plug P2B as second CAN interface and the CAN transceiver on the Development Board with galvanic separation the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP30	closed	Pin 8 at P2B is connected with TXD6-232 from the phyCORE-MPC5200B tiny
JP33	1 + 2	Pin 2 at P2B is connected with RxD6-232 from the phyCORE-MPC5200B tiny
	2 + 4	Pin 2 at P2B is connected with CAN2_RX from the on-board CAN transceiver on the phyCORE-MPC5200B tiny
JP34	2 + 3	Pin 7 at P2B is connected with CAN2_TX from the on-board CAN transceiver on the phyCORE-MPC5200B tiny
JP14	1 + 2	Input at opto-coupler U6 on the Development Board is connected to SPI_SS of the phyCORE-MPC5200B tiny
	2 + 3	Input at opto-coupler U6 on the Development Board is connected to EXT_AD31 of the phyCORE-MPC5200B tiny
	open	Input at opto-coupler U6 on the Development Board not connected
JP15	1 + 2	Output at opto-coupler U7 on the Development Board is connected to SPI_CLK of the phyCORE-MPC5200B tiny
	2 + 3	Output at opto-coupler U7 on the Development Board is connected to EXT_AD28 of the phyCORE-MPC5200B tiny
	open	Output at opto-coupler U7 on the Development Board not connected
JP13	2 + 3	Supply voltage for CAN transceiver and opto-coupler derived from local supply circuitry on the phyCORE Development Board HD200
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	*see Table 24*	Incorrect CAN bus supply voltage reduction for CAN circuitry

Table 29: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

13.3.7 Programmable LED D3

The phyCORE Development Board HD200 offers a programmable LED at D3 for user implementations. This LED can be connected to port pin Gpio_Wkup_7 (Ball C12) of the MPC5200B CPU. A low-level at port pin Gpio_Wkup_7 causes the LED to illuminate, LED D3 remains off when writing a high-level.

Jumper	Setting	Description
JP17	closed	Port pin Gpio_Wkup_7 of the MPC5200B controls LED D3 on the Development Board

Table 30: JP17 Configuration of the Programmable LED D3

13.3.8 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 13.1*, all signals from the phyCORE-MPC5200B tiny extend in a strict 1:1 assignment to the Expansion Bus connector X2 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Development Board at X2.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X2 on the Development Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

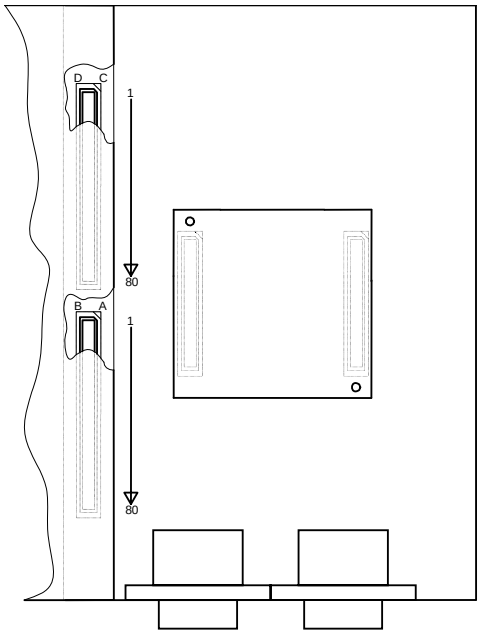


Figure 23: Pin Assignment Scheme of the Expansion Bus

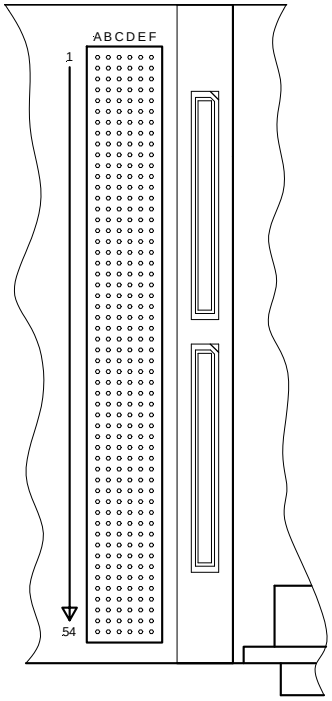


Figure 24: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MPC5200B tiny, in conjunction with the Expansion Bus (X2) on the Development Board and the patch field on an expansion board, is as follows:

Signal	phyCORE Module	Expansion Bus	Patch Field
Ext_AD0	8B	8B	30B
Ext_AD1	9A	9A	30D
Ext_AD2	10A	10A	30F
Ext_AD3	10B	10B	31A
Ext_AD4	11A	11A	31E
Ext_AD5	11B	11B	31B
Ext_AD6	12B	12B	31F
Ext_AD7	13A	13A	32A
Ext_AD8	13B	13B	32C
Ext_AD9	14A	14A	32E
Ext_AD10	15A	15A	32B
Ext_AD11	15B	15B	32F
Ext_AD12	16A	16A	33A
Ext_AD13	16B	16B	33C
Ext_AD14	17B	17B	33E
Ext_AD15	18A	18A	33B
Ext_AD16	18B	18B	33F
Ext_AD17	19A	19A	34A
Ext_AD18	20A	20A	34E
Ext_AD19	20B	20B	34B
Ext_AD20	21A	21A	34D
Ext_AD21	21B	21B	34F
Ext_AD22	22B	22B	35A
Ext_AD23	23A	23A	35E
Ext_AD24	23B	23B	35B
Ext_AD25	24A	24A	35D
Ext_AD26	25A	25A	35F
Ext_AD27	25B	25B	36A
Ext_AD28	26A	26A	36E
Ext_AD29	26B	26B	36B
Ext_AD30	27B	27B	36F
Ext_AD31	28A	28A	37A

Table 31: Pin Assignment Data/Address Bus for the phyCORE-MPC5200B tiny / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/LP_CS1	5A	5A	29E
/LP_CS2	5B	5B	29B
/LP_CS3	6B	6B	29F
/LP_Cs4	30A	30A	37B
/LP_Cs5	30B	30B	37F
/LP_Cs6	31A	31A	38A
/LP_Cs7	31B	31B	38C
/LP_Ts	29A	29A	37E
LP_Ack	28B	28B	37C
/LP_Ale	6A	6A	29D
/LP_Oe	7B	7B	30A
LP_RD/WR	8A	8A	30E

Table 32: Pin Assignment Dedicated LocalPlus Control Signals phyCORE-MPC5200B tiny / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/Pci_Reset	40A	40A	40F
Pci_Clock	40B	40B	41A
/Pci_Gnt	41A	41A	41E
/Pci_Req	42B	42B	41F
/Pci_Cbe_3	43A	43A	42A
Pci_Idsel	43B	43B	42C
/Pci_Cbe_2	44A	44A	42E
/Pci_Irdy	45A	45A	42B
/Pci_Frame	45B	45B	42F
/Pci_Devsel	46A	46A	43A
/Pci_Trdy	46B	46B	43C
/Pci_Stop	47B	47B	43E
/Pci_Perr	48A	48A	43B
Pci_Par	48B	48B	43F
/Pci_Serr	49A	49A	44A
/Pci_Cbe_1	50A	50A	44E
/Pci_Cbe_0	50B	50B	44B

Table 33: Pin Assignment PCI dedicated signals phyCORE-MPC5200B tiny / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
ATA_Isolation	37B	37B	40A
/ATA_Ior	38A	38A	40E
/ATA_Dack	38B	38B	40B
ATA_intrq	39A	39A	40D
ATA_Cs1	35A	35A	39E
ATA_Drq	35B	35B	39B
ATA_Cs0	34A	34A	39A
ATA_Iochrdy	36A	36A	39D
/ATA_Iow	36B	36B	39F

Table 34: Pin Assignment Dedicated ATA /IDE Interface Signals phyCORE-MPC5200B tiny / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
AC97_1_Sdata_In	16C	16C	5F
AC97_1_Sdata_O	15D	15D	5B
AC97_1_Res	13C	13C	4F
AC97_1_Sync	14C	14C	5C
AC97_1_Bitclk	15C	15C	5E
TXD6-232	23C	23C	8A
RXD6-232	21C	21C	7B
UART6_TXD_TTL	20C	20C	7A
UART6_RXD_TTL	19C	19C	6F
UART6_RTS_TTL	24C	24C	8B
UART6_CTS_TTL	25C	25C	8D
RXD3-232	22D	22D	7F
TXD3-232	23D	23D	8E
UART3_TXD_TTL	17D	17D	6C
UART3_RXD_TTL	16D	16D	6A
UART3_RTS_TTL	25D	25D	8F
UART3_CTS_TTL	26D	26D	9E
CAN1_TX	21D	21D	7D
CAN1_RX	20D	20D	7E
CAN2_TX	18C	18C	6E
CAN2_RX	18D	18D	6B
I2C1_Clk	31C	31C	10F
I2C1_Io	32D	32D	11C
I2C2_Clk	26C	26C	9A
I2C2_Io	28C	28C	9F
SPI_Mosi	27D	27D	9B
SPI_Miso	28D	28D	10A

Signal	phyCORE Module	Expansion Bus	Patch Field
SPI_Clk	30D	30D	10B
SPI_Ss	31D	31D	11A
ETH_RX-	35C	35C	12A
ETH_RX+	35D	35D	12E
ETH_TX-	36C	36C	12B
ETH_TX+	36D	36D	12D
/ETH_INT	37D	37D	12F
ETH_LINK	33C	33C	11E
ETH_SPEED	34C	34C	11F
/ETH_PD	38C	38C	13A
USB1_Oe	50C	50C	17A
USB1_TXP	50D	50D	17E
USB1_TXN	49C	49C	16F
USB1_RXD	47D	47D	16C
USB1_RXP	48D	48D	16B
USB1_RXN	48C	48C	16E
USB1_Suspend	46C	46C	15F
USB1_PortPwr	45D	45D	15B
USB1_Overcnt	45C	45C	15E
USB1_Speed	46D	46D	16A

Table 35: Pin Assignment Interfaces for the phyCORE-MPC5200B tiny / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
CPU_TCK	38D	38D	12E
/COP_TRST	39C	39C	13B
CPU_TDI	40D	40D	13F
CPU_TDO	41D	41D	14E
CPU_TMS	42D	42D	14B
CK_STOP	40C	40C	13D

Table 36: Pin Assignment COP Interface Signals for the phyCORE-MPC5200B tiny /Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/IRQ_0	4A	4A	29A
/IRQ_1	2B	2B	28E
/IRQ_2	3B	3B	28F
/IRQ_3	3A	3A	28B
Timer2	12D	12D	4B
Timer3	13D	13D	5A
Timer4	29C	29C	10C
Timer5	30C	30C	10E
Timer6	44C	44C	15C
Timer7	43D	43D	15A
/RESIN	10D	10D	3F
/HReset	11C	11C	4E
/SReset	10C	10C	3D
RESOUT	7D	7D	2F
GPIO6	9C	9C	3B
GPIO7	11D	11D	4A
RTC_CLKOUT	1B	1B	28C
/IRQRTC	33D	33D	11B
FL_VPEN	41C	41C	14A
PSC2_4	43C	43C	14F
ETH_TXD3	33A	33A	38B
ETH_TXD1	8C	8C	3E
ETH_RXD1	33B	33B	38F
Test_Sel_1	32B	32B	38E
ETH_NWAYEN	41C	41C	14A
/PHYReset	8D	8D	3A

Table 37: Pin Assignment Misc. Control Signals for the phyCORE-MPC5200B tiny /Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
3V3	1C, 2C, 4C, 5C, 1D, 2D	1C, 2C, 4C, 5C, 1D, 2D	1A, 1C, 2A, 1B
VCC_SRAM	6D	6D	2D
VBAT	6C	6C	2B
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 41B, 44B, 49B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 52D, 57D, 62D, 67D, 72D, 77D	3C, 4C, 7C, 8C, 9C, 12C, 13C, 14C, 17C, 18C, 19C, 22C, 23C, 24C, 27C, 29C, 30C, 31C, 34C, 35C, 36C, 39C, 40C, 41C, 44C, 45C, 46C, 49C, 50C, 51C, 54C, 4D, 5D, 6D, 9D, 10D, 11D, 14D, 15D, 16D, 9D, 20D, 21D, 24D, 25D, 26D, 28D, 31D, 32D, 33D, 36D, 37D, 38D, 41D, 42D, 43D, 46D, 47D, 48D, 51D, 52D, 53D, 1E, 2E, 1F

Table 38: Pin Assignment Power Supply for the phyCORE-MPC5200B tiny / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
NC	1A, 4D, 5D	50A, 51A, 53A, 54A, 55A, 56A, 58A, 59A, 60A, 61A, 63A, 64A, 65A, 66A, 68A, 69A, 70A, 71A, 73A, 74A, 75A, 76A, 78A, 79A, 80A 51B, 53B, 54B, 55B, 56B, 58B, 59B, 60B, 61B, 63B, 64B, 65B, 66B, 68B, 69B, 70B, 71B, 73B, 74B, 75B, 76B, 78B, 79B, 80B 51C, 53C, 54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C, 73C, 74C, 75C, 76C, 78C, 79C, 80C 4D, 5D, 7D, 8D, 51D, 53D, 54D, 55D, 56D, 58D, 59D, 60D, 61D, 63D, 64D, 65D, 66D, 68D, 69D, 70D, 71D, 73D, 74D, 75D, 76D, 78D, 79D, 80D	18A, 19A, 20A, 21A, 22A, 23A 24A, 25A, 26A, 27A, 45A, 46A, 47A, 48A, 49A, 50A, 51A, 52A, 53A, 54A 17B, 18B, 19B, 20B, 21B, 22B, 23B, 24B, 25B, 26B, 27B, 45B, 46B, 47B, 48B, 49B, 50B, 51B, 52B, 53B, 54B 20C, 21C, 25C, 26C, 47C, 48C, 52C, 53C 17D, 18D, 22D, 23D, 27D, 44D 45D, 49D, 50D, 54D 18E, 19E, 20E, 21E, 22E, 23E, 24E, 25E, 26E, 27E, 45E, 46E, 47E, 48E, 49E, 50E, 51E, 52E, 53E, 54E 17F, 18F, 19F, 20F, 21F, 22F, 23F, 24F, 25F, 26F, 27F, 44F, 45F, 46F, 47F, 48F, 49F, 50F, 51F, 52F, 53F, 54F

Table 39: Unused Pins on the phyCORE-MPC5200B tiny / Development Board / Expansion Board

13.3.9 Battery Connector BAT1

The mounting space BAT1 (*see PCB stencil*) is provided for connection of a battery that buffers the RTC on the phyCORE-MPC5200B tiny. In the event of a VCC operating voltage failure the RTC is automatically supplied with power from the connected battery. The optional battery required for the RTC buffering is available through PHYTEC (order code BL-011).

13.3.10 DS2401 Silicon Serial Number

Communication to a DS2401 Silicon Serial Number can be implemented in various software applications for the definition of a node address or as copy protection in networked applications. The DS2401 can be soldered on space U10 or U9 on the Development Board, depending on the type of device packaging being used.

The Silicon Serial Number Chip mounted on the phyCORE Development Board HD200 can be connected to port Timer2 of the phyCORE-MPC5200B tiny available at GPIO1 (JP19 = closed).

Jumper	Setting	Description
JP19	closed	Port Timer2 (GPIO1) of the MPC5200B is used to access the Silicon Serial Number

Table 40: JP19 Jumper Configuration for Silicon Serial Number Chip

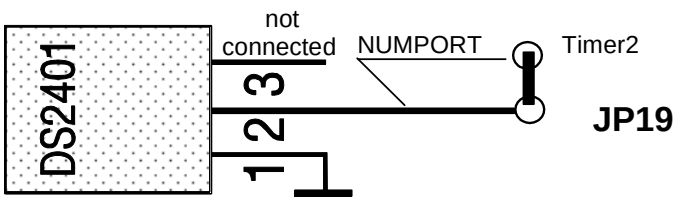


Figure 25: Connecting the DS2401 Silicon Serial Number

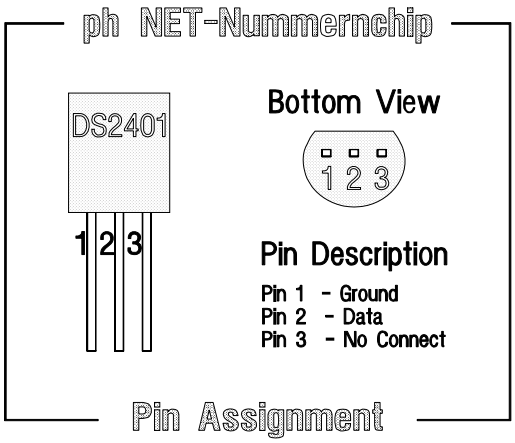


Figure 26: Pin Assignment of the DS2401 Silicon Serial Number

13.3.11Pin Header Connector X4

The pin header X4 on the Development Board enables connection of an optional modem power supply. Connector X4 supplies 5 V = at pin 1 and provides the phyCORE Development Board HD200 GND potential at pin 2. The maximum current draw depends on the power adapter used. We recommend the use of modems with less than 250 mA current draw.

14 Ethernet Port

The phyCORE Development Board HD200 provides a 10-pin header connector at X7 for mounting the PHYTEC Ethernet transformer module. The optional add-on module is available through PHYTEC (order code EAD-003-MPC5200). This allows for direct connection of the phyCORE-MPC5200B tiny mounted on a Development Board HD200 to a 10/100Base-T network.

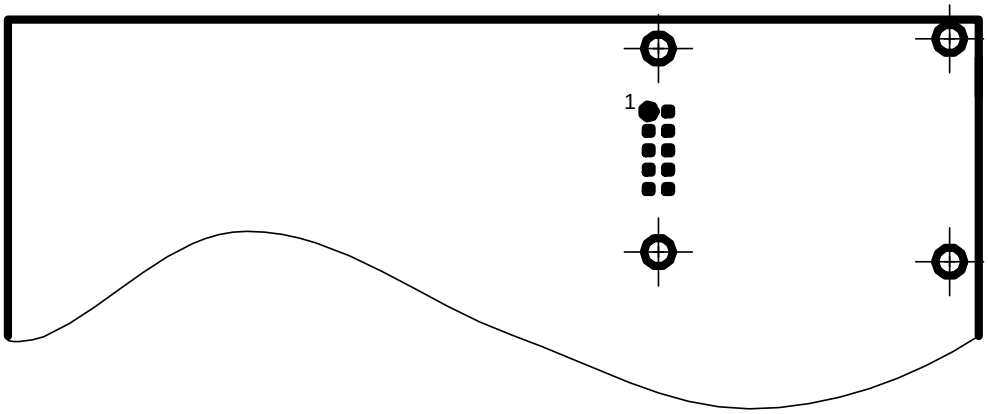


Figure 27: Ethernet Transformer Module Connector

The pinout for the Ethernet transformer connector is shown below:

Pin#	Function	Note
1	ETH_LanLED	Make sure JP37 on the Development Board is closed at position 1+2.
2	ETH_LinkLED	Make sure JP38 on the Development Board is closed at position 1+2.
3	VCC	
4	ETH_TxD+	
5	ETH_TxD-	
6	GND	
7	ETH_RxD+	
8	ETH_RxD-	
9	GND	
10	VCC	

Table 41: Ethernet Transformer Connector Pinout

15 Revision History

Date	Version numbers	Changes in this manual
18-Jan-2006	Manual L-678e_0 PCM-030 PCB# 1245.0 PCM-997-V2 PCB# 1179.5/6	First draft, Preliminary documentation. phyCORE-MPC5200B tiny in "Prototype" state
05-Sep-2006	Manual L-678e_1 PCM-030 PCB# 1245.1 PCM-997-V2 PCB# 1179.5	Second draft, Preliminary documentation. phyCORE-MPC5200B tiny in "Prototype" state New Ethernet signals added. New U-Boot section started, still under construction.
06-Dec-2006	Manual L-678e_2 PCM-030 PCB# 1245.1 PCM-997-V2 PCB# 1179.5	First Release U-Boot section finished.

16 Component Placement Diagram

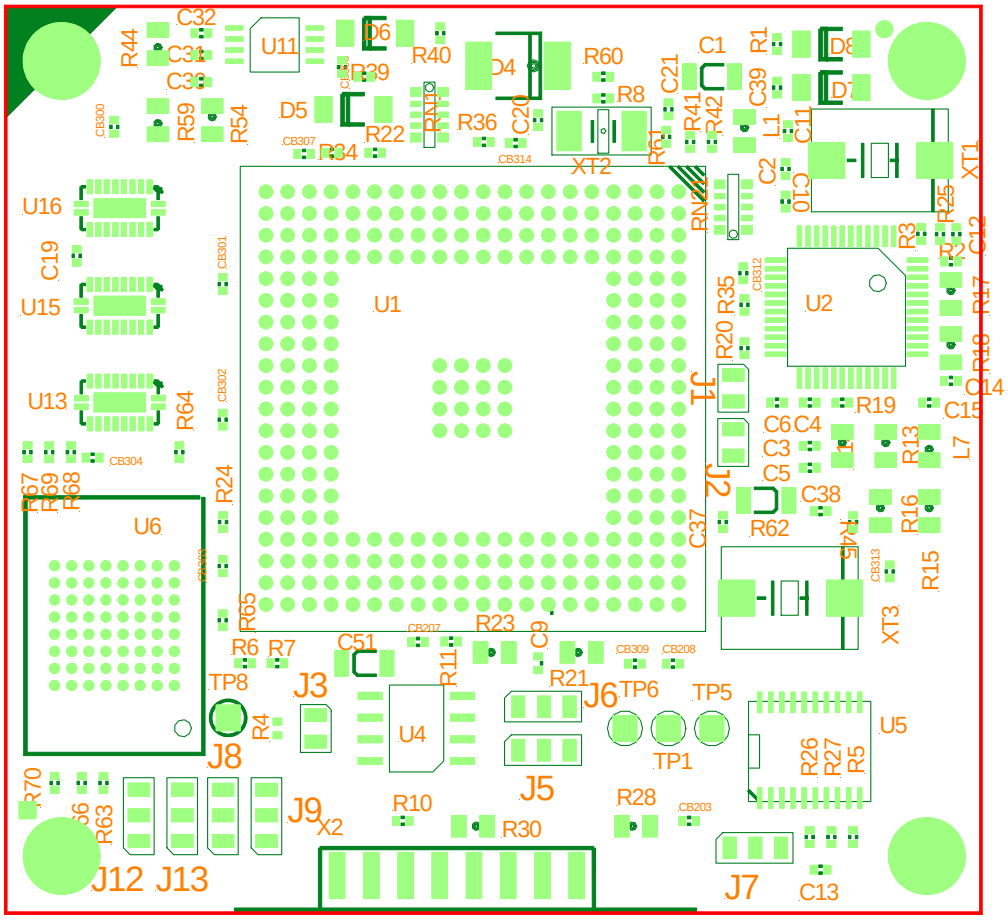


Figure 28: phyCORE-MPC5200B tiny Component Placement, Top View

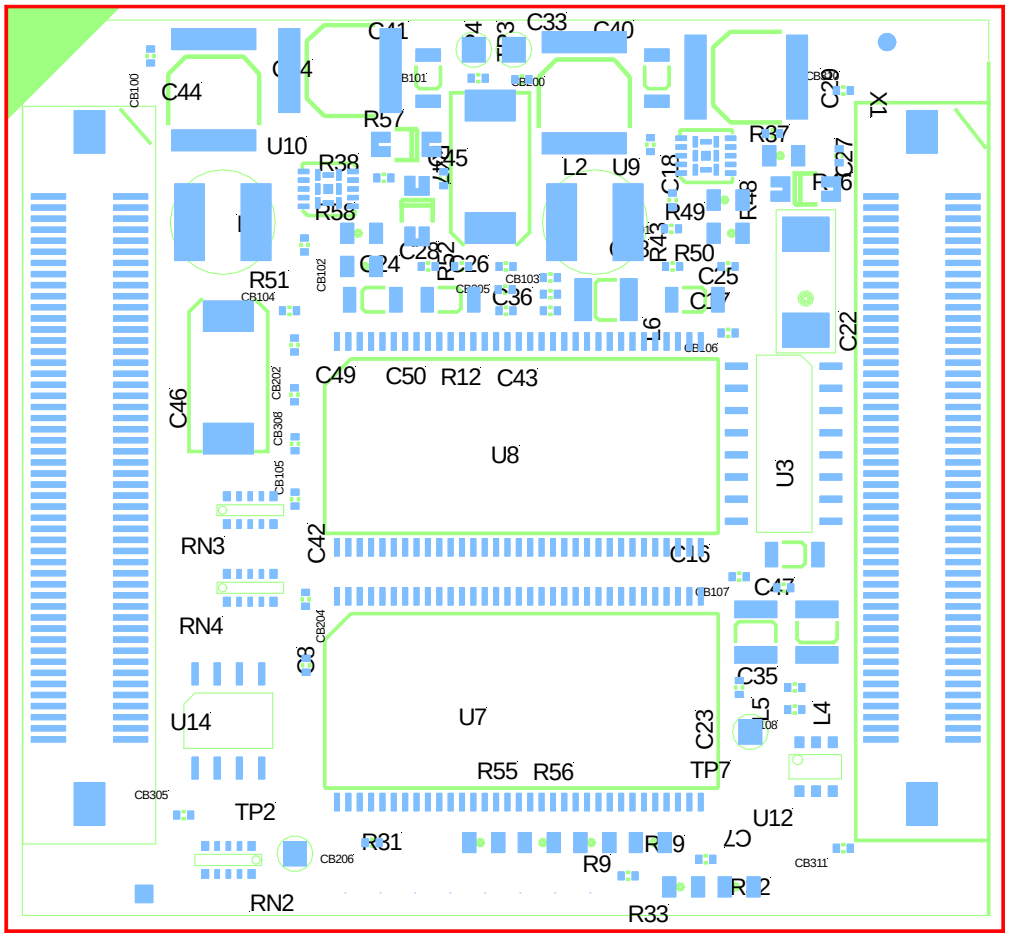


Figure 29: phyCORE-MPC5200B tiny Component Placement, Bottom View

Index

A Appendix

A.1 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Document: **phyCORE-MPC5200B tiny**
Document number: **L-678e_2, December 2006**

How would you improve this manual?

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Published by

PHYTEC

Order No. L-678e_2
Printed in Germany