phyCORE-MCF548x

Hardware Manual

Edition January 2005

A product of a PHYTEC Technology Holding company

In this manual are descriptions for copyrighted products that are not explicitly indicated as such. The absence of the trademark (™) and copyright (©) symbols does not imply that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual.

The information in this document has been carefully checked and is believed to be entirely reliable. However, PHYTEC Messtechnik GmbH assumes no responsibility for any inaccuracies. PHYTEC Messtechnik GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product. PHYTEC Messtechnik GmbH reserves the right to alter the information contained herein without prior notification and accepts no responsibility for any damages which might result.

Additionally, PHYTEC Messtechnik GmbH offers no guarantee nor accepts any liability for damages arising from the improper usage or improper installation of the hardware or software. PHYTEC Messtechnik GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

1st Edition: January 2005

Index of Figures

Index of Tables

Preface

This phyCORE-MCF548x Hardware Manual describes the board's design and functions. Precise specifications for the Freescale MCF548X microcontroller series can be found in the enclosed MCF548X microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal. The MSB and LSB of the data and address busses shown in the circuit diagram are based on the conventions of Freescale. Accordingly, D0 and A0 represent the LSB, while D31 and A31 represent the MSB. These conventions are also valid for the parallel I/O signals.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MCF548x

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MCF548x is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and selected 32-bit controllers on two types of Single Boards Computers:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MCF548x belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MCF548x is a subminiature (70 x 57 mm) insert-ready Single Board Computer populated with Freescale's ColdFire MCF548X microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MCF548X controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MCF548x.

The phyCORE-MCF548x offers the following features:

- Single Board Computer in subminiature form factor (70 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 160-pin Molex connectors
- processor: Freescale embedded ColdFire MCF548X (200 MHz clock)

Internal Features of the MCF548X:

- 32-bit ColdFire V4e core, 200 MHz CPU speed
- 32 kByte instruction cache
- 32 kByte data cache
- MMU with 32 entries
- 64-bit FPU double precision IEEE-754
- EMAC unit
- DMA unit
- Encryption unit
- 32 kByte SRAM
- Watchdog
- Two system timers
- Four 32-bit general purpose timers
- Four UARTs
- SPI interfaces
- Two CAN 2.0B interfaces
- I²C Maser/Slave controller
- Two Fast Ethernet controllers
- USB2.0 Slave
- PCI bus
- BDM test/debug port

Memory Configuration[1]:

- DDR SDRAM: 64 MByte to 128 MByte
- Flash: 32 MByte to 64 MByte Intel Strata Flash memory, 32-Bit memory width, synchronous (K3) or asynchronous (J3) devices are supported
- I^2C Memory: 4 kByte EEPROM (up to 32 kByte, alternatively I^2C FRAM, I^2C SRAM)

Other Board-Level Features:

- Four UART ports
  RS-232 interfaces (RxD/TxD/RTS/CTS) and two TTL-level interfaces
- Two CAN ports, on-board CAN transceivers; also configurable as TTL
- Two 10/100Mbit Ethernet ports
- Logic Device Lattice ispXPLD 5000 family
  256/512/768 Macrocells and 128/256/384 kBit SRAM, in-system-programmable
  For applications like:
  single-, dual-port RAM or FIFO
  Timer, PWM, CapComp etc.
  Decoder, Encoder
  IP core
  application-specific logic
  special bus interfaces
  multi-purpose I/O signals etc.
- PCI 2.2 bus
- SPI bus, Synchronous Serial Interface with two Chip Selects
- I^2C bus
- I^2C Real-Time Clock with calendar and alarm function
- 12-bit ADC, 8 channels, connected to I^2C Bus
- 12-bit DAC, 1 channel, connected to I^2C Bus
- JTAG/BDM test/debug port
- Industrial temperature range (-40…+85°C)

1: Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

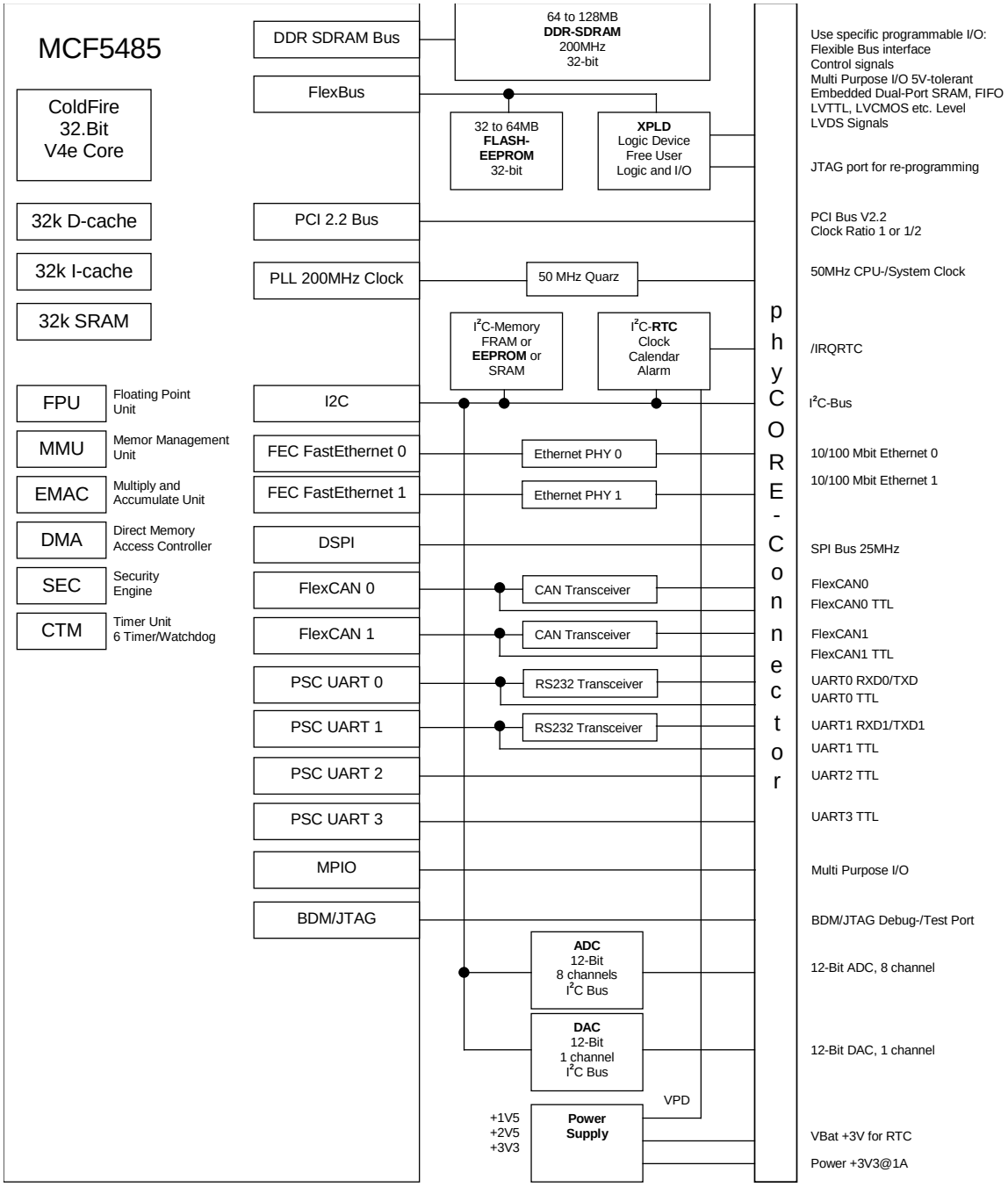

Figure 1: Block Diagram phyCORE-MCF548x

1.2 View of the phyCORE-MCF548x

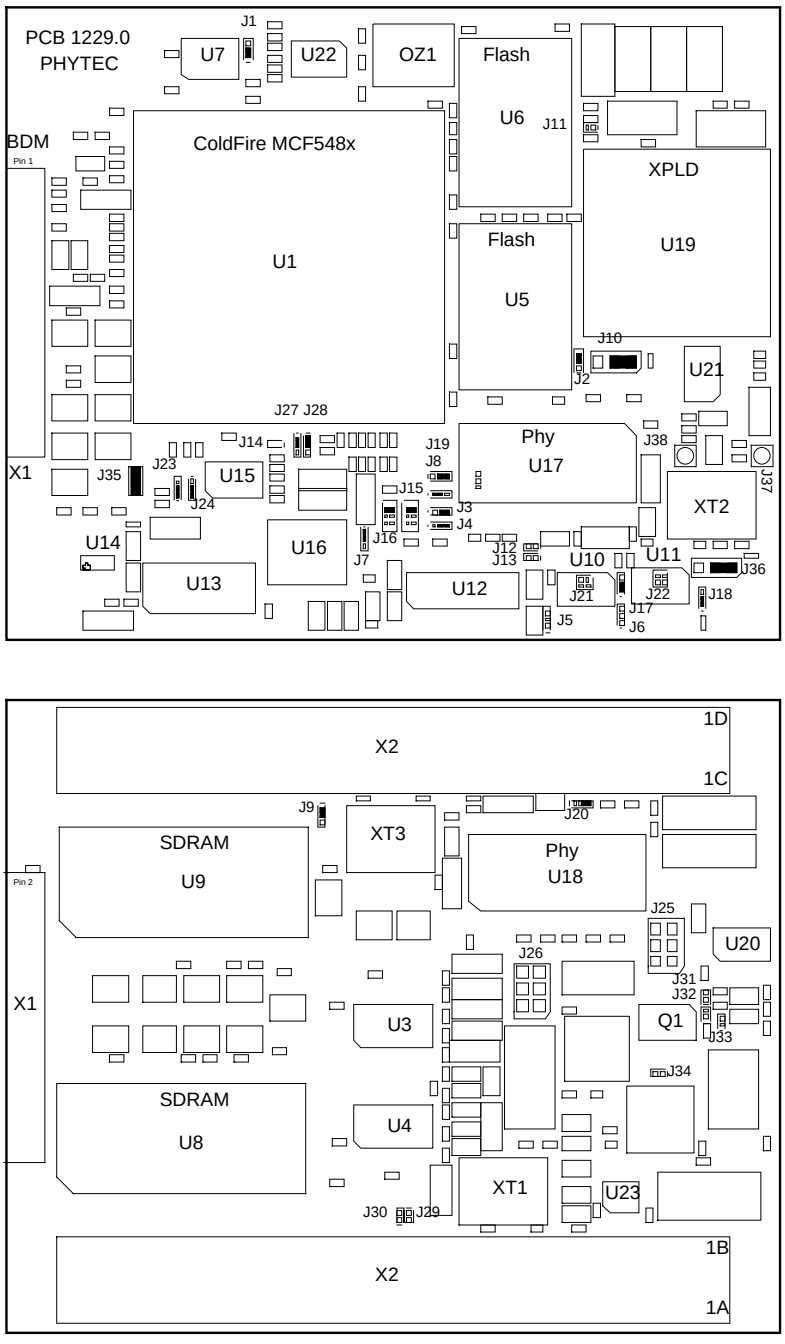

Figure 2: View of the phyCORE-MCF548x Revision 1229.0 (M 1.5:1)

1.3 Minimum Requirements to Operate the phyCORE-MCF548x

Basic operation of the phyCORE-MCF548x only requires supply of a +3V3 input voltage and the corresponding GND connection.

These supply pins are located at the phyCORE-connector X2:

+3V3	X2	1C, 2C, 1D, 2D, 4D, 5D
GND	X2	3C, 3D, 7C, 9D, 12C, 14D

Caution:
We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-MCF548x and at least the matching number of GND pins neighboring the +3V3 pins.

In addition, proper implementation of the phyCORE module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to section 4 for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector; *refer to section 11*). This allows the phyCORE-MCF548x to be plugged into any target application like a "big chip".

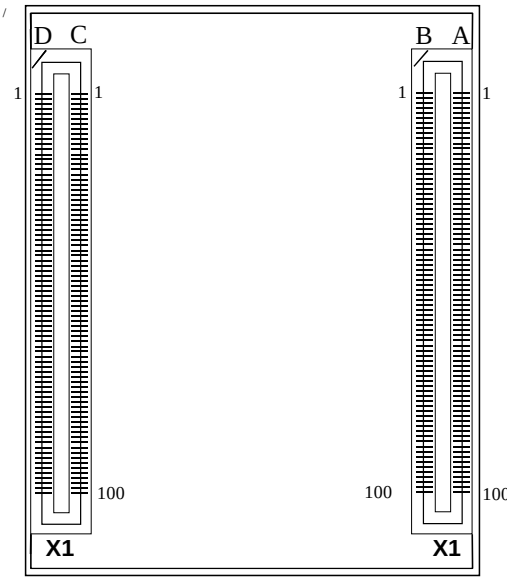

Figure 3: Pinout of the phyCORE-MCF548x (Bottom View)

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. Reset state means the behavior of the signal while the processor's reset input /RSTI is active.

Please refer to the Freescale MCF548x User Manual/Data Sheet for details on the functions and features of controller signals and port pins.

Pin Number	Signal	I/O	Comments
Pin Row X1A			
1A	EXTCLK	I	Clock input for GCLK3 of the XPLD 10 kOhm pull-down
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	/IRQ7	I I	Interrupt input 7 of the ColdFire processor. GPI PIRQ7 Reset state: GPI
4A	XPLD3_0	I/O	XPLD GPIO
5A	/FB_CS1	O I/O	Chip Select 1 of the ColdFire FlexBus. Reset state: high PFBCS1 GPIO

Pin Number	Signal	I/O	Comments
6A 8A 9A 10A 11A 13A 14A 15A 16A 18A 19A 20A 21A 23A 24A 25A 26A 28A 29A 30A 31A 33A 34A 35A 36A 38A 39A 40A	XPLD3_1 XPLD3_3 XPLD3_5 XPLD3_6 XPLD3_8 XPLD3_11 XPLD3_13 XPLD3_14 XPLD3_16 XPLD3_19 XPLD3_21 XPLD3_22 XPLD3_24 XPLD3_27 XPLD3_29 XPLD3_30 XPLD3_32 XPLD3_35 XPLD0_1 XPLD0_2 XPLD0_4 XPLD0_7 XPLD0_9 XPLD0_10 XPLD0_12 XPLD0_15 XPLD0_17 XPLD0_18		XPLD GPIO Freely available I/O pins to implement application-specific functionality.
41A	/FB_CS4	O I/O	Chip Select 4 of the ColdFire FlexBus. Reset state: high PFBCS4 GPIO
43A	/DACK0	O I/O O	DMA acknowledge 0 PDMA2 GPIO Reset state: GPI TOUT0 GP timer output 0
44A	/DACK1	O I/O O	DMA acknowledge 1 PDMA3 GPIO Reset state: GPI TOUT1 GP timer output 1
45A	/PCI_RESET	O	PCI reset Reset state: Low
46A	/PCI_BR0	I I/O I	PCI bus request 0 PPCIBR0 GPIO Reset state: GPI TIN0 GP timer input 0

Pin Number	Signal	I/O	Comments
48A	/PCI_BR1	I I/O I	PCI bus request 1 PPCIBR1 GPIO Reset state: GPI TIN1 general purpose timer input 1
49A	/PCI_BR2	I I/O I	PCI bus request 2 PPCIBR0 GPIO Reset state: GPI TIN2 general purpose timer input 2
50A	/PCI_BR3	I I/O I	PCI bus request 3 PPCIBR3 GPIO Reset state: GPI TIN3 general purpose timer input 3
51A	/PCI_BR4	I I/O 	PCI bus request 4 PPCIBR4 GPIO Reset state: GPI
		I	/IRQ4 interrupt input 4 of the ColdFire processor.
53A 54A 55A 56A 59A 60A 61A 63A 71A 73A 74A 75A 76A 78A 79A 80A	PCI_AD31 PCI_AD29 PCI_AD27 PCI_AD25 PCI_AD23 PCI_AD21 PCI_AD19 PCI_AD17 PCI_AD14 PCI_AD12 PCI_AD10 PCI_AD8 PCI_AD7 PCI_AD5 PCI_AD3 PCI_AD1	I/O O	PCI address/data bus Reset state: tristate Bootstrap configuration[1]: FBMODE=1 *Refer to A.1 for additional information.* FBADDRx FlexBus address lines
58A	/PCI_CXBE3	I/O	PCI command/byte enable signal 3 Reset state: tristate
64A	/PCI_CXBE2	I/O	PCI command/byte enable signal 2 Reset state: tristate
65A	/PCI_IRDY	I/O	PCI initiator ready signal Reset state: tristate
66A	/PCI_DEVSEL	I/O	PCI device select signal Reset state: tristate
68A	/PCI_PERR	I/O	PCI parity error signal Reset state: tristate
69A	/PCI_SERR	I/O	PCI system error signal Reset state: tristate
70°	/PCI_CXBE1	I/O	PCI command/byte enable signal 1 Reset state: tristate

[1] *Refer to Table 3 for additional information to the system's start-up configuration.*

Pin Number	Signal	I/O	Comments
Pin Row X1B			
1B	CLK_EXT	O	Reference clock output of the processor's input clock.
2B	/IRQ5	I I	Interrupt input 5 of the ColdFire processor. GPI PIRQ5 Reset state: GPI
3B	/IRQ6	I I	Interrupt input 6 of the ColdFire processor. GPI PIRQ6 Reset state: GPI
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND		Ground 0 V
5B	/FB_CS2	O I/O	Chip Select 2 of the ColdFire FlexBus. Reset state: high PFBCS2 GPIO
6B	/FB_CS3	O I/O	Chip Select 3 of the ColdFire FlexBus. Reset state: high PFBCS3 GPIO

Pin Number	Signal	I/O	Comments
7B 8B 10B 11B 12B 13B 15B 16B 17B 18B 20B 21B 22B 23B 25B 26B 27B 28B 30B 31B 32B 33B 35B 36B 37B 38B 40B	XPLD3_2 XPLD3_4 XPLD3_7 XPLD3_9 XPLD3_10 XPLD3_12 XPLD3_15 XPLD3_17 XPLD3_18 XPLD3_20 XPLD3_23 XPLD3_25 XPLD3_26 XPLD3_28 XPLD3_31 XPLD3_33 XPLD3_34 XPLD0_0 XPLD0_3 XPLD0_5 XPLD0_6 XPLD0_8 XPLD0_11 XPLD0_13 XPLD0_14 XPLD0_16 XPLD0_19	I/O	XPLD GPIO Free usable pins to implement application specific functionality.
41B	/FB_CS5	O I/O	Chip Select 5 of the ColdFire FlexBus. Reset state: high PFBCS5 GPIO
42B	/DREQ0	I I/O I	DMA request signal 0 of the processor. PDMA0 GPIO Reset state: GPI TIN1 GP timer input 1
43B	/DREQ1	I I/O I I	DMA request signal 1 of the processor. PDMA1 GPIO Reset state: GPI TIN0 GP timer input 0 /IRQ1 interrupt input 1
45B	CLK_PCI	O	PCI reference clock output supplied from the clock distribution device at U22.
46B	GND		Ground 0 V
47B	/PCI_BG0	O I/O O	PCI external bus grant signal 0. PPCIBG0 GPIO Reset state: GPI (PAR_PCIBG0) TOUT0 GP timer output 0

Pin Number	Signal	I/O	Comments
48B	/PCI_BG1	O I/O O	PCI external bus grant signal 1. PPCIBG1 GPIO Reset state: GPI (PAR_PCIBG1) TOUT1 GP timer output 1
50B	/PCI_BG2	O I/O O	PCI external bus grant signal 2. PPCIBG2 GPIO Reset state: GPI (PAR_PCIBG2) TOUT2 GP timer output 2
51B	/PCI_BG3	O I/O O	PCI external bus grant signal 3. PPCIBG3 GPIO Reset state: GPI (PAR_PCIBG3) TOUT3 GP timer output 3
52B	/PCI_BG4	O I/O O	PCI external bus grant signal 0. PPCIBG4 GPIO Reset state: GPI (PAR_PCIBG3) /TBST transfer burst signal of the FlexBus
53B 55B 56B 57B 60B 61B 62B 63B 70B 71B 72B 73B 76B 77B 78B 80B	PCI_AD30 PCI_AD28 PCI_AD26 PCI_AD24 PCI_AD22 PCI_AD20 PCI_AD18 PCI_AD16 PCI_AD15 PCI_AD13 PCI_AD11 PCI_AD9 PCI_AD6 PCI_AD4 PCI_AD2 PCI_AD0	I/O O	PCI address/data bus Reset state: tristate Bootstrap configuration[1]: FBMODE=1 *Refer to A.1 for additional information.* FBADDRx FlexBus address lines
58B	PCI_IDSEL	I	PCI initialization device select signal Reset state: tristate
65B	/PCI_FRM	I/O	PCI frame signal Reset state: tristate
66B	PCI_TRDY	I/O	PCI target Ready signal Reset state: tristate
67B	/PCI_STOP	I/O	PCI stop signal Reset state: tristate
68B	PCI_PAR	I/O	PCI parity signal Reset state: tristate
75B	/PCI_CXBE0	I/O	PCI command/byte enable signal 0 Reset state: tristate

[1] *Refer to Table 3 for additional information to the system's start-up configuration.*

Pin Number	Signal	I/O	Comments
Pin Row X1C			
1C, 2C	+3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C	GND	-	Ground 0 V
4C, 5C	VIN5V	I	Alternatively supply voltage +5 VDC for CAN transceivers. Refer the description of jumper J36 in *Table 2.*
6C	VBAT	I	Connection for external battery (+) 2.4-3.3 V to supply (backup) the RTC and the serial memory.
8C 9C 26C 48C 49C 50C 51C 53C 54C 55C 56C 58C 59C 60C 61C	XPLD1_2 XPLD1_3 XPLD1_4 XPLD1_5 XPLD1_7 XPLD1_8 XPLD1_10 XPLD0_34 XPLD0_32 XPLD0_31 XPLD0_29 XPLD0_26 XPLD0_24 XPLD0_22 XPLD0_20	I/O	XPLD GPIO Freely available pins to implement application-specific functionality.
10C	/RSTI	I/O	Reset input signal of the ColdFire processor. Reset signal supplied by the voltage supervision device U23 to the processor's /RSTI reset input pin. Can be driven externally. Input resistance is 1kOhm. Do not connect push buttons e.g. to this pin. This pin should be controlled by logic devices only. It is recommended to control the system reset via the /RESIN signal located at X2D10. Asserting the /RESIN signal results in asserting /RSTI from the voltage supervisor. The voltage supervisor adds a reset delay of 200 ms for /RSTI. That means /RSTI will stay active 200 ms after /RESIN is released.
11C	/RSTO	O	Reset output signal of the ColdFire processor. Reset state: low *Refer to A.1 for additional information.*

Pin Number	Signal	I/O	Comments
13C	TXD3_TTL	O I/O	PSC3 transmit data signal PPSC3PSC24 GPIO Reset state: GPI
14C	RXD3_TTL	I I/O	PSC3 receive data signal PPSC3PSC25 GPIO Reset state: GPI
15C	/CTS3_TTL	O I/O I	PCS3 clear to send signal PPSC3PSC27 GPIO Reset state: GPI PSC3BCLK PSC3 modem clock
16C	/RTS3_TTL	I I/O I	PSC3 request to send signal PPSC3PSC26 GPIO Reset state: GPI PSC3FSYNC PSC3 frame sync
18C	CAN_H1	I/O	CAN_High output from the CAN transceiver of the second CAN interface.
19C	RXD1_TTL	I I/O	PSC1 receive data signal PPSC1PSC05 GPIO Reset state: GPI
20C	TXD1_TTL	O I/O	PSC1 transmit data signal PPSC1PSC04 GPIO Reset state: GPI
21C	RXD1	I	RxD input on the RS-232 transceiver for the second ColdFire UART PSC1.
23C	TXD1	O	TxD output on the RS-232 transceiver for the second ColdFire UART PSC1.
24C	/RTS1_TTL	I I/O I	PSC1 request to send signal PPSC1PSC06 GPIO Reset state: GPI PSC1FSYNC PSC1 frame sync
25C	/CTS1_TTL	O I/O I	PCS1 clear to send signal PPSC1PSC07 GPIO Reset state: GPI PSC1BCLK PSC1 modem clock
28C	DSPI_CS5	O I/O	QSPI Chip Select signal 5 PDSPI6 GPIO Reset state: GPI
30C	DSPI_CS2	O I/O O O	QSPI Chip Select signal 5 PDSPI4 GPIO Reset ctate: GPI TOUT2 GP timer output 2 CANTX1 FlexCAN transmit 1
31C	SCL	I/O I/O	I^2C serial clock signal PFECI2C0 GPIO Reset state: GPI

Pin Number	Signal	I/O	Comments
33C	E0_LED0	O	Ethernet 0 LED output for link/activity monitoring.
34C	E0_LED1	O	Ethernet 0 LED output for speed monitoring.
35C	E0_RX-	I	Ethernet 0 negative receive input.
36C	E0_TX-	O	Ethernet 0 negative transmit output.
38C	USBVBUS	I	USB voltage monitor input
39C	E1_LED0	O	Ethernet 1 LED output for link/activity monitoring.
40C	E1_RX-	I	Ethernet 1 negative receive input.
41C	E1_TX-	O	Ethernet 1 negative transmit output.
43C	TIN0	I	GP timer input 0 Reset state: GPI
44C	TIN1	I	GP timer input 1 Reset State: GPI
45C	TOUT1	O	GP timer output 1 Reset state: tristate
46C	TOUT2	O	GP timer output 2 Reset state: tristate
63C	DSCLK	I I	BDM debug serial clock input Bootstrap configuration: MTMOD0=0 /TRST JTAG reset
64C	TCK	I	JTAG test clock input
65C	DSO	O	BDM debug serial output Reset state: high Bootstrap configuration: MTMOD0=0 TDO JTAG data output
66C 68C 69C	PSTDDATA6 PSTDDATA4 PSTDDATA2	O	ColdFire processor status debug data output
70C	/TA	I I/O	Transfer acknowledge on the FlexBus Reset state: tristate PFBCTL1 GPIO (PAR_TA=0)
71C	PSTCLK	O	Processor clock output Supplies 100MHz with 50MHz input clock. Reset state: high
73C	XPLD_TCK	I	XPLD JTAG clock input
74C	XPLD_TMS	I	XPLD JTAG test mode select input. 10kOhm pull-up
75C	DAC0	O	Analog output of the digital to analog converter U14. This device is connected to the I^2C bus with slave address 0x98/0x99.
76C 78C 79C 80C	ADC6 ADC3 ADC1 ADC0	I	Analog input of the analog to digital converter U13. This device is connected to the I^2C bus with slave address 0x90/0x91. *For detailed description refer to the ADC7828 Data Sheet provided by Texas Instruments/Burr-Brown.*

Pin Number	Signal	I/O	Comments
Pin Row X1D			
1D, 2D, 4D, 5D	+3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D	GND	-	Ground 0 V
6D	VPD	O	Power-down supply voltage VPD is generated by VBAT or +3V3 using a diode switching circuitry. VPD serves as supply voltage for the Real-Time Clock and the serial EPROM.
7D 8D 50D 51D 52D 53D 55D 56D 57D 58D 60D 61D	XPLD1_0 XPLD1_1 XPLD1_6 XPLD1_9 XPLD0_35 XPLD0_33 XPLD0_30 XPLD0_28 XPLD0_27 XPLD0_25 XPLD0_23 XPLD0_21	I/O	XPLD GPIO Freely available pins to implement application specific functionality.
10D	/RESIN	I	Manual reset input of the voltage supervisor device U23. Asserting /RESIN results in asserting the system reset /RSTI. After negation of /RESIN the system reset /RSTI stays active for additional 200ms (reset delay). This signal can be used for connection of a reset push button e.g. Signal connected to +3V3 via 10kOhm pull-up resistor.
11D	TXD2_TTL	O I/O	PSC2 transmit data signal PPSC3PSC20 GPIO Reset state: GPI
12D	RXD2_TTL	I I/O	PSC2 receive data signal PPSC3PSC021 GPIO Reset state: GPI
13D	/CTS2_TTL	O I/O I I	PCS2 clear to send signal PPSC3PSC23 GPIO Reset state: GPI PSC2BCLK PSC2 modem clock CANRX0 FlexCAN receive input 0

Pin Number	Signal	I/O	Comments
15D	/RTS2_TTL	I	PSC2 request to send signal
		I/O	PPSC3PSC22 GPIO Reset state: GPI
		I	PSC2FSYNC PSC2 frame sync
		O	CANTX0 FlexCAN transmit output 0
16D	RXD0_TTL	I	PSC0 receive data signal
		I/O	PPSC1PSC01 GPIO Reset state: GPI
17D	TXD0_TTL	O	PSC0 transmit data signal
		I/O	PPSC1PSC00 GPIO Reset state: GPI
18D	CAN_L1	I/O	CANL output on the CAN transceiver for the second CAN interface.
20D	CAN_L0	I/O	CANL output on the CAN transceiver for the first CAN interface.
21D	CAN_H0	I/O	CANH output on the CAN transceiver for the first CAN interface.
22D	RXD0	I	RxD input on the RS-232 transceiver for the first serial interface. Jumper J13 must be closed to use this interface.
23D	TXD0	O	TxD output on the RS-232 transceiver for the first serial interface.
25D	/RTS0_TTL	I	PSC0 request to send signal
		I/O	PPSC1PSC02 GPIO Reset state: GPI
		I	PSC0FSYNC PSC0 frame sync
26D	/CTS0_TTL	O	PCS0 clear to send signal
		I/O	PPSC1PSC03 GPIO Reset state: GPI
		I	PSC0BCLK PSC0 modem clock
27D	DSPI_SIN	I	DSPI serial data in signal
		I/O	PDSPI1 GPIO Reset state: GPI
		I	PSC3RXD PSC3 receive data signal
28D	DSPI_SOUT	O	DSPI serial data out signal
		I/O	PDSPI0 GPIO Reset state: GPI
		O	PCS3TXD PSC3 transmit data signal
30D	DSPI_SCK	I/O	DSPI clock signal
		I/O	PDSPI2 GPIO Reset state: GPI
		O	/PCS3CTS PCS3 clear to send signal
		I	PCS3BCLK PSC3 modem clock
31D	DSPI_CS0	O	DSPICS0/SS DSPI Chip Select 0 in master mode or slave select in slave mode.
		I/O	PDSPI3 GPIO Reset state: GPI
		I	/PSC3RTS PSC3 request to send signal
		I	PSC3FSYNC PSC3 frame sync

Pin Number	Signal	I/O	Comments
32D	SDA	I/O I/O	I^2C serial clock signal PFECI2C1 GPIO Reset state: GPI
33D	/IRQRTC	O	Interrupt output of the RTC U13
35D	E0_RX+	I	Ethernet positive receive input 0
36D	E0_TX+	O	Ethernet positive transmit output 0
37D	USB+	I/O	USB 2.0 positive differential data signal
38D	USB-	I/O	USB 2.0 negative differential data signal
40D	E1_RX+	I	Ethernet positive receive input 1
41D	E1_TX+	O	Ethernet positive transmit output 1
42D	E1_LED1	O	Ethernet 1 LED output for speed monitoring
43D	TOUT0	O	GP timer 0 output
45D	TIN2	I I/O I I	GP timer 2 input PTIM5 GPIO Reset state: GPI /IRQ2 interrupt request input 2 CANRX1 FlexCAN receive input 1
46D	TIN3	I I/O I I	GP timer 3 input PTIM7 GPIO Reset state: GPI /IRQ3 interrupt request input 3 CANRX1 FlexCAN receive input 1
47D	TOUT3	I I/O O	GP timer 3 output PTIM6 GPIO Reset state: GPI CANTX1 FlexCAN transmit output 1
66D 67D 68D 70D 71D	PSTDDATA7 PSTDDATA5 PSTDDATA3 PSTDDATA1 PSTDDATA0	O	ColdFire processor status debug data output
72D	XPLD_TDI	I	XPLD JTAG data input
73D	XPLD_TDO	O	XPLD JTAG data output
75D 76D 77D 78D	ADC7 ADC5 ADC4 ADC2	I	Analog input of the analog to digital converter U13. This device is connected to the I^2C bus with slave address 0x90/0x91. The maximum input voltage must not exceed 3.3 V. *For detailed description refer to the ADC7828 data sheet provided by Texas Instruments/Burr-Brown*
80D	REFA	I/O	Reference voltage input for the ADC at U13. Maximum input voltage must not exceed 3.3 V. The ADC provides an internal 2.5 V reference voltage that can be programmed for output. *For detailed description refer to the ADC7828 data sheet provided by Texas Instruments/Burr-Brown.*

Table 1: Pinout of the phyCORE-Connector X2

3 Jumpers

For configuration purposes, the phyCORE-MCF548x has 36 solder jumpers, some of which have been installed prior to delivery. *Figure 4* illustrates the numbering of the jumper pads, while *Figure 5* and *Figure 6* indicate the location of the jumpers on the board.

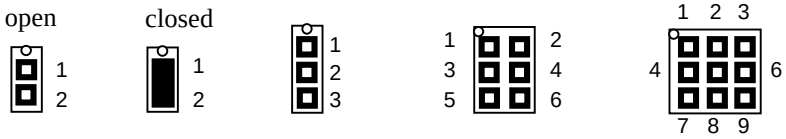

Figure 4: Numbering of the Jumper Pads

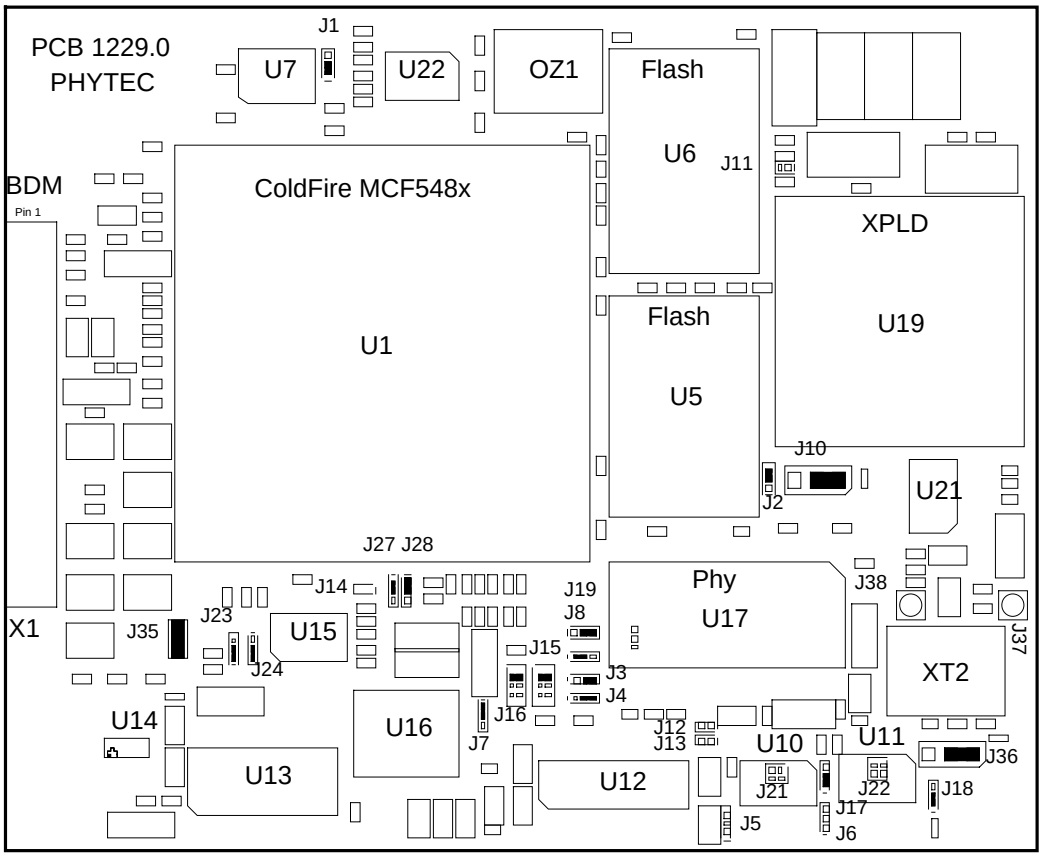

Figure 5: Location of the Jumpers (Controller Side) and Default Settings (phyCORE-MCF548x Standard Version)

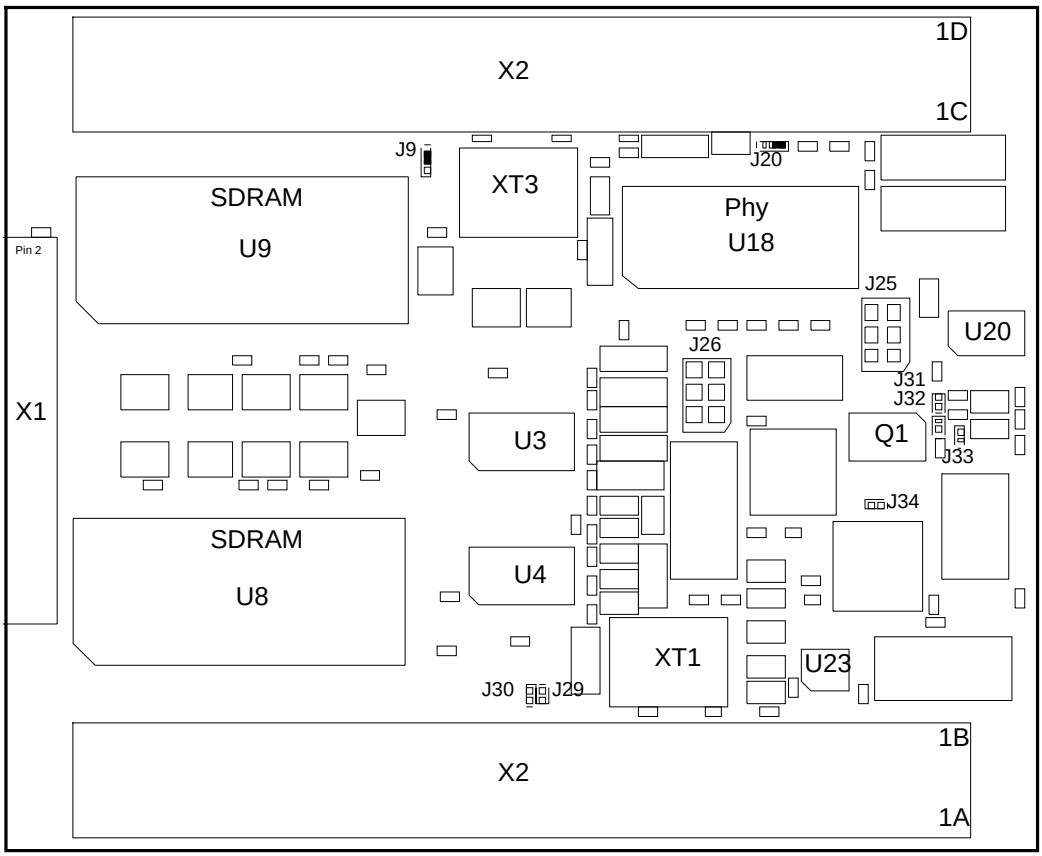

Figure 6: Location of the Jumpers (Connector Side) and Default Settings (phyCORE-MCF548x Standard Version)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1		Selection of CLK_CPU for the address latch signal (ALE).
1 + 2	X	Connects CLK_CPU.
2 + 3		Disconnects CLK_CPU
Package Type		0R in SMD 0402
J2		Selection of /TS or /FB_CS0 for the /ADV input of the Flash devices.
1 + 2		Connects /TS to /ADV
2 + 3	X	Connects /FB_CS0 to /ADV
Package Type		0R in SMD 0402
J3		J3 connects the CANTX0 input of the CAN transceiver U10 to the desired processor CAN output signal. The processor's CAN output must be configured by software. *Please refer to the Processor User's Manual for more detailed information.*
1 + 2		Connects E1_MDC to CANTX0
2 + 3	X	Connects /RTS2_TTL to CANTX0
Package Type		0R in SMD 0402
J4		CANRX0 signal selection. Software has to initialize this signal routing for the FLEX-CAN signals.
1 + 2		Connects E1_MDIO to CANRX0
2 + 3	X	Connects /CTS2_TTL to CANRX0
Package Type		0R in SMD 0402
J5	open	Reference voltage for CAN transceiver at U10
1 + 2		Do not close this jumper.
2 + 3		Do not close this jumper.
Package Type		0R in SMD 0402
J6	open	Reference voltage for CAN transceiver at U11
1 + 2		Do not close this jumper.
2 + 3		Do not close this jumper.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J7		Selection of the supply voltage (3V3 or VPD) of the serial memory. VPD is used in the case that a serial SRAM, which requires buffering of its memory contents, populates the module. For EEPROM and FRAM memory, 3V3 is used, as these memory devices are not volatile.
1 + 2	X	The serial memory is supplied with +3V3.
2 + 3		The serial memory is supplied with VPD.
Package Type		0R in SMD 0402
J8		Connection of the interrupt output (/E0_INT) on the PHY at U17 to the processor.
1 + 2	X	Connects the PHY interrupt to the /IRQ1 (/DREQ1) input on the processor.
2 + 3		Connects the PHY interrupt to the /IRQ2 (TIN2) input on the processor.
Package Type		0R in SMD 0402
J9		Connection of the interrupt output (E1_INT) on the PHY at U18 to the processor
1 + 2	X	Connects the PHY interrupt to the /IRQ4 (/PCI_BR4) input on the processor.
2 + 3		Connects the PHY interrupt to the /IRQ3 (TIN3) input on the processor.
Package Type		0R in SMD 0402
J10		Connection of the power supply for the XPLD device.
1 + 2	X	Connects +3V3 to the supply inputs (ispXPLD LC5256MV)
2 + 3		Connects +2V5 to the supply inputs.
Package Type		0R in SMD 0805
J11		Connection of the WAIT signal for the Flash devices to the processor's /TA signal.
open	X	Disconnects WAIT from /TA signal.
closed		Connects WAIT to the /TA signal.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J12, J13		J12 and J13 disconnect the receive lines (RXD0_TTL and RXD1_TTL) of the MCF548X UART 0 and UART 1 from the RS-232 transceiver at U12. This makes the controller's TTL signals available at pins X2D16 (RXD0_TTL) and X2C19 (RXD1_TTL). This is useful, for instance, for optical isolation of the RS-232 interface.
open		The UART receive signals RXD0_TTL and RXD1_TTL are disconnected from the RS-232 transceiver.
closed	X	The UART receive signals RXD0_TTL and RXD1_TTL are connected to the RS-232 transceiver.
Package Type		0R in SMD 0402
J14		J14 connects pin 7 of the serial memory at U15 to 3V3. On many memory devices pin 7 enables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-MCF548x will have this writing protection function. *Please refer to the corresponding memory data sheet for more detailed information.*
open	X	
closed		
Package Type		0R in SMD 0402
J15		J15 connects the CANTX1 input of the CAN transceiver U11 to the desired processor CAN output signal. The processor's CAN output must be configured by software. *Please refer to the Processor User's Manual for more detailed information.*
1 + 2	X	TOUT2 is connected to CANTX1.
3 + 4		TOUT3 is connected to CANTX1.
5 + 6		DSPI_CS2 is connected to CANTX1.
7 + 8		DSPI_CS3 is connected to CANTX1.
Package Type		0R in SMD 0402
J16		J16 connects the CANRX1 output of the CAN transceiver U11 to the desired processor CAN input signal. The processor's CAN input must be configured by software. *Please refer to the Processor User's Manual for more detailed information.*
1 + 2	X	TIN2 is connected to CANRX1
3 + 4		TIN3 is connected to CANRX1
5 + 6		/IRQ5 is connected to CANRX1
7 + 8		/IRQ6 is connected to CANRX1
Package Type		0R in SMD 0402

Jumper	Default	Comment
J17, J18		J17 and J18 serve to configure the CAN transceiver of FlexCAN channels 0 and 1 on the MCF548X. Texas Instruments SN65HVD230 (or compatible) devices are used as transceivers. Using a resistor tied to GND, the rise time of the CAN signal edge can be configured. With a 0R solder jumper against VCAN, the transceivers are switched to stand-by. VCAN can be configured to 3.3 V or 5 V depending on the used CAN Transceiver device (default 3.3 V). *Please refer the description of J36.*
1 + 2	X	0R resistor: minimal rise time
1 + 2		To reduce electromagnetic interference (EMI), a suitable resistor can populate the board in support of a lower CAN baud rate.
2 + 3		0R resistor: Stand-by
Package Type		0R in SMD 0402
J19, J20		FXSD/FXEN pin configuration for Ethernet PHY U17/U18. *Refer to the Micrel KS8721B/BT data sheet for details.*
1 + 2		Enable Fiber mode, connects FXSD/FXEN to 2V5.
2 + 3	X	Disable Fiber mode, connects FXSD/FXEN to GND.
Package Type		0R in SMD 0402
J21		J21 allows for alternate CAN signal routing of the FlexCAN 0 interface. This jumper must only be closed if no CAN transceiver populates U10 on the module. This option is used e.g. for galvanic isolation of the CAN bus signals.
1 + 2		Routes CANTX0 signal to pin CAN_H0 at X2D21.
3 + 4		Routes CANRX0 signal to pin CAN_L0 at X2D20.
Package Type		0R in SMD 0402
J22		J22 allows for alternate CAN signal routing of the FlexCAN 1 interface. This jumper must only be closed if no CAN transceiver populates U11 on the module. This option is used e.g. for galvanic isolation of the CAN bus signals.
1 + 2		Routes CANTX0 signal to pin CAN_H1 at X2C18.
3 + 4		Routes CANRX0 signal to pin CAN_L1 at X2D18.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J23, J24		J23 and J24 define the slave addresses (A2 and A1) of the serial memory U15 on the I^2C bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. A0 is tied to GND. It must be noted that the RTC at U16 is also connected to the I^2C bus. The RTC has the address 0xA2/ 0xA3 which can not be changed.
1 + 2, 2 + 3	X	A2= 0, A1= 0, A0= 0 (0xA0 / 0xA1) I^2C slave address 0xA0 for write operations and 0xA1 for read access.
1 + 2, 1 + 2		A2= 1, A1= 0, A0= 0 (0xA8 / 0xA9)
2 + 3, 2 + 3		A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5)
2 + 3, 1 + 2		A2= 1, A1= 1, A0=0 (0xAC / 0xAD)
Package Type		0R in SMD 0402
J25		J25 selects the I/O voltage for the XPLD VCCO0. VCCO0 supplies the XPLD signals XPLD0_0 to XPLD0_35. VCCO1 and VCCO2 of the XPLD are connected to 3V3.
1 + 2	X	I/O voltage +3V3
3 + 4		I/O voltage +2V5
5 + 6		I/O voltage +1V5
Package Type		0R in SMD 0805
J26		J26 selects the I/O voltage for the XPLD VCCO3. VCCO3 supplies the XPLD signals XPLD3_0 to XPLD3_35.
1 + 2	X	I/O voltage +3V3
3 + 4		I/O voltage +2V5
5 + 6		I/O voltage +1V5
Package Type		0R in SMD 0805
J27		Jumper to correct processor pin assignment bugs due to unclear ball definition of the initial processor releases. Do not change this jumper!
1 + 2	X	Connects ball V4 of the processor to +1V5.
2 + 3		Connects ball V4 of the processor to +3V3.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J28		Jumper to correct processor pin assignment bugs due to unclear ball definition of the initial processor releases. Do not change this jumper!
1 + 2	X	Connects ball P3 of the processor to +2V5.
2 + 3		Connects ball P3 of the processor to +3V3.
Package Type		0R in SMD 0402
J29		J29 connects the processor's /FB_BWE1 (FlexBus byte write enable) signal to XPLD signal XPLD0_18.
open	X	/FB_BWE1 is not connected to XPLD0_18.
closed		/FB_BWE1 is connected to XPLD0_18.
Package Type		0R in SMD 0402
J30		J30 connects the processor's /FB_BWE3 (FlexBus byte write enable) signal to XPLD signal XPLD0_19.
open	X	/FB_BWE3 is not connected to XPLD0_19.
closed		/FB_BWE3 is connected to XPLD0_19.
Package Type		0R in SMD 0402
J31		J31 connects the power down control input (/E0_PD) of the Ethernet 0 PHY transceiver U17 to the XPLD signal XPLD0_32. /E0_PD has a pull-up resistor of 10kOhm.
open	X	/E0_PD is not connected to XPLD0_32.
closed		/E0_PD is connected to XPLD0_32.
Package Type		0R in SMD 0402
J32		J32 connects the power down control input (/E1_PD) of the Ethernet 1 PHY transceiver U18 to the XPLD signal XPLD0_32. /E1_PD has a pull-up resistor of 10kOhm.
open	X	/E1_PD is not connected to XPLD0_33.
closed		/E1_PD is connected to XPLD0_33.
Package Type		0R in SMD 0402
J33		J33 connects the global clock input XPLD_CLK1 to the signal XPLD0_35 of the XPLD logic device. This feature may be used to establish a wired feedback of a software controlled global clock signal.
open	X	XPLD_CLK1 is not connected to XPLD0_35.
closed		XPLD_CLK1 is connected to XPLD0_35.
Package Type		0R in SMD 0402

Jumper	Default	Comment
J34		J34 connects the global clock input XPLD_CLK2 to the signal XPLD0_34 of the XPLD logic device. This feature may be used to establish a wired feedback of a software controlled global clock signal.
open	X	XPLD_CLK2 is not connected to XPLD0_34.
closed		XPLD_CLK2 is connected to XPLD0_34.
Package Type		0R in SMD 0402
J35		J35 connects the digital ground to the analog ground.
open		GND is not connected to GNDA.
closed	X	GND is connected to GNDA.
Package Type		0R in SMD 0805
J36		J36 selects the VCAN power supply for the CAN transceivers at U10 and U11 depending on the devices populating the module.
1 + 2	X	VCAN is connected to +3V3.
2 + 3		VCAN is connected to VIN5V.
Package Type		0R in SMD 0805
J37		Test point for +2V5 voltage.
J38		Test point for +1V5 voltage.

Table 2: Jumper Settings

4 Power Requirements

The phyCORE-MCF548x must be supplied with one supply voltage only:

Supply voltage: +3.3 V ±10 % with 1A load

Caution:
Connect all +3V3 input pins to your power supply and at least the matching number of GND pins neighboring the +3V3 pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

Optional Supply Inputs VIN5V and VBAT:

VIN5V is used as an alternative 5 V supply voltage for the CAN transceivers populating U10 and U11. VIN5V is connected to the applicable supply pin on these devices by closing Jumper J36 at position 2+3. The standard version of the phyCORE module uses Texas Instruments SN65HVD230 CAN transceivers that are supplied with +3V3 (J36 = 1+2).

VBAT is the input pin that supplies the internal power down voltage VPD. VBAT is connected over two schottky diodes (D10 and D11) to VPD. VPD is also connected over a schottky diode (D9) to +3V3. As long as +3V3 is applied, VPD will be fed through +3V3. Do not apply any voltage source to the VPD pin. This is an output signal. VPD is used to supply the Real-Time Clock U13 and the serial memory device U15 if J7 is closed at position 2+3. VBAT should be supplied from a 3 V source.

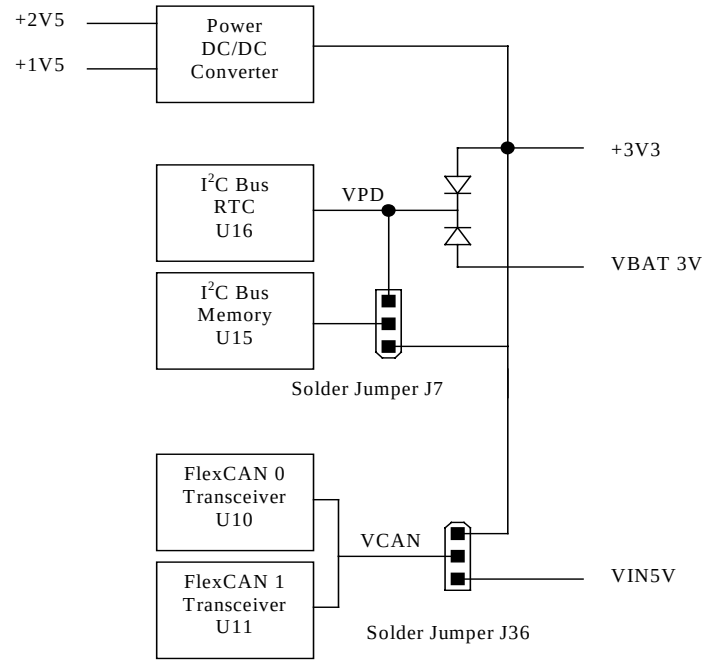

Figure 7: Power Supply Diagram

Internally generated voltages: 1V5, 2V5, 3V3

- 1V5 ColdFire Core
- 2V5 DDR SDRAM and Ethernet PHY
- 3V3 ColdFire I/O, Flash memory and XPLD

4.1 Voltage Supervision and Reset

The input voltage +3V3 as well as the on-board generated operation voltages +2V5 and +1V5 are monitored by a voltage supervisor device at U23. This circuitry is responsible for generation of the system reset signal /RSTI. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /RSTI line will be inactive (high). /RSTI connects to the processor reset input.

/RSTI is a bi-directional signal that can be connected to more then one source. For instance, /RSTI is also connected to the BDM connector of the phyCORE module. The resistance of the signal is 1kOhm.

Special care must be taken when using this signal externally. Do not connect push buttons or long signal lines to this port because this can lead to undesired behavior on this local system reset signal. To connect external reset sources such as push buttons e.g. use the input port /RESIN. /RESIN is connected to a 10kOhm pull-up resistor.

5 System Start-Up Configuration

During the reset cycle, the ColdFire processor reads the state of the local FlexBUS address/data lines to determine the basic system configuration. The configuration circuitry (pull-up or pull-down resistors) is located on the phyCORE module. The processor's FlexBus lines are not directly connected to the phyCORE connector which makes this a very safe procedure since no external circuitry can overwrite these system startup values.

The system start-up configuration includes:

- Clock configuration
- Basic FlexBus characteristic for boot memory configuration
- BDM/JTAG configuration

The following default configuration is read by the processor with the rising edge of reset line /RSTI.

FlexBus Line	**Logic Level**	**Description**	**Default**
FB_AD0 FB_AD1	0 0	PSCONFIG Port Size Configuration of /FB_CS0 connected to Boot Flash Memory	32-bit port
FB_AD2	1	AACONFIG Auto Acknowledge Configuration for /FB_CS0	63 wait states enabled
FB_AD3	1	BECONFIG Byte Enable Configuration	Byte write enable /FB_BWE[3..0]
FB_AD4	1	FBMODE FlexBus Operating Mode	Multiplexed FlexBus and PCI bus on PCI_AD[31..0]
FB_AD5	0	FBSIZE FlexBus Size Configuration	/FB_BWE[3..0] are used for byte strobe and not for TSIZE[1..0] and FB_AD[1..0]
FB_AD6 FB_AD7		reserved	
FB_AD8 FB_AD9 FB_AD10 FB_AD11 FB_AD12	1 1 0 0 0	CLKCONFIG[4..0] CLKIN to SDCLK Ratio	Ratio 1:2 50MHz CLKIN 100MHz int. 200MHz Core

Table 3: System Start-up Configuration

The configuration of the debug/test port is determined by the MTMOD[3..0] signals. The state of these lines is latched with the rising edge of /RSTI.

MTMOD	**Logic Level**	**Description**	**Default**
MTMOD3 MTMOD2 MTMOD1		reserved	Each line tied to GND over 4k7 resistor.
MTMOD0	0	Determines the signal assignment of the test/debug port lines. MTMOD0=1 select JTAG mode MTMOD0=0 selects BDM mode	BDM mode

Table 4: System Start-up Configuration Test/Debug Port

MTMOD0 should not be changed while /RSTI is inactive (high). Dynamic switching between BDM and JTAG operation is not supported.

6 System Memory

The system memory consist of Flash memory, DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) and a small non-volatile memory device:

- 32 or 64 MByte Intel Strata Flash memory
- 64 or 128 MByte DDR SDRAM
- 4 kByte to 32 kByte serial memory (EEPROM, FRAM, buffered SRAM)

The Flash memory is connected to the ColdFire FlexBus and is controlled by /FB_CS0. This Chip Select signal is used for boot operation.

The DDR SDRAM is connected to the special SDRAM interface of the Freescale ColdFire processor and operates at the maximum frequency.

Communication to the small non-volatile memory device (EPROM, FRAM or SRAM) is established over the processor's I^2C bus. This memory device can be used for parameter storage.

6.1 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-MCF548x provides an easily reprogrammable means of code storage. Various Flash devices can be used on the phyCORE-MCF548x:

- 32 or 64 MByte Intel Strata Flash memory
- 32-bit bus width with two devices in parallel
- synchronous or asynchronous operation is possible

The Flash memory bank supports the following Intel memory devices:

Type	Size	Manufacturer	Device Code	Manufacturer Code
Synchronous Devices				
28F256K3	32 MByte	Intel	0x8801	0x0089
28F128K3	16 MByte	Intel	0x8802	0x0089
28F640K3	8 MByte	Intel	0x8803	0x0089
Asynchronous Devices				
28F256J3	32 MByte	Intel	0x001D	0x0089
28F128J3	16 MByte	Intel	0x0018	0x0089
28F640J3	8 MByte	Intel	0x0017	0x0089
28F320J3	4 MByte	Intel	0x0016	0x0089

Table 5: Choice of Flash Memory Devices and Manufacturers[1]

The organization of the Flash memory bank is 32-bit. Two of these 16-bit memory devices are connected to the processor FlexBus in parallel to achieve the 32-bit data bus width. The Flash memory bank is controlled by the processor Chip Select signal /FB_CS0. This Chip Select signal is the dedicated control signal for boot purposes.

1: Flash types in the shaded lines are the preferred parts on the module.

U5 represents the low order (FB_AD[15..0]) and U6 the high order (FB_AD[31..16]) memory device. The Flash memory bank starts at address 0x0000_0000 relative to the base address of the processor's Chip Select signal /FB_CS0.

The access speed depends on the equipped memory device. The FlexBus clock cycle is determined by the processor's input clock. The default configuration selects 50 MHz. The resulting basic cycle time is 20 ns. A processor read or write cycle with 0 wait states consists of one address cycle and one data cycle. The basic access time for a write or read operation amounts to 40 ns. The access time can be extended with the software configurable wait states. One wait state adds a clock cycle time of 20 ns.

To support all memory speed grades up to 120 ns, an access cycle time of 120 ns should be configured. This means that at least 4 wait states must be added for /FB_CS0.

- 4 wait states for /FB_CS0 (supports all possible module configurations)

Following reset a synchronous Flash device (K3 series) always starts in asynchronous mode. To enter the synchronous burst mode, a special initialization sequence must be sent to the Flash devices.

No additional voltages are needed for in-system programming. As of the printing of this manual, Flash devices generally guarantee at least 100.000 erase/programming cycles. *Refer to the applicable INTEL data sheet for detailed description of the erasing and programming procedure.*

6.2 DDR SDRAM

The phyCORE-MCF548x is equipped with fast "Double Data Rate Synchronous Dynamic Random Access Memory" DDR SDRAM devices. This memory is connected to the dedicated SDRAM interface provided by the MCF548x ColdFire processor. This enables the processor to communicate at full core speed of 200 MHz.

The DDR SDRAM memory bank consist of two devices with 16-bit port size each in parallel to support the 32-bit bus width of the processor. The memory bank is controlled by Chip Select signal /SD_CS0 of the processor's DDR SDRAM controller.

Table 6 shows all possible memory configurations.

Available Capacity	Device Organization	Devices (two)
32 MByte	128 MBit 2 MBit x 16 x 4 Banks	MT46V8M16 TSOP66
64 MByte	256 MBit 4 MBit x 16 x 4 Banks	MT46V16M16 TSOP66
128 MByte	512 MBit 8 MBit x 16 x 4 Banks	MT46V32M16 TSOP66

Table 6: DDR SDRAM Device Selection

6.3 Serial Memory

The phyCORE-MCF548x features a non-volatile memory device with a serial I^2C interface. This memory can be used for storage of configuration data or operating parameters, that must not be lost in the event of a power interruption. Depending on the module's configuration, this memory can be in the form of an EEPROM, FRAM or SRAM. The available capacity ranges from 512 Byte to 32 kByte.

If SRAM is used, solder jumper J7 must be closed at position 2+3 to supply the memory device via VPD, hence supporting battery backup.

The MCF548X provides an on-chip I^2C interface to which the memory device is connected.

Table 7 gives an overview of the possible devices for use at U15 as of the printing of this manual.

Type	Size	I^2C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	256/512 Byte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC02/04	CATALYST
	1/ 2 kByte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC08/16	CATALYST
	4/8 kByte	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32/64	CATALYST
	32 kByte	1 MHz	A1, A0	100 000	100 yrs.	CAT24WC256	CATALYST
FRAM	512 Byte	1 MHz	A2, A1	10 billion	10 yrs.	FM24C04	RAMTRON
	8 kByte	1 MHz	A2, A1, A0	10 billion	10 yrs.	FM24C64	RAMTRON
SRAM	256 Byte	100 kHz	A2, A1, A0	-	-	PCF8570	PHILIPS

Table 7: Serial Memory Options for U15

It is important to note that the RTC U16 is also connected to the I^2C bus. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I^2C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using the solder jumpers J23 (A1) and J24 (A2), so that no collision occurs. The address input A0 is hard-wired to GND.

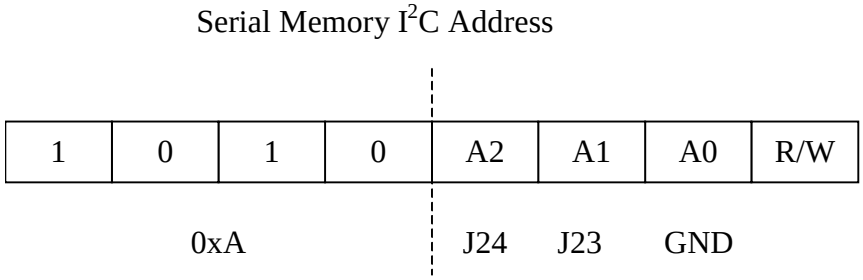

Figure 8: Serial Memory I²C Slave Address

Possible configuration options are shown below:

I²C Address	**J23 A1**	**J24 A2**
0xA0 / 0xA1	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3
0xA8 / 0xA9	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	1 + 2

Table 8: Serial Memory I²C Address (Examples)

Address lines A1 and A2 are not always made available with certain serial memory types. This should be noted when configuring the I²C bus slave address.

7 XPLD System Logic Device

The XPLD logic device U19, supplied by Lattice Semiconductor, is responsible for routing resources on the phyCORE-MCF548x and provides a very flexibly way to connect and operate application-specific hardware components or interfaces in a target design. In general, the XPLD device is not part of the basic processor system as it is not needed to handle the Chip Select signal of the Flash memory or other basic functions. This allows reprogramming of the XPLD during runtime of the processor via the JTAG port. The XPLD JTAG port can served by an external source (programming cable e.g.) or by the on-board ColdFire processor over general purpose I/O pins.

The XPLD is a member of the ispXPLD 5000MX family provided by Lattice Semiconductor (www.latticesemi.com).

- Lattice ispXPLD LC5256MV 5F256-75I

Device Features:

- 256 Macrocells
- 128 kBit internal memory for single or dual-port SRAM, FIFO etc.
- two programmable PLL's; clock shifting capability
- 300 MHz operating frequency
- 141 I/O's with configurable signal characteristics
  pull-up, pull-down, bus-keeper, open-drain
  programmable impedance
  LVCMOS 1.8, 2.5, 3.3 V
  LVTTL
  5 V tolerant I/O for LVCMOS3.3 and LVTTL
  LVDS ports
  SSTL 2, 3 (I & II), HSTL (I, III, IV), PCI 3.3, GTL+, LVPECL

The XPLD is connected to the local processor FlexBus with 32-bit bus width. The logic device acts as bridge for connecting external peripheral devices or interfaces to the ColdFire. A total of 82 I/O lines are available on the Molex connector X2 and can be used for application-specific features.

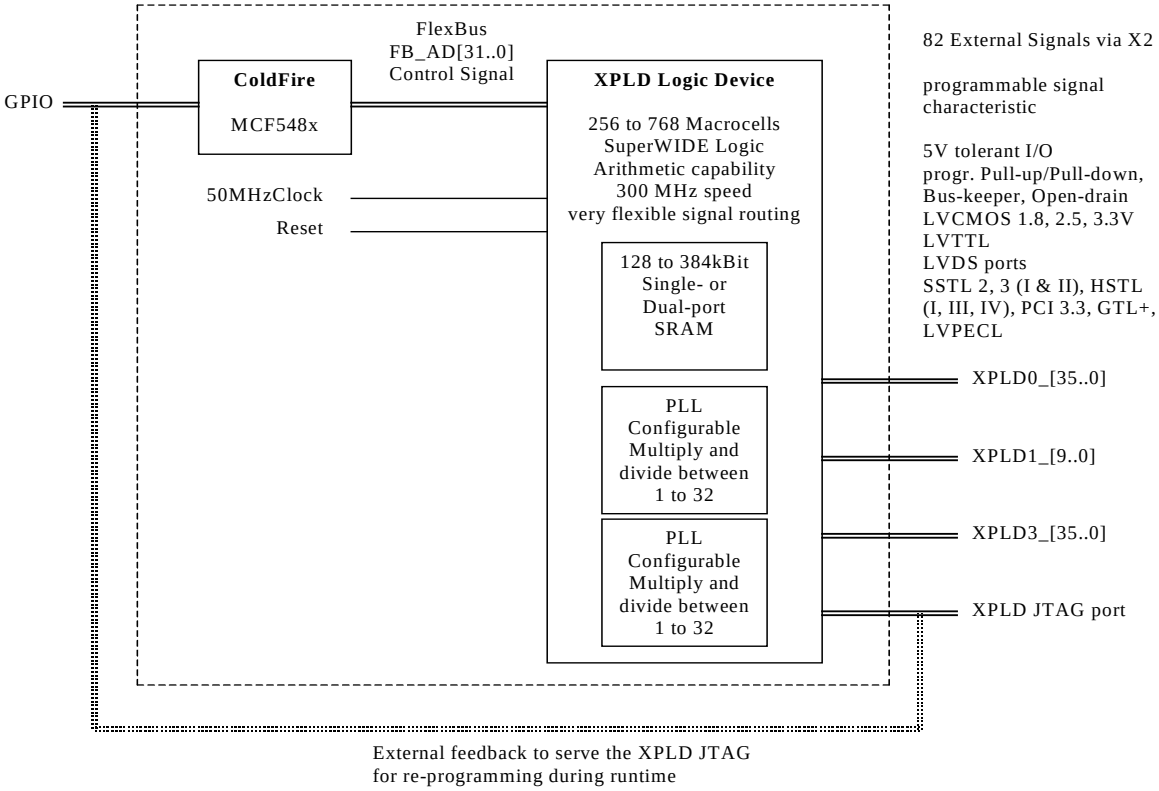

Figure 9: XPLD Configuration

7.1 XPLD Firmware Development

A basic firmware project with pin and signal assignment is provided by PHYTEC. This project is written in VHLD and can be easily extended with customer-specific functionality.

The required development tool is called ispLever and is provided by Lattice Semiconductor. The tool can be downloaded from www.latticesemi.com and is free in its basic version. This version is suitable to compile and create the programmable output file.

8 Serial Interfaces

8.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MCF548x at U12. This device adjusts the signal levels of the TXD0_TTL/RXD0_TTL and TXD1_TTL/RXD1_TTL lines (MCF548X UART). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXD0 or RXD1 line (X2D22/X2C21) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXD0 or TXD1 line (X2D23/X2C23) is connected to the RXD line of the COM port. The Ground circuitry of the phyCORE-MCF548x must also be connected to the applicable Ground pin on the COM port.

The micrcontroller's on-chip UART supports handshake signal communication. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore it is possible to use the TTL signals of both of the UART channels externally. These signals are available at X2D16, X2D17 (RXD0_TTL, TXD0_TTL) and X2C19, X2C20 (RXD1_TTL, TXD1_TTL) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals. Using the solder jumpers J12 and J13, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines RXD0_TTL and RXD1_TTL. This is required so that the external transceiver does not drive signals against the on-board transceiver. The transmit lines TXD0_TTL / TXD1_TTL can be connected parallel to the transceiver input without causing any signal conflicts.

8.2 CAN Interface

Two CAN transceivers (SN65HV230) populate the phyCORE-MCF548x module at U10 / U11.

The on-board transceivers enable transmission and reception of CAN signals via CANTX0 / CANRX0 and CANTX1 / CANRX1. The CAN transceivers support transmission speeds of up to 1 MBit/s and connection of up to 110 nodes on a single CAN network. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). Additionally, the common mode voltage of both CAN transceivers must not exceed the specified threshold: -4 V / +16 V (recommended range –2V to +7V) for the SN65HV230. If the CAN bus system exceeds these limiting values galvanic isolation of the CAN signals is required. For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-MCF548x.

To add external circuits for optical isolation, the CAN transceivers must be removed and the CAN bus signals bypassed by means of soldering jumpers J21 and J22. Then the CAN TTL signals are routed to pins X2C18, X2D18 (CANTX1, CANRX1) and X2D21, X2D20 (CANTX0, CANRX0) of the phyCORE-connector.

For connection of the CANTx and CANRx lines to an external transceiver, we recommend using a Agilent HCPL06xx, Toshiba TLP113, Sharp PC410L0NIP or similar fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

[1] CiA CAN in Automation -.Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

In order to ensure proper message transmission over the CAN bus, a 120 Ohm terminating resistor must be connected to each end of the CAN bus between the CAN_H and CAN_L signals.

Configuration of the On-Board Transceiver:

The transceivers at U10 and U11 can be switched to stand-by by populating jumpers J17 and J18 with a 10k resistor (position 2+3).

Furthermore, the signal rise time can be configured by closing both jumpers at 1+2 (leaving 2+3 open). This results in reduced interference from the CAN bus when using lower baud rates. *For additional information refer to the data sheet for the SN65HV230 CAN transceiver*.

8.3 BDM Debug Interface

The MCF548X offers an on-chip Background Debug Mode (BDM) interface. This interface allows external debug access to the controller without requiring a service software or firmware, such as a Monitor program, running on the chip. This internal debug interface also contains hardware features supporting common cross development systems and debug environments, such as Metrowerks' CodeWarrior. For instance, the MCF548X features internal breakpoint registers enabling debugging in Flash memory.

The on-chip BDM interface extends from the MCF548X to a 26-pin connector at which an external BDM signal converter circuitry can be attached. Such BDM signal converters enable connection of the MCF548X to a host-PC for debugging purposes. This BDM converter is **NOT** located on the phyCORE-MCF548x module.

The BDM signals are available on the pin header connector X1 located at the front edge of the phyCORE module (*refer to Figure 10*).

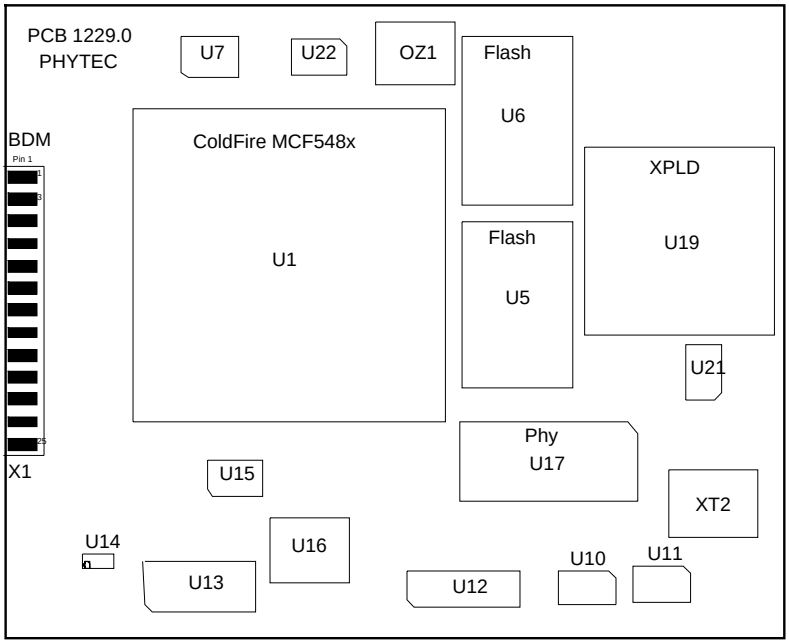

Figure 10: BDM Interface Card Edge Header X1 (Top View)

The footprint of X1 is designed for a double row 26-pin header with 2.0 mm pin spacing. The location of the odd pads on the top side of the PCB is shown in *Figure 10*. The even pin numbers are located on the bottom of the PCB. Pin header X1 is not installed on the standard version of the phyCORE-MCF548x module. In addition, the BDM signals are routed to pins on the Molex connectors (*refer to Table 9*).

The phyCORE-MCF548x Development Board (PCM-982) contains a BDM signal converter circuitry through which decoded BDM signals are routed to the connector at P3. This enables easy connection of the phyCORE-MCF548x (mounted on a Development Board) to a host-PC for start-up, download of user code and debugging.

Table 9 shows the pin assignment on the 26-pin BDM header X1.

BDM Pin #	**Signal[1]**	**BDM Header X1**	**phyCORE X2**
1	reserved	not connected	-
2	/BKPT	/BKPT	D63
3	GND	GND	C62
4	DSCLK	DSCLK	C63
5	GND	GND	D64
6	reserved	TCK	C64
7	/RSTI	/RSTI	C10
8	DSI	DSI	D65
9	+3V3 (VDDIO)	+3V3	C1, D1, C2, D2, D4, D5
10	DSO	DSO	C65
11	GND	GND	C67
12	PSTDDATA7	PSTDDATA7	D66
13	PSTDDATA6	PSTDDATA6	C66
14	PSTDDATA5	PSTDDATA5	D67
15	PSTDDATA4	PSTDDATA4	C68
16	PSTDDATA3	PSTDDATA3	D68
17	PSTDDATA2	PSTDDATA2	C69
18	PSTDDATA1	PSTDDATA1	D70
19	PSTDDATA0	PSTDDATA0	D71
20	GND	GND	D69
21	reserved	not connected	-
22	reserved	not connected	-
23	GND	GND	C72
24	PSTCLK	PSTCLK	C71
25	VDD_CPU	+1V5 Core voltage	-
26	/TA	/TA	C70

Table 9: 26-Pin BDM Connector (X1) and Corresponding Pins on the phyCORE-Connector (X2)

[1]: Recommended BDM Pin Assignment by Freescale

8.4 Ethernet Interface

Connection of the phyCORE-MCF548x to the world wide web or a local network is possible over the integrated FEC's (Fast Ethernet Controller) of the Freescale ColdFire processor. The processor provides up to two FEC's (MCF5485) depending on the actual processor derivate populating the phyCORE module. These FEC's operate with a data transmission speed of 10 or 100 Mbit/s.

8.4.1 PHY Physical Layer Transceiver

The phyCORE-MCF548x has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED monitoring signals extends to phyCORE-connector X2. The MII interface of the FEC's is not available to the user. In order to connect the module to an existing 10/100Base-T network some external circuitry is required. It is important to note that the Physical Layer Transceiver KS8721B (MICREL www.micrel.com) implemented on the phyCORE-MCF548x operates with a 2.5 V supply voltage.

If you are using the applicable Development Board for the phyCORE-MCF548x (part number PCM-982), the external circuitry mentioned above is already integrated on the board (*refer to section 10*).

The PHY address configured with the boot-strapping option is default 0x1 for both devices.

Table 10 shows the interface signals for Ethernet channel 0.

FEC Channel 0 PHY U17	**Pin Function**	**phyCORE Connector X2**
E0_RX+	Differential positive receive input signal	D35
E0_RX-	Differential negative receive input signal	C35
E0_TX+	Differential positive transmit output signal	D36
E0_TX-	Differential negative transmit output signal	C36
E0_LED0	Link/activity LED output "H"/LED off no link "L"/LED on link "toggle"/LED toggle activity	C33
E0_LED1	Speed LED output "H"/LED off 10BT "L"/LED on 100BT	C34

Table 10: Signal Definition PHY 0 Ethernet Port (U17)

Table 11 shows the interface signals for the Ethernet channel 1.

FEC Channel 1 PHY U18	**Pin Function**	**phyCORE Connector X2**
E1_RX+	Differential positive receive input signal	D40
E1_RX-	Differential negative receive input signal	C40
E1_TX+	Differential positive transmit output signal	D41
E1_TX-	Differential negative transmit output signal	C41
E1_LED0	Link/activity LED output "H"/LED off no link "L"/LED on link "toggle"/LED toggle activity	C39
E1_LED1	Speed LED output "H"/LED off 10BT "L"/LED on 100BT	D42

Table 11: Signal Definition PHY 1 Ethernet Port (U18)

8.4.2 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MCF548x is located on the bar code sticker attached to the module. This number is a 12-position HEX value.

8.5 USB 2.0 Interface

The phyCORE-MCF548x integrates a complete USB 2.0 compliant slave interface. This interface supports high-speed (480 Mbit/s) and full-speed (12 Mbit/s) transmission rates. The USB 2.0 controller is integrated in the ColdFire processor including the physical layer transceiver unit.

Table 12 shows the USB signals extend to the phyCORE module connector X2.

USB 2.0 Signals	Pin Function	phyCORE Connector X2
USB+	Differential positive transceiver signal	D37
USB-	Differential negative transceiver signal	D38
USBVBUS	USB voltage monitoring input	C38

Table 12: Signal Definition USB 2.0 Port

For additional information of the USB 2.0 controller refer to the MCF548x Reference Manual as well as the USB 2.0 bus specification provided by www.usb.org.

9 Real-Time Clock RTC-8564 (U16)

For real-time or time-driven applications, the phyCORE-MCF548x is equipped with a RTC-8564 Real-Time Clock at U16. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2
- Power consumption

  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-MCF548x is equipped with a battery (VBAT), the Real-Time Clock runs independently of the board's power supply.

The Real-Time Clock is programmed via the I^2C bus (address 0xA2 / 0xA3). Since the MCF548X is equipped with an internal I^2C controller, the I^2C protocol is processed very effective without extensive processor action (*refer also to section 6.3)*

The Real-Time Clock also provides an interrupt output that extends to the /WAKEUP signal via jumper J26. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

If the RTC interrupt should be used as a software interrupt via a corresponding interrupt input of the processor, the signal /IRTC must be connected externally with a processor interrupt input.

For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.

Note:
After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

10 phyCORE Development Board PCM-982

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

10.1 Concept of the phyCORE Development Board PCM-982

The phyCORE Development Board PCM-982 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MCF548x Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

The following sections contain specific information relevant to the operation of the phyCORE-MCF548x mounted on the phyCORE Development Board PCM-982.

10.2 Development Board PCM-982 Overview

10.2.1 Connectors, Buttons, LEDs

As shown in *Figure 11*, the following connectors, push buttons and LEDs are available on the phyCORE Development Board PCM-982:

X1-	phyCORE-connector for mounting applicable phyCORE module
X2	BDM header, 26-pin, 2.54 mm spacing
X3	JTAG header XPLD, 10-pin, 2.54 mm spacing
X4	PCI slot
X5	JTAG header PCI slot, 10-pin, 2.54 mm spacing
X6	dual USB host sockets
X7	dual USB host sockets
X8	Compact Flash card socket
X9	MMC/SD card socket
X10	socket for +5 volt power supply connectivity
X11	pin header (2.54 mm) for +12 V/-12 V power supply to the PCI slot
X12	mating receptacle for expansion board connectivity
X13	housing/shielding contact
J2	USB slave (MCF) socket
L16	LAN port 0 10/100 Mbit/s Ethernet, RJ-45 socket
L17	LAN port 1 10/100 Mbit/s Ethernet, RJ-45 socket
GND1	GND connector (for connection of GND signal of measuring devices such as an oscilloscope)
P1	dual DB-9 plugs for CAN interface connectivity
P2	dual DB-9 sockets for RS-232 interface connectivity
S1	Boot/NMI push button
S2	Reset push button

D2, 3, 4, 5	USB host port 1 to 4 link LEDs
D6, 7, 10, 11	USB host port 1 to 4 green LEDs
D12, 13, 14, 15	USB host port 1 to 4 amber LEDs
D29	red LED, monitors MCF548X I/O line MPIO0
D30	red LED, monitors the /RSTO line
D31	green power LED, monitors +5V
D32	green power LED, monitors +3V3
D33	red LED, monitors the /RSTI line

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

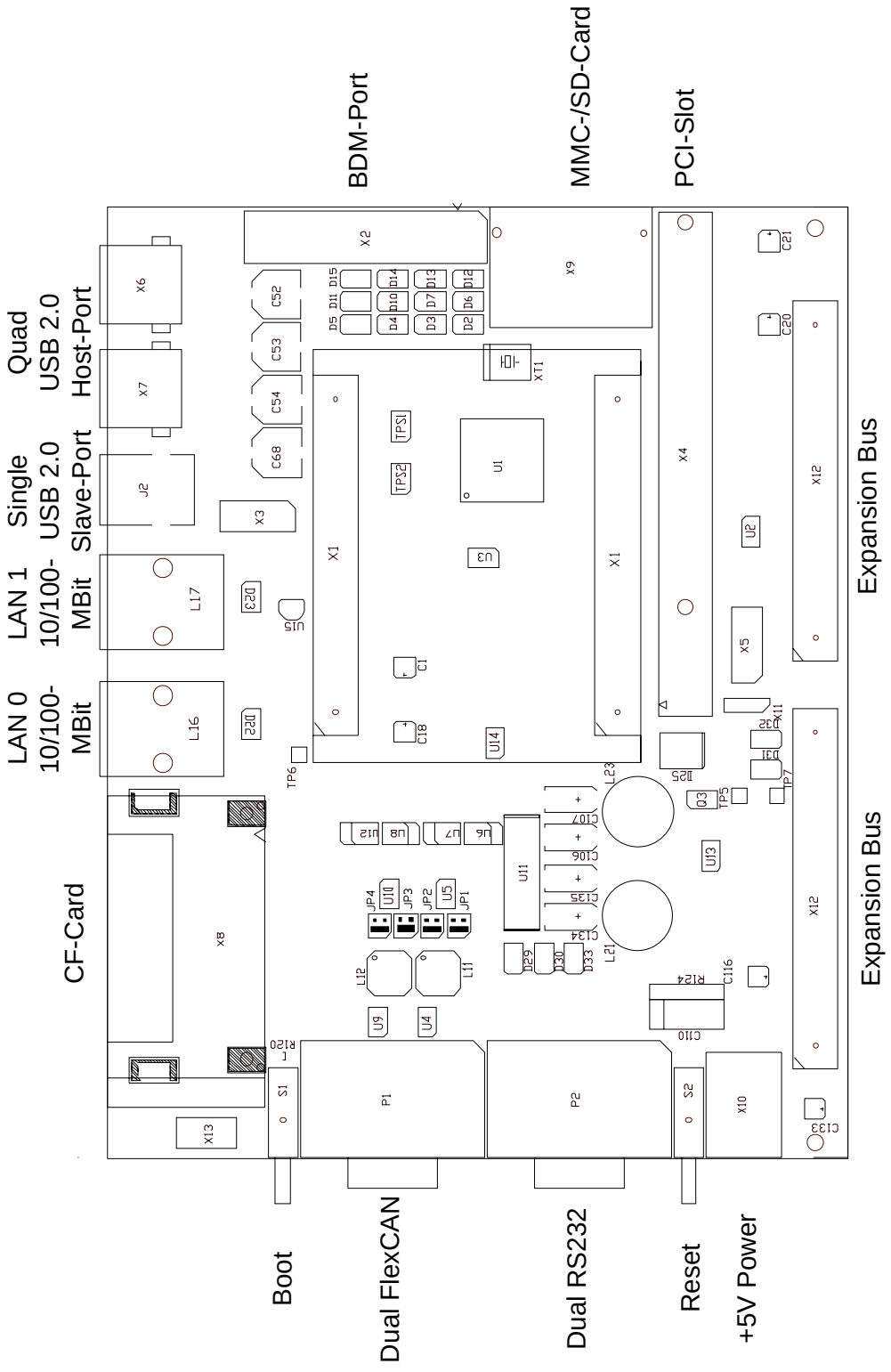

Figure 11: View of the Development Board PCM-982

10.2.2 Jumpers on the phyCORE Development Board PCM-982

Peripheral components of the phyCORE Development Board PCM-982 can be connected to the signals of the phyCORE-MCF548x by setting the applicable jumpers.

The Development Board's peripheral components are configured for use with the phyCORE-MCF548x by means of removable jumpers. If no jumpers are set, no signals are connected to the CAN transceivers. The reset input on the phyCORE-MCF548x directly connects to the Reset button (S2). *Figure 12* illustrates the numbering of the jumper pads, while *Figure 13* indicates the location of the jumpers on the Development Board with its default configuration.

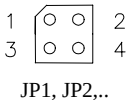

Figure 12: Numbering of Jumper Pads

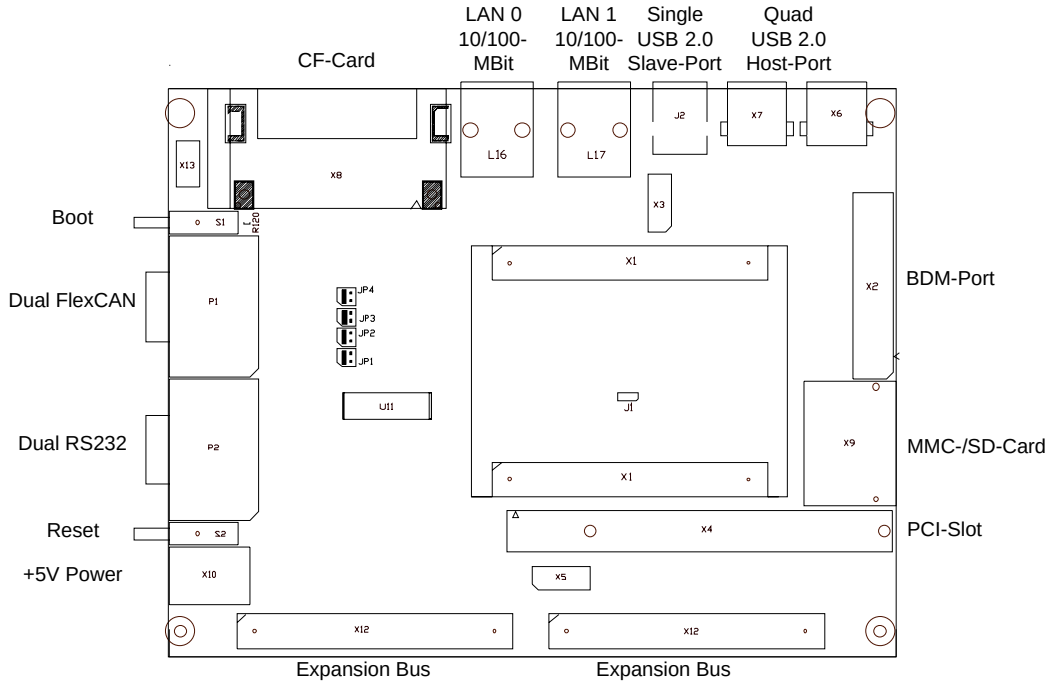

Figure 13: Location of the Jumpers (View of the Component Side)

Jumper	Default Setting	Description
JP1		Routing of the CAN_H0 signal.
1 + 2	X	Connects CAN_H0 to pin 7 of P1A.
1 + 3		Connects CAN_H0 to the opto-coupler U6.
2 + 4		Connects transceiver output CAN_H0_TR to P1A.
JP2		Routing of the CAN_L0 signal.
1 + 2	X	Connects CAN_L0 to pin 2 of P1A.
1 + 3		Connects CAN_L0 to the opto-coupler U7.
2 + 4		Connects transceiver output CAN_L0_TR to P1A.
JP3		Routing of the CAN_H1 signal.
1 + 2	X	Connects CAN_H1 to pin 7 of P1B.
1 + 3		Connects CAN_H1 to the opto-coupler U8.
2 + 4		Connects transceiver output CAN_H1_TR to P1B.
JP4		Routing of the CAN_L1 signal.
1 + 2	X	Connects CAN_L1 to pin 2 of P1B.
1 + 3		Connects CAN_L1 to the opto-coupler U12.
2 + 4		Connects transceiver output CAN_L1_TR to P1B.

Table 13: Development Board Jumper Overview

Figure 13 shows the factory default jumper settings for operation of the phyCORE Development Board PCM-982 with the standard phyCORE-MCF548x. Jumper settings for other functional configurations of the phyCORE-MCF548x module mounted on the Development Board are described in *section 10.3*.

10.3 Functional Components on the phyCORE Development Board PCM-982

This section describes the functional components of the phyCORE Development Board PCM-982 supported by the phyCORE-MCF548x and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MCF548x module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure* 13 and enable alternative or additional functions on the phyCORE Development Board PCM-982 depending on user needs.

10.3.1 Power Supply at X10

Caution:
Do not use a laboratory adapter to supply power to the Development Board! Power spikes during power-on could destroy the phyCORE module mounted on the Development Board! Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +5 VDC ±10% regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MCF548x mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 1000 mA is recommended.

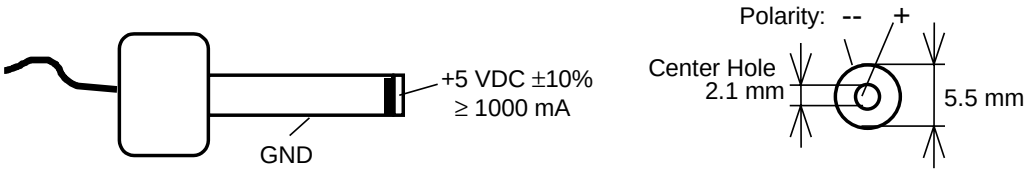

Figure 14: Connecting the Supply Voltage at X10

10.3.2 First Serial Interface at Socket P2A

Socket P2A is the bottom socket of the double DB-9 connector at P2. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the first serial interface.

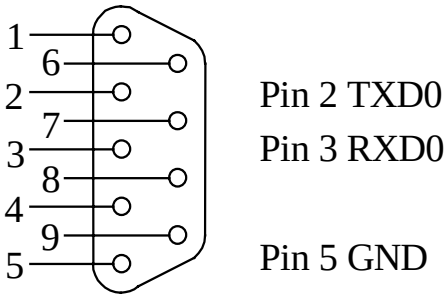

Figure 15: Pin Assignment of the DB-9 Socket P2A as First RS-232 (Front View)

10.3.3 Second Serial Interface at Socket P2B

Socket P2B is the top socket of the double DB-9 connector at P2.

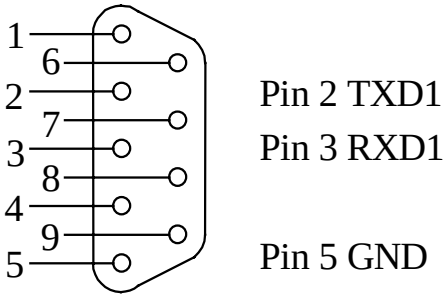

Figure 16: Pin Assignment of the DB-9 Socket P2B as Second RS-232 (Front View)

10.3.4 First CAN Interface at Plug P1A

Plug P1A is the bottom plug of the double DB-9 connector at P1. P1A is connected to the first CAN interface (CAN_0) of the phyCORE-MCF548x via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following two configurations are possible:

1. CAN transceiver on the phyCORE-MCF548x is populated and the CAN signals from the module extend directly to plug P1A.

Jumper	Setting	Description
JP1	1 + 2	Pin 7 of the DB-9 plug P1A is connected to CAN_H0 from on-board transceiver on the phyCORE module
JP2	1 + 2	Pin 2 of the DB-9 plug P1A is connected to CAN_L0 from on-board transceiver on the phyCORE module

Table 14: Jumper Configuration for CAN Plug P1A Using the CAN Transceiver on the phyCORE-MCF548x

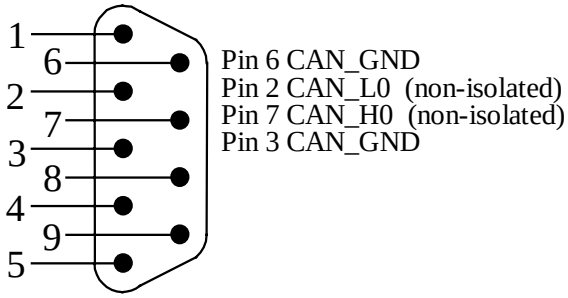

Figure 17: Pin Assignment of the DB-9 Plug P1A (CAN Transceiver on phyCORE-MCF548x, Front View)

2. The CAN transceiver is not populated on the phyCORE-MCF548x and Jumper J21 is closed at 1+2 and 3+4; CAN signals generated by the CAN transceiver (U5) on the Development Board extend to connector P1A **with galvanic separation.**

Jumper	Setting	Description
JP1	2 + 4	Pin 7 of the DB-9 plug P1A is connected to CAN_H0 from on-board transceiver on the Development Board PCM-982.
	1 + 3[1]	Input at opto-coupler U6 on the phyCORE Development Board PCM-982 connected with CAN_H0 (CAN_TX) of the phyCORE-MCF548x.
JP2	2 + 4	Pin 2 of the DB-9 plug P1A is connected to CAN_L0 from on-board transceiver on the Development Board PCM-982.
	1 + 3[1]	Output at opto-coupler U7 on the phyCORE Development Board PCM-982 connected with CAN_L0 (CAN_RX) of the phyCORE-MCF548x.

Table 15: Jumper Configuration for CAN Plug P1A Using the CAN Transceiver on the Development Board with Galvanic Separation

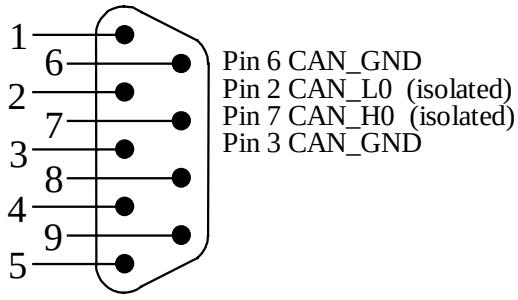

Figure 18: Pin Assignment of the DB-9 Plug P1A (CAN Transceiver on Development Board with Galvanic Separation)

[1]: Please make sure the CAN transceiver on the phyCORE-MCF548x is not populated and Jumper J21 is closed at 1+2 and 3+4.

10.3.5 Second CAN Interface at Plug P1B

Plug P1B is the top plug of the double DB-9 connector at P1. P1B is connected to the second CAN interface (CAN_1) of the phyCORE-MCF548x via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following two configurations are possible:

1. CAN transceiver populating the phyCORE-MCF548x is populated and the CAN signals from the module extend directly to plug P1B.

Jumper	Setting	Description
JP3	1 + 2	Pin 7 of the DB-9 plug P1B is connected to CAN_H1 from on-board transceiver on the phyCORE module
JP4	1 + 2	Pin 2 of the DB-9 plug P1B is connected to CAN_L1 from on-board transceiver on the phyCORE module

Table 16: Jumper Configuration for CAN Plug P2B Using the CAN Transceiver on the phyCORE-MCF548x

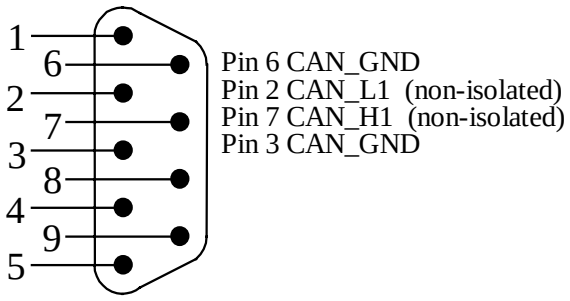

Figure 19: Pin Assignment of the DB-9 Plug P1B (CAN Transceiver on phyCORE-MCF548x, Front View)

2. The CAN transceiver is not populated on the phyCORE-MCF548x and Jumper J22 is closed at 1+2 and 3+4; CAN signals generated by the CAN transceiver (U10) on the Development Board extend to connector P1B **with galvanic separation.**

Jumper	Setting	Description
JP3	2 + 4	Pin 7 of the DB-9 plug P1B is connected to CAN_H1 from on-board transceiver on the Development Board PCM-982.
	1 + 3[1]	Input at opto-coupler U8 on the phyCORE Development Board PCM-982 connected with CAN_H1 (CAN_TX) of the phyCORE-MCF548x.
JP4	2 + 4	Pin 2 of the DB-9 plug P1B is connected to CAN_L1 from on-board transceiver on the Development Board PCM-982.
	1 + 3[1]	Output at opto-coupler U12 on the phyCORE Development Board PCM-982 connected with CAN_L1 (CAN_RX) of the phyCORE-MCF548x.

Table 17: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board with Galvanic Separation

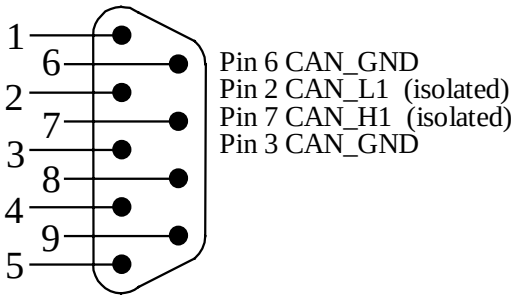

Figure 20: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

[1]: Please make sure the CAN transceiver on the phyCORE-MCF548x is not populated and Jumper J21 is closed at 1+2 and 3+4.

10.3.6 Programmable LED D29

The phyCORE Development Board PCM-982 offers a programmable LED at D29 for user implementations. This LED is connected to port pin XPLD1_0 of the phyCORE-MCF548x. A low-level at port pin XPLD1_0 causes the LED to illuminate, LED D29 remains off when writing a high-level to XPLD1_0.

10.3.7 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 10.1*, most signals from the phyCORE-MCF548x extend to the expansion bus connector X12 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Development Board at X12.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the expansion bus connector (X12 on the Development Board) as well as the patch field.

However, the numbering scheme for expansion bus connector an patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

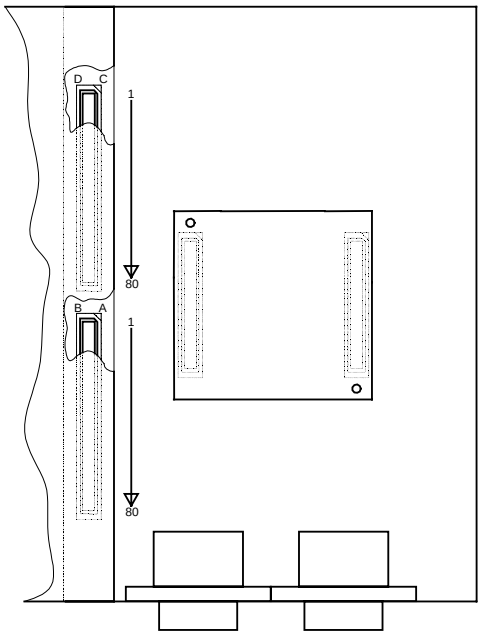

Figure 21: Pin Assignment Scheme of the Expansion Bus

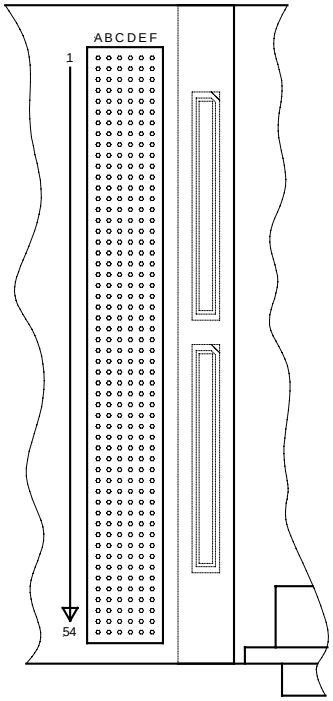

Figure 22: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MCF548x, in conjunction with the expansion bus (X12) on the Development Board and the patch field on an expansion board, is as follows:

phyCORE-MCF548x		**Development Board PCM-982 Expansion Bus**			**Expansion Board PCM-988 Patch Field**	
X2		**X12**			**X21**	
Pin	**Signal**	**Pin**	**Signal**	**Alt. Function**	**Pin**	**Signal**
1A	EXTCLK	1A	EXTCLK		28A	BUS0
3A	/IRQ7	3A	/IRQ7		28B	BUS3
4A	XPLD3_0	4A	XPLD3_0	BOOT	29A	BUS5
5A	/FB_CS1	5A	/FB_CS1		29E	BUS6
6A	XPLD3_1	6A	XPLD3_1	CF_CS0[1]	29D	BUS8
8A	XPLD3_3	8A	XPLD3_3	CF_WR	30E	BUS11
9A	XPLD3_5	9A	XPLD3_5	A1	30D	BUS13
10A	XPLD3_6	10A	XPLD3_6	A2	30F	BUS14
11A	XPLD3_8	11A	XPLD3_8	A4	31E	BUS16
13A	XPLD3_11	13A	XPLD3_11	A7	32A	BUS19
14A	XPLD3_13	14A	XPLD3_13	A9	32E	BUS21
15A	XPLD3_14	15A	XPLD3_14	A10	32B	BUS22
16A	XPLD3_16	16A	XPLD3_16	CF_VS1	33A	BUS24
18A	XPLD3_19	18A	XPLD3_19	CF_IORD	33B	BUS27
19A	XPLD3_21	19A	XPLD3_21	D1	34A	BUS29
20A	XPLD3_22	20A	XPLD3_22	D2	34E	BUS30
21A	XPLD3_24	21A	XPLD3_24	D4	34D	BUS32
23A	XPLD3_27	23A	XPLD3_27	D7	35E	BUS35
24A	XPLD3_29	24A	XPLD3_29	CF_INTRQ	35D	BUS37
25A	XPLD3_30	25A	XPLD3_30	CF_REG	35F	BUS38
26A	XPLD3_32	26A	XPLD3_32	CF_WP	36E	BUS40
28A	XPLD3_35	28A	XPLD3_35	CF_INPK	37A	BUS43
29A	XPLD0_1	29A	XPLD0_1	D9	37E	BUS45
30A	XPLD0_2	30A	XPLD0_2	D10	37B	BUS46
31A	XPLD0_4	31A	XPLD0_4	D12	38A	BUS48
33A	XPLD0_7	33A	XPLD0_7	D15	38B	BUS51
34A	XPLD0_9	34A	XPLD0_9	CF_RDY	39A	BUS53
35A	XPLD0_10	35A	XPLD0_10		39E	BUS54
36A	XPLD0_12	36A	XPLD0_12		39D	BUS56
38A	XPLD0_15	38A	XPLD0_15	CF_CD2	40E	BUS59
39A	XPLD0_17	39A	XPLD0_17		40D	BUS61
40A	XPLD0_18	40A	XPLD0_18		40F	BUS62
41A	/FB_CS4	41A	/FB_CS4		41E	BUS64
43A	/DACK0	43A	/DACK0		42A	BUS67
44A	/DACK1	44A	/DACK1		42E	BUS69
45A	/PCI_RESET	45A	/PCI_RESET		42B	BUS70
46A	/PCI_BR0	46A	/PCI_BR0		43A	BUS72
48A	/PCI_BR1	48A	/PCI_BR1		43B	BUS75

[1] : *See release notes for PCM-982 phyCORE Development Board.*

phyCORE-MCF548x		**Development Board PCM-982 Expansion Bus**			**Expansion Board PCM-988 Patch Field**	
X2		**X12**			**X21**	
Pin	**Signal**	**Pin**	**Signal**	**Alt. Function**	**Pin**	**Signal**
49A	/PCI_BR2	49A	/PCI_BR2		44A	BUS77
50A	/PCI_BR3	50A	/PCI_BR3		44E	BUS78
51A	/PCI_BR4	51A	/PCI_BR4		44D	BUS80
53A	PCI_AD31	53A	PCI_AD31		45E	BUS83
54A	PCI_AD29	54A	PCI_AD29		45D	BUS85
55A	PCI_AD27	55A	PCI_AD27		45F	BUS86
56A	PCI_AD25	56A	PCI_AD25		46E	BUS88
58A	/PCI_CXBE3	58A	/PCI_CXBE3		47A	BUS91
59A	PCI_AD23	59A	PCI_AD23		47E	BUS93
60A	PCI_AD21	60A	PCI_AD21		47B	BUS94
61A	PCI_AD19	61A	PCI_AD19		48A	BUS96
63A	PCI_AD17	63A	PCI_AD17		48B	BUS99
64A	/PCI_CXBE2	64A	/PCI_CXBE2		49A	BUS101
65A	/PCI_IRDY	65A	/PCI_IRDY		49E	BUS102
66A	/PCI_DEVSEL	66A	/PCI_DEVSEL		49D	BUS104
68A	/PCI_PERR	68A	/PCI_PERR		50E	BUS107
69A	/PCI_SERR	69A	/PCI_SERR		50D	BUS109
70A	/PCI_CXBE1	70A	/PCI_CXBE1		50F	BUS110
71A	PCI_AD14	71A	PCI_AD14		51E	BUS112
73A	PCI_AD12	73A	PCI_AD12		52A	BUS115
74A	PCI_AD10	74A	PCI_AD10		52E	BUS117
75A	PCI_AD8	75A	PCI_AD8		52B	BUS118
76A	PCI_AD7	76A	PCI_AD7		53A	BUS120
78A	PCI_AD5	78A	PCI_AD5		53B	BUS123
79A	PCI_AD3	79A	PCI_AD3		54A	BUS125
80A	PCI_AD1	80A	PCI_AD1		54E	BUS126
1B	CLK_EXT	1B	CLK_EXT		28C	BUS1
2B	/IRQ5	2B	/IRQ5		28E	BUS2
3B	/IRQ6	3B	/IRQ6		28F	BUS4
5B	/FB_CS2	5B	/FB_CS2		29B	BUS7
6B	/FB_CS3	6B	/FB_CS3		29F	BUS9
7B	XPLD3_2	7B	XPLD3_2	CF_RD	30A	BUS10
8B	XPLD3_4	8B	XPLD3_4	A0	30B	BUS12
10B	XPLD3_7	10B	XPLD3_7	A3	31A	BUS15
11B	XPLD3_9	11B	XPLD3_9	A5	31B	BUS17
12B	XPLD3_10	12B	XPLD3_10	A6	31F	BUS18
13B	XPLD3_12	13B	XPLD3_12	A8	32C	BUS20
15B	XPLD3_15	15B	XPLD3_15	CF_VS2	32F	BUS23
16B	XPLD3_17	16B	XPLD3_17	CF_CSEL	33C	BUS25
17B	XPLD3_18	17B	XPLD3_18	CF_CS1	33E	BUS26
18B	XPLD3_20	18B	XPLD3_20	D0	33F	BUS28
20B	XPLD3_23	20B	XPLD3_23	D3	34B	BUS31
21B	XPLD3_25	21B	XPLD3_25	D5	34F	BUS33
22B	XPLD3_26	22B	XPLD3_26	D6	35A	BUS34
23B	XPLD3_28	23B	XPLD3_28	CF_IOWR	35B	BUS36

phyCORE-MCF548x		**Development Board PCM-982 Expansion Bus**			**Expansion Board PCM-988 Patch Field**	
X2		**X12**			**X21**	
Pin	**Signal**	**Pin**	**Signal**	**Alt. Function**	**Pin**	**Signal**
25B	XPLD3_31	25B	XPLD3_31	CF_RESET	36A	BUS39
26B	XPLD3_33	26B	XPLD3_33	CF_PDIAG	36B	BUS41
27B	XPLD3_34	27B	XPLD3_34	CF_SPKR	36F	BUS42
28B	XPLD0_0	28B	XPLD0_0	D8	37C	BUS44
30B	XPLD0_3	30B	XPLD0_3	D11	37F	BUS47
31B	XPLD0_5	31B	XPLD0_5	D13	38C	BUS49
32B	XPLD0_6	32B	XPLD0_6	D14	38E	BUS50
33B	XPLD0_8	33B	XPLD0_8		38F	BUS52
35B	XPLD0_11	35B	XPLD0_11		39B	BUS55
36B	XPLD0_13	36B	XPLD0_13		39F	BUS57
37B	XPLD0_14	37B	XPLD0_14	CF_CD1	40A	BUS58
38B	XPLD0_16	38B	XPLD0_16		40B	BUS60
40B	XPLD0_19	40B	XPLD0_19		41A	BUS63
41B	/FB_CS5	41B	/FB_CS5		41B	BUS65
42B	/DREQ0	42B	/DREQ0		41F	BUS66
43B	/DREQ1	43B	/DREQ1		42C	BUS68
45B	CLK_PCI	45B	CLK_PCI_EXP		42F	BUS71
46B	GND	46B	GND		43C	BUS73
47B	/PCI_BG0	47B	/PCI_BG0		43E	BUS74
48B	/PCI_BG1	48B	/PCI_BG1		43F	BUS76
50B	/PCI_BG2	50B	/PCI_BG2		44B	BUS79
51B	/PCI_BG3	51B	/PCI_BG3		44F	BUS81
52B	/PCI_BG4	52B	/PCI_BG4		45A	BUS82
53B	PCI_AD30	53B	PCI_AD30		45B	BUS84
55B	PCI_AD28	55B	PCI_AD28		46A	BUS87
56B	PCI_AD26	56B	PCI_AD26		46B	BUS89
57B	PCI_AD24	57B	PCI_AD24		46F	BUS90
58B	PCI_IDSEL	58B	PCI_IDSEL		47C	BUS92
60B	PCI_AD22	60B	PCI_AD22		47F	BUS95
61B	PCI_AD20	61B	PCI_AD20		48C	BUS97
62B	PCI_AD18	62B	PCI_AD18		48E	BUS98
63B	PCI_AD16	63B	PCI_AD16		48F	BUS100
65B	/PCI_FRM	65B	/PCI_FRM		49B	BUS103
66B	PCI_TRDY	66B	/PCI_TRDY		49F	BUS105
67B	/PCI_STOP	67B	/PCI_STOP		50A	BUS106
68B	PCI_PAR	68B	PCI_PAR		50B	BUS108
70B	PCI_AD15	70B	PCI_AD15		51A	BUS111
71B	PCI_AD13	71B	PCI_AD13		51B	BUS113
72B	PCI_AD11	72B	PCI_AD11		51F	BUS114
73B	PCI_AD9	73B	PCI_AD9		52C	BUS116
75B	/PCI_CXBE0	75B	/PCI_CXBE0		52F	BUS119
76B	PCI_AD6	76B	PCI_AD6		53C	BUS121
77B	PCI_AD4	77B	PCI_AD4		53E	BUS122
78B	PCI_AD2	78B	PCI_AD2		53F	BUS124
80B	PCI_AD0	80B	PCI_AD0		54B	BUS127

phyCORE-MCF548x		**Development Board PCM-982 Expansion Bus**			**Expansion Board PCM-988 Patch Field**	
X2		**X12**			**X21**	
Pin	**Signal**	**Pin**	**Signal**	**Alt. Function**	**Pin**	**Signal**
6C	VBAT	6C	VBAT		2B	VBAT
8C	XPLD1_2	8C	XPLD1_2		3E	PFO
9C	XPLD1_3	9C	XPLD1_3		3B	BOOT//BOOT
10C	/RSTI	10C	/RSTI		3D	/RESET
11C	/RSTO	11C	/RSTO		4E	/RESOUT
13C	TXD3_TTL	13C	TXD3_TTL		4F	GPIO2
14C	RXD3_TTL	14C	RXD3_TTL		5C	GPIO4
15C	/CTS3_TTL	15C	/CTS3_TTL		5E	GPIO5
16C	/RTS3_TTL	16C	/RTS3_TTL		5F	GPIO7
18C	CAN_H1	18C	CAN_H1		6E	GPIO10
19C	RXD1_TTL	19C	RXD1_TTL		6F	GPIO12
20C	TXD1_TTL	20C	TXD1_TTL		7A	GPIO13
21C	RXD1	21C	RXD1		7B	GPIO15
23C	TXD1	23C	TXD1		8A	GPIO18
24C	/RTS1_TTL	24C	/RTS1_TTL		8B	GPIO20
25C	/CTS1_TTL	25C	/CTS1_TTL		8D	GPIO21
26C	XPLD1_4	26C	XPLD1_4		9A	GPIO23
28C	DSPI_CS5	28C	DSPI_CS5		9F	GPIO26
29C	DSPI_CS3	29C	DSPI_CS3		10C	GPIO28
30C	DSPI_CS2	30C	DSPI_CS2		10E	GPIO29
31C	SCL	31C	SCL		10F	GPIO31
33C	E0_LED0	33C	E0_LED0		11E	GPIO34
34C	E0_LED1	34C	E0_LED1		11F	GPIO36
35C	E0_RX-	35C	E0_RX-		12A	GPIO37
36C	E0_TX-	36C	E0_TX-		12B	GPIO39
38C	USBVBUS	38C	USBVBUS		13A	GPIO42
39C	E1_LED0	39C	E1_LED0		13B	GPIO44
40C	E1_RX-	40C	E1_RX-		13D	GPIO45
41C	E1_TX-	41C	E1_TX-		14A	GPIO47
43C	TIN0	43C	TIN0		14F	GPIO50
44C	TIN1	44C	TIN1		15C	GPIO52
45C	TOUT1	45C	TOUT1		15E	GPIO53
46C	TOUT2	46C	TOUT2		15F	GPIO55
48C	XPLD1_5	48C	XPLD1_5		16E	GPIO58
49C	XPLD1_7	49C	XPLD1_7		16F	GPIO60
50C	XPLD1_8	50C	XPLD1_8		17A	GPIO61
51C	XPLD1_10	51C	XPLD1_10		17B	GPIO63
53C	XPLD0_34	53C	XPLD0_34		18A	GPIO66
54C	XPLD0_32	54C	XPLD0_32		18B	GPIO68
55C	XPLD0_31	55C	XPLD0_31		18D	GPIO69
56C	XPLD0_29	56C	XPLD0_29		19A	GPIO71
58C	XPLD0_26	58C	XPLD0_26		19F	GPIO74
59C	XPLD0_24	59C	XPLD0_24		20C	GPIO76
60C	XPLD0_22	60C	XPLD0_22		20E	GPIO77

phyCORE-MCF548x		**Development Board PCM-982 Expansion Bus**			**Expansion Board PCM-988 Patch Field**	
X2		**X12**			**X21**	
Pin	**Signal**	**Pin**	**Signal**	**Alt. Function**	**Pin**	**Signal**
61C	XPLD0_20	61C	XPLD0_20		20F	GPIO79
63C	DSCLK	63C	DSCLK		21E	GPIO82
64C	TCK	64C	TCK		21F	GPIO84
65C	DSO	65C	DSO		22A	GPIO85
66C	PSTDDATA6	66C	PSTDDATA6		22B	GPIO87
68C	PSTDDATA4	68C	PSTDDATA4		23A	GPIO90
69C	PSTDDATA2	69C	PSTDDATA2		23B	GPIO92
70C	/TA	70C	/TA		23D	GPIO93
71C	PSTCLK	71C	PSTCLK		24A	GPIO95
73C	XPLD_TCK	73C	XPLD_TCK		24F	GPIO98
74C	XPLD_TMS	74C	XPLD_TMS		25C	GPIO100
75C	DAC0	75C	DAC0		25E	GPIO101
76C	ADC6	76C	ADC6		25F	GPIO103
78C	ADC3	78C	ADC3		26E	GPIO106
79C	ADC1	79C	ADC1		26F	GPIO108
80C	ADC0	80C	ADC0		27A	GPIO109
6D	VPD	6D	VPD		2D	VPD
7D	XPLD1_0	7D	XPLD1_0		2F	PFI
8D	XPLD1_1	8D	XPLD1_1		3A	WDI
10D	/RESIN	10D	/RESIN		3F	/RESIN
11D	TXD2_TTL	11D	TXD2_TTL		4A	GPIO0
12D	RXD2_TTL	12D	RXD2_TTL		4B	GPIO1
13D	/CTS2_TTL	13D	/CTS2_TTL		5A	GPIO3
15D	/RTS2_TTL	15D	/RTS2_TTL		5B	GPIO6
16D	RXD0_TTL	16D	RXD0_TTL		6A	GPIO8
17D	TXD0_TTL	17D	TXD0_TTL		6C	GPIO9
18D	CAN_L1	18D	CAN_L1		6B	GPIO11
20D	CAN_L0	20D	CAN_L0		7E	GPIO14
21D	CAN_H0	21D	CAN_H0		7D	GPIO16
22D	RXD0	22D	RXD0		7F	GPIO17
23D	TXD0	23D	TXD0		8E	GPIO19
25D	/RTS0_TTL	25D	/RTS0_TTL		8F	GPIO22
26D	/CTS0_TTL	26D	/CTS0_TTL		9E	GPIO24
27D	DSPI_SIN	27D	DSPI_SIN		9B	GPIO25
28D	DSPI_SOUT	28D	DSPI_SOUT		10A	GPIO27
30D	DSPI_SCK	30D	DSPI_SCK		10B	GPIO30
31D	DSPI_CS0	31D	DSPI_CS0		11A	GPIO32
32D	SDA	32D	SDA		11C	GPIO33
33D	/IRQRTC	33D	/IRQRTC		11B	GPIO35
35D	E0_RX+	35D	E0_RX+		12E	GPIO38
36D	E0_TX+	36D	E0_TX+		12D	GPIO40
37D	USB+	37D	USB+		12F	GPIO41
38D	USB-	38D	USB-		13E	GPIO43
40D	E1_RX+	40D	E1_RX+		13F	GPIO46

phyCORE-MCF548x		**Development Board PCM-982 Expansion Bus**			**Expansion Board PCM-988 Patch Field**	
X2		**X12**			**X21**	
Pin	**Signal**	**Pin**	**Signal**	**Alt. Function**	**Pin**	**Signal**
41D	E1_TX+	41D	E1_TX+		14E	GPIO48
42D	E1_LED1	42D	E1_LED1		14B	GPIO49
43D	TOUT0	43D	TOUT0		15A	GPIO51
45D	TIN2	45D	TIN2		15B	GPIO54
46D	TIN3	46D	TIN3		16A	GPIO56
47D	TOUT3	47D	TOUT3		16C	GPIO57
48D	nc	48D	GPIO59		16B	GPIO59
50D	XPLD1_6	50D	XPLD1_6		17E	GPIO62
51D	XPLD1_9	51D	XPLD1_9		17D	GPIO64
52D	XPLD0_35	52D	XPLD0_35		17F	GPIO65
53D	XPLD0_33	53D	XPLD0_33		18E	GPIO67
55D	XPLD0_30	55D	XPLD0_30		18F	GPIO70
56D	XPLD0_28	56D	XPLD0_28		19E	GPIO72
57D	XPLD0_27	57D	XPLD0_27		19B	GPIO73
58D	XPLD0_25	58D	XPLD0_25		20A	GPIO75
60D	XPLD0_23	60D	XPLD0_23		20B	GPIO78
61D	XPLD0_21	61D	XPLD0_21		21A	GPIO80
62D	MTMOD0	62D	MTMOD0		21C	GPIO81
63D	/BKPT	63D	/BKPT		21B	GPIO83
65D	DSI	65D	DSI		22E	GPIO86
66D	PSTDDATA7	66D	PSTDDATA7		22D	GPIO88
67D	PSTDDATA5	67D	PSTDDATA5		22F	GPIO89
68D	PSTDDATA3	68D	PSTDDATA3		23E	GPIO91
70D	PSTDDATA1	70D	PSTDDATA1		23F	GPIO94
71D	PSTDDATA0	71D	PSTDDATA0		24E	GPIO96
72D	XPLD_TDI	72D	XPLD_TDI		24B	GPIO97
73D	XPLD_TDO	73D	XPLD_TDO		25A	GPIO99
75D	ADC7	75D	ADC7		25B	GPIO102
76D	ADC5	76D	ADC5		26A	GPIO104
77D	ADC4	77D	ADC4		26C	GPIO105
78D	ADC2	78D	ADC2		26B	GPIO107
80D	REFA	80D	REFA		27E	GPIO110

Table 18: Signal Pin Assignment for the phyCORE-MCF548x / Development Board / Expansion Board

phyCORE MCF548X		**Development Board PCM-982 Expansion Bus**		**Expansion Board PCM-988 Patch Field**	
+3V3	1C, 2C, 1D, 2D	3V3	1C, 2C, 1D, 2D	VCC1	1A, 1C
VIN5V	4C, 5C	5V	4C, 5C	VCC2	2A, 1B
+3V3	4D, 5D	3V3	4D, 5D	VCC3	2C, 1D
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D	GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D	GND	3C, 4C, 7C, 8C, 9C, 12C, 13C, 14C, 17C, 18C, 19C, 22C, 23C, 24C, 27C, 29C, 30C, 31C, 34C, 35C, 36C, 39C, 40C, 41C, 44C, 45C, 46C, 49C, 50C, 51C, 54C, 4D, 5D, 6D, 9D, 10D, 11D, 14D, 15D, 16D, 19D, 20D, 21D, 24D, 25D, 26D, 28D, 31D, 32D, 33D, 36D, 37D, 38D, 41D, 42D, 43D, 46D, 47D, 48D, 51D, 52D, 53D, 1E, 2E
GNDA	77C, 74D, 79D	GNDA	77C, 74D, 79D		

Table 19: Pin Assignment Power Supply for the phyCORE-MCF548x / Development Board / Expansion Board

10.3.8 Silicon Serial Number/Temperature Sensor

Communication to a DS2401 Silicon Serial Number or DS18B20 Temperature Sensor Silicon Serial Number can be implemented in various software applications for the definition of a node address or as copy protection in networked applications. The DS18B20 measures the ambient temperature form –55°C to +125°C. The accuracy is ±0.5°C within –10 to +85°C. The device can be soldered at space U15 on the Development Board.

The Silicon Serial Number Chip mounted on the phyCORE Development Board PCM-982 is connected to port pin XPLD1_4 of the XPLD.

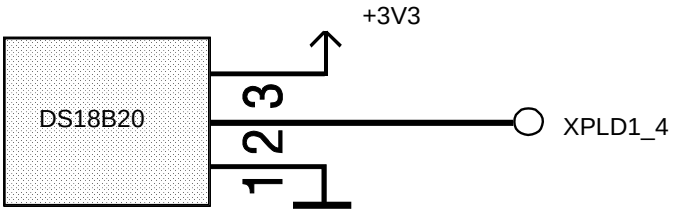

Figure 23: Connecting the DS18B20 Temperature Sensor with Silicon Serial Number

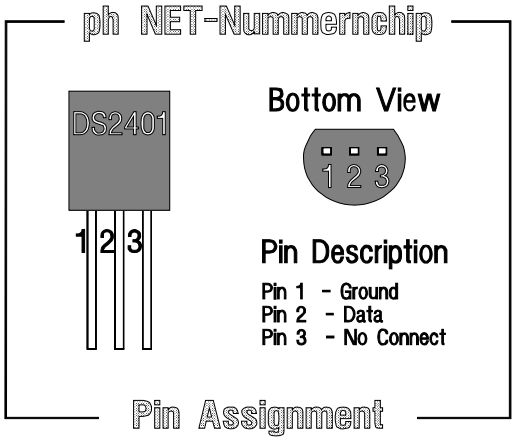

Figure 24: Pin Assignment of the DS2401 Silicon Serial Number

10.3.9 BDM Port X2

The 26-pin header with 2.54 mm pin spacing at X2 is used to connect the processor's BDM debug port to the host-PC's development system (e.g. Metrowerks CodeWarrior) using an appropriate BDM interface unit (e.g. Abatron BDI 2000, P&E BDM interface).

BDM Pin Number	BDM Header X2
1	Not connected
2	/BKPT
3	GND
4	DSCLK
5	GND
6	TCK
7	/RSTI
8	DSI
9	+3V3
10	DSO
11	GND
12	PSTDDATA7
13	PSTDDATA6
14	PSTDDATA5
15	PSTDDATA4
16	PSTDDATA3
17	PSTDDATA2
18	PSTDDATA1
19	PSTDDATA0
20	GND
21	Not connected
22	Not connected
23	GND
24	PSTCLK
25	+1V5
26	/TA

Table 20: Pin Assignment of the BDM Pin Header X2

Caution:
Do not install or remove the BDM cable from the header while the target system is powered up. Always disconnect the power supply before attaching or removing the BDM device!

10.3.10 Technical Specification of the Development Board

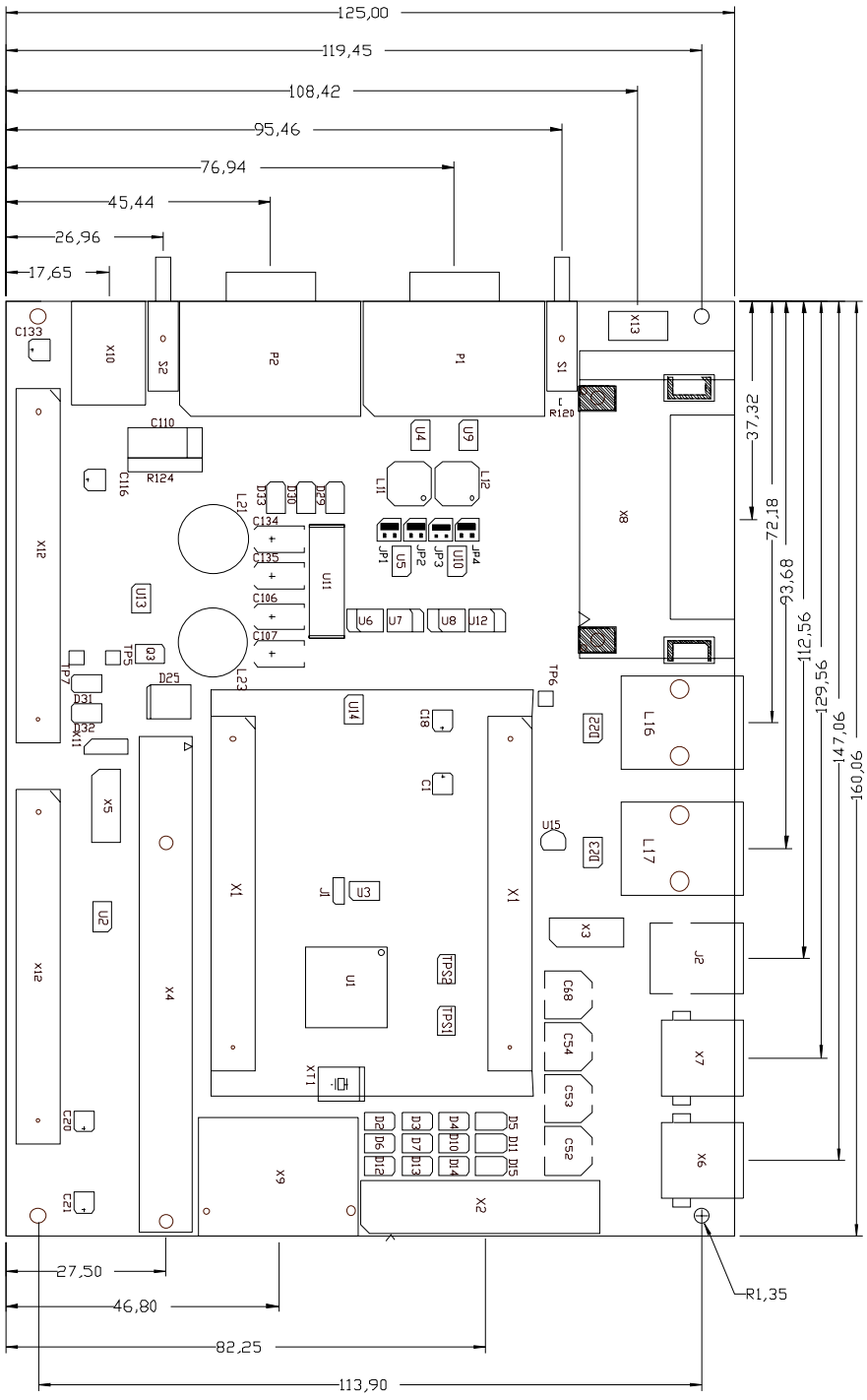

Figure 25 Physical Dimensions of the Development Board PCM-982

Technical Data:

Parameter	Requirements	Characteristics
Dimensions		160 mm x 125 mm
Weight	With maximum circuitry installed, no PCI connector mounted	Approximately 190 grams
Humidity		Max. 95 % r.F., not condensed
Storage Temp. Range		-40° to +90°C
Operating Temp. Range:		0 °C to +70 °C
Operating voltages:		5 V ±10 %
Operating Power Consumption: Voltage +5 V	phyCORE-MCF548x ColdFire MCF5485 200 MHz core clock 128 Mbyte DDR SDRAM 32 Mbyte Flash without any installed I/O line or CF card, MMC/SD card, PCI card or expansion board	 Typ. 750 mA

Table 21: Technical Data of the Development Board PCM-982

10.3.11 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Caution:
This manual exclusively describes the board revision 4132.0

Revision: PCB# 4132.0

- /RESTI signal monitoring LED D33 without function. Current limiting resistor R122 is removed. With installed R122, /RSTI signal don't reach signal low level.

- CF-Card socket X8 pin 7 is disconnected from /FB_CS1 and wired to the phyCORE connector X1A6 signal XPLD3_1.

- Power Connector X10: Pins 2 and 3 have to short circuit to connect the system ground to the external power supply line.

11 Technical Specifications of the phyCORE-MCF548x

The physical dimensions of the phyCORE-MCF548x are represented in *Figure 26.*

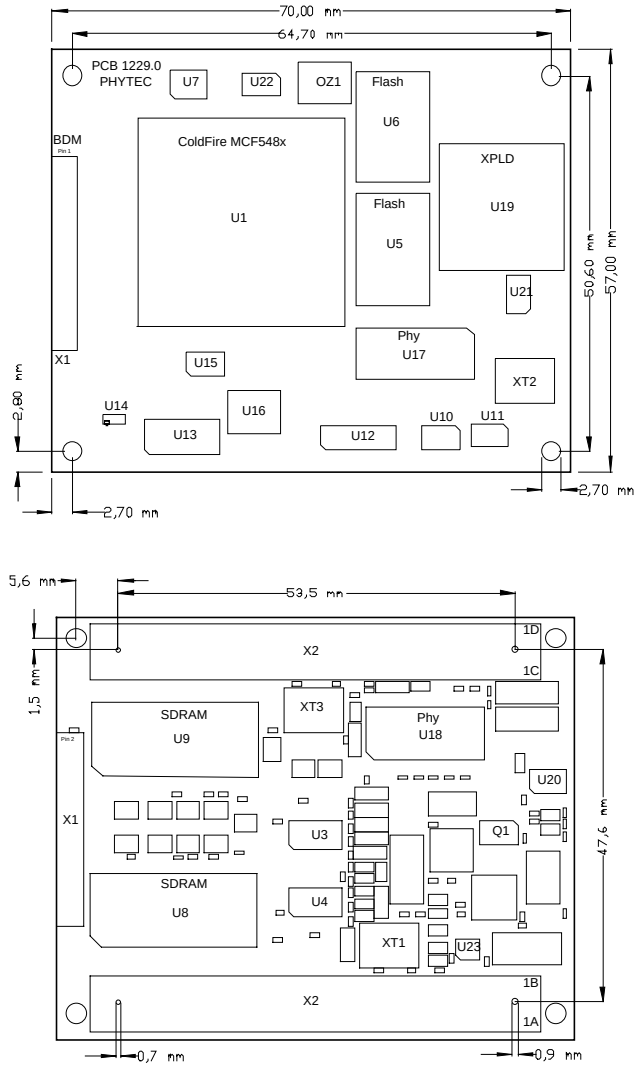

Figure 26: Physical Dimensions

The height of all components on the top side of the PCB is ca. 3 mm. The PCB itself is approximately 1.3 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 3 mm.

Technical Data:

Parameter	Requirements	Characteristics
Dimensions		70 mm x 57 mm
Weight	With maximum circuitry installed, no BDM header at X1	Approximately 31 grams
Humidity		Max. 95 % r.F., not condensed
Storage Temp. Range		-40° to +90°C
Operating Temp. Range:		-40 °C to +85 °C
Operating voltages: Voltage +3V3 Optional: Voltage VIN5V VBAT		 3.3 V ±10 % 5 V ±10 % Typ. 3 V
Operating Power Consumption: Voltage +3V3 Voltage VBAT	50 MHz input frequency ColdFire MCF5485 200 MHz core clock 128 MByte DDR SDRAM 32 MByte Flash without applied +3V3 RTC only	 Typ. 650 mA Typ. <1 µA
Reset Delay Time	After valid system voltages	Approx. 200 ms

Table 22: Technical Data of the phyCORE-MCF548x

These specifications describe the standard configuration of the phyCORE-MCF548x as of the printing of this manual.

Connectors on the phyCORE-MCF548x:

Manufacturer	Molex
Number of pins per contact rows	160 (2 rows of 80)
Molex part number	52760-1609 (receptacle)
Molex part number (lead free)	52760-1679 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-MCF548x. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the underside of the phyCORE must be subtracted.

- Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number	55091-1609 (plug)
Molex part number (lead free)	55091-1679 (plug)
PHYTEC type number	VB082

- Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number	53553-1609 (plug)
Molex part number (lead free)	53553-1679 (plug)
PHYTEC type number	VB085

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

12 Hints for Handling the Module

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Integrating the phyCORE-MCF548x in Application Circuitry

Successful integration in user target circuitry depends on whether the layout for the GND connections matches those of the phyCORE module. It is recommended that the target application circuitry is equipped with one layer dedicated to carry the GND potential. In any case, be sure to connect all GND pins neighboring signals which are used in the application circuitry. For the supply voltage, there must be contact with at least six of the GND pins neighboring the supply voltage pins.

13 Design Considerations - Check List

Please note the following facts when implementing the phyCORE-MCF548x into target applications:

- Data line D0 represents the LSB and D31 the MSB.
- Address line A0 represents the LSB and A31 the MSB.
- Byte ordering is Big Endian.
- Never connect signals to the MCF548X output drivers carrying a higher potential (e.g. pull-ups) than the internal supply voltage.

For more information on the controller's I/O voltage range as well as other controller-related features please refer to the detailed MCF548X User's Manual provided by Freescale.

14 Revision History

Date	Version numbers	Changes in this manual
1/21/05	Manual L-645e_1 PCM-024 PCB# 1229.0 PCM-982 PCB# 4132.0	First release version.

15 Component Placement Diagram

INSERT 1229-0BS TurboCAD.dxf

Figure 27: phyCORE-MCF548x Component Placement, Top View

INSERT 1229-0LS TurboCAD.dxf

Figure 28: phyCORE-MCF548x Component Placement, Bottom View

A Appendices

A.1 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Caution:
This manual exclusively describes the board revision 1229.0

Revision: PCB# 1229.0

Refer to the processor's errata sheet provided by Freescale.

- ColdFire integrated USB device does not work due to a processor bug.

- /RSTO does not follow /RSTI. During /RSTI active /RSTO is held tristate by the processor resulting in a signal level depending on the external connected components. /RSTO needs an external pull-up resistor.

- Bootstrapping option FBMODE is set to FlexBus address bus on PCIAD pins. This is done by the pull-down resistor R11. Next revision will have a pull-up resistor to initiate the PCI bus. PCI bus cannot be used while FBMODE is initialized to 1.

- ADC converter is not present on 1229.0. Footprint is not compatible to the device.

- Bootstrapping problems for the PHY 1 (U18) device. Reset input must be connected to /RSTI instead of /RSTO.

Index

F

G

H

I

J

Document: **phyCORE-MCF548x**
Document number: **L-645e_1, January 2005**

How would you improve this manual?

Did you find any mistakes in this manual? page

Submitted by:
Customer number: _____

Name: _____

Company: _____

Address: _____

_____

Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

Published by

PHYTEC

Ordering No. L-645e_1
Printed in Germany