Modification of the pinout for the phyCORE-i.MX 6UL (PCL-063-xxxxxxx.A0)

The information in this document is relevant for development of carrier boards for future phyCORE-i.MX 6UL modules (from PCB# 1468.1 on).

Dear valued Kit-customer,
We appreciate your interest in evaluating our phyCORE-i.MX 6UL. For this purpose, you do receive the Alpha kit in this delivery. The kit is still based on pin-assignment PCB-No 1468.0 (see below).

The phyCORE-i.MX 6UL is currently in redesign-stage in order to support all i.MX 6UL device options. SNVS_TAMPER pins can not be used as GPIO in G3 version of the i.MX 6UL.

Unfortunately we are forced to change the pin-assignment of the module as part the current redesign process. The new circuit diagram is labelled "PCB-No.: 1468.1" on the bottom right side; the current version which matches the design of the module you received is labelled "PCB-No.: 1468.0"

Do only use the new pin-assignment according to "PCB-No.: 1468.1" for your baseboard designs.

The following table provides an overview of the changes in the phyCORE-i.MX 6UL's pinout. The changes may affect the pin-muxing of custom carrier boards as well as software changes in the BSP.

List of the pin-assignment-changes:

Pin#	Previous pad-/signal name revision **1468.0**	Future pad-/signal name from revision **1468.1** on
51	NAND_CE1_B	SNVS_TAMPER9 (GPIO5_9)
95	GPIO1_2	SNVS_TAMPER5 (GPIO5_5)
74	GPIO1_8	GPIO1_8 **default** Changeable for G3 version with J11 to: SNVS_TAMPER4 (GPIO5_4)

The following table describes the signals at Pin74 and USER_LED depending on the configuration of Jumper J11:

	J11 1+4, 2+3 **default**	J11 1+2, 3+4
Pin 74	GPIO1_8	SNVS_TAMPER4 (GPIO5_4)
USER_LED	SNVS_TAMPER4 (GPIO5_4) –› does not work with G3	GPIO1_8

Please contact our support team (+49 (6131) 9221-31, or support@phytec.de) if you need any further information.

We apologize for any inconveniences.
Best regards, your PHYTEC-Team

