SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C517A

Data Sheet 01.99

C517A Data Sheet **Revision History :**		01.99
Previous Releases :		08.97 (Original Version)
Page (previous version)	Page (new version)	Subjects (changes since last revision)
All sections	All sections	V_{CC} is changed to V_{DD} and I_{CC} is changed to I_{DD}.
2	2	"with wake-up capability through INT0 pin" is removed.
2	2	P-LCC-84 package is added under the feature list.
2 to 3	2	Table 1; deleted and replaced by “Ordering Information” paragraph “Additional Literature”;deleted.
5	5	Figure 4; added.
5	6	Table 1; modified, column “P-LCC-84” is added.
47	50	"or by a short low pulse at pin P3.2/INT0" is removed.
48	50	"Short low pulse at pin P3.2/INT0" is removed.
49	52	“Absolute Maximum Ratings” is changed to tabular form.
49	52	Fifth line; “During overload conditions ...” changed to “During absolute maximum rating conditons ...”.
49	52	“Operating Conditions” is added.
50	53	“V_{CC} = 5 V + 10% ... “ is replaced by “(Operating Conditions apply)”.
51	54	Notes (7); modified.
53	56	“V_{CC} = 5 V + 10% ... “ is replaced by “(Operating Conditions apply)”.
55	58	“V_{CC} = 5 V + 10% ... “ is replaced by “(Operating Conditions apply)”.
62	65	First line; “C517A-1RM” is replaced by “C517A-4RM/4RN”
-	69	Figure 38; added.

Edition 01.99

This edition was realized using the software system FrameMaker®.

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SIEMENS

8-Bit CMOS Microcontroller C517A

Advance Information

- Full upward compatibility with SAB 80C517A/83C517A-5
- Up to 24 MHz external operating frequency
  – 500 ns instruction cycle at 24 MHz operation
- Superset of the 8051 architecture with 8 datapointers
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- 32K byte on-chip ROM (with optional ROM protection)
  – alternatively up to 64K byte external program memory
- Up to 64K byte external data memory
- 256 byte on-chip RAM
- Additional 2K byte on-chip RAM (XRAM)
- Seven 8-bit parallel I/O ports
- Two input ports for analog/digital input

(further features are on next page)

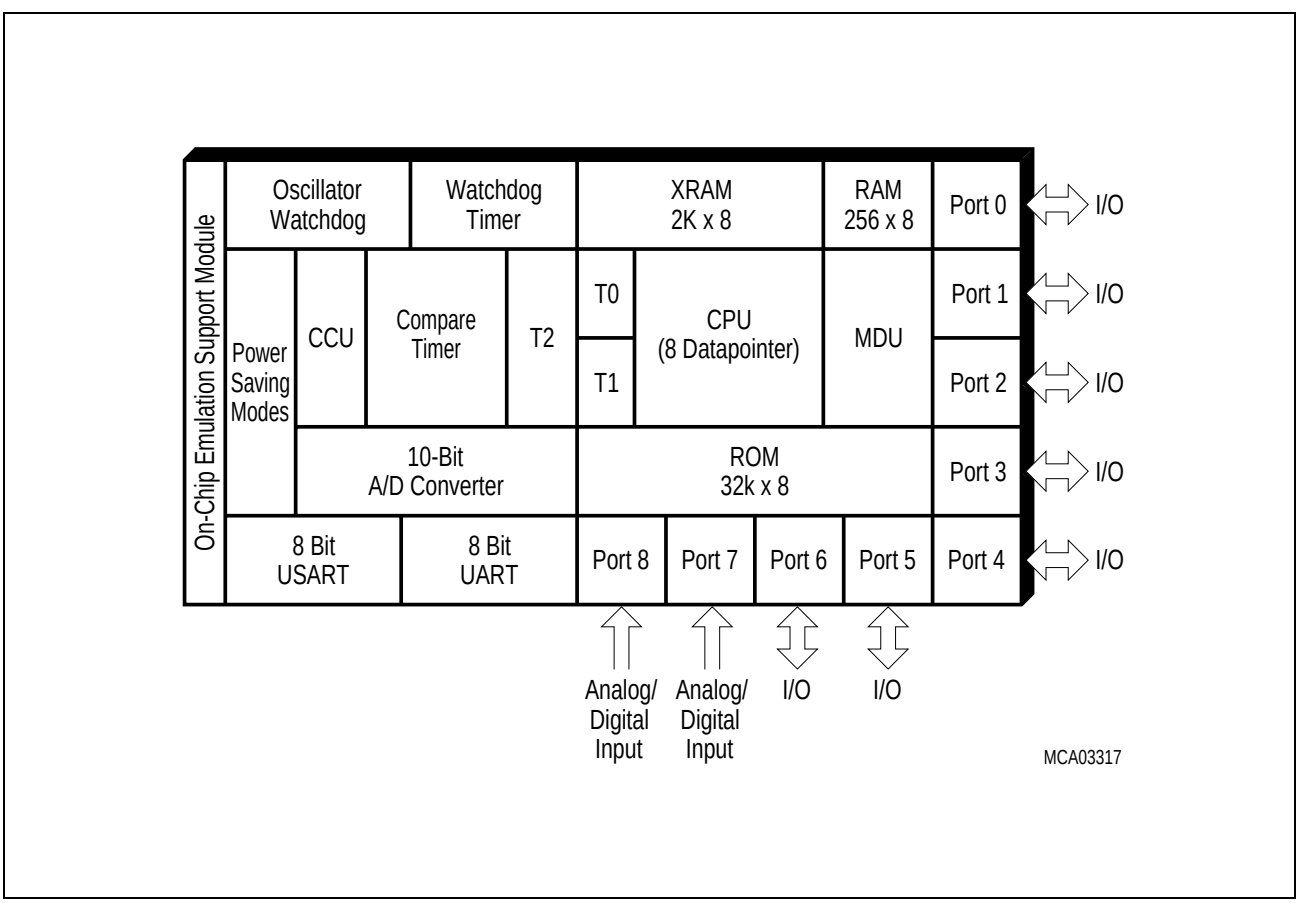


Figure 1
C517A Functional Units

Features (continued) :

- Two full duplex serial interfaces (USART)
  - 4 operating modes, fixed or variabie baud rates
  - programmable baud rate generators
- Four 16-bit timer/counters
  - Timer 0 / 1 (C501 compatible)
  - Timer 2 for 16-bit reload, compare, or capture functions
  - Compare timer for compare/capture functions
- Powerful 16-bit compare/capture unt (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- 10-bit A/D converter
  - 12 multiplexed analog inputs
  - Built-in self calibration
- Extended watchdog facilities
  - 15-bit programmable watchdog timer
  - Oscillator watchdog
- Power saving modes
  - Slow down mode
  - Idle mode (can be combined with slow down mode)
  - Software power-down mode
  - Hardware power-down mode
- 17 interrupt sources (7 external, 10 internal) selectable at 4 priority levels
- P-MQFP-100 and P-LCC-84 packages
- Temperature Ranges : SAB-C517A T_A = 0 to 70 °C
  SAF-C517A T_A = -40 to 85 °C
  SAH-C517A T_A = -40 to 110 °C

Ordering Information

The ordering code for Siemens microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set
- the specified temperature range
- the package and the type of delivery.

For the available ordering codes for the C517A please refer to the
„**Product Information Microcontrollers**“, which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

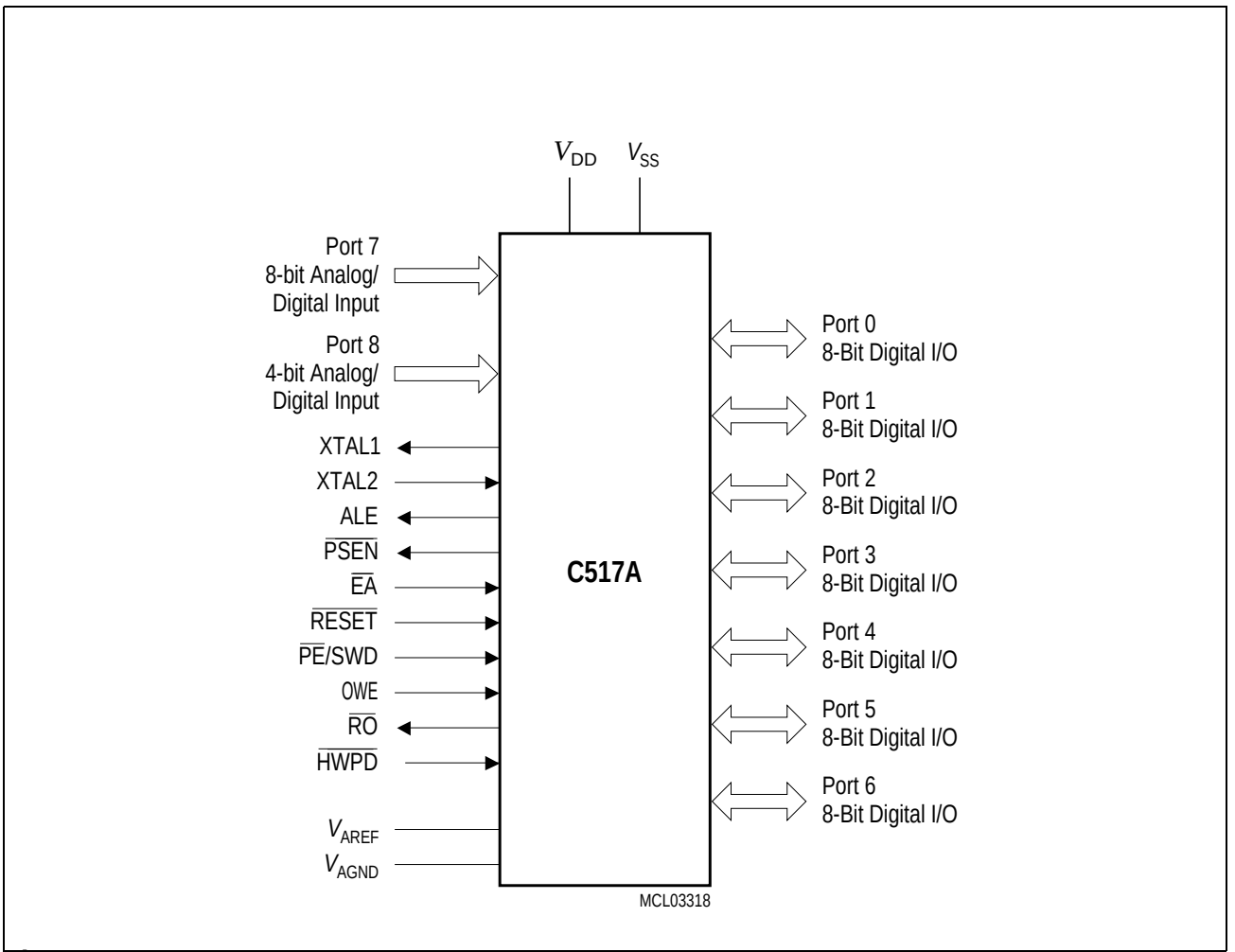


Figure 2
Logic Symbol

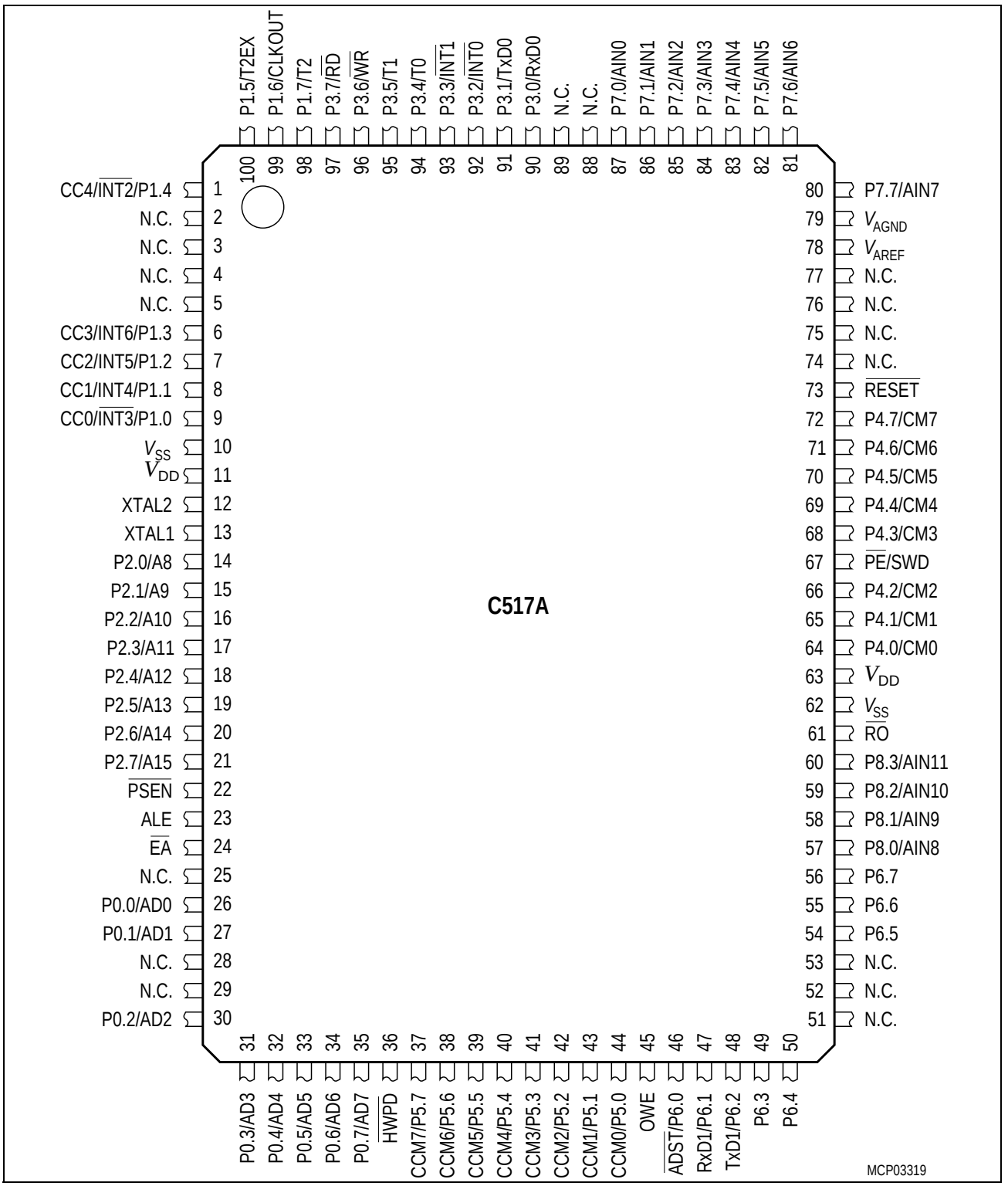


Figure 3
Pin Configuration P-MQFP-100 Package (Top View)

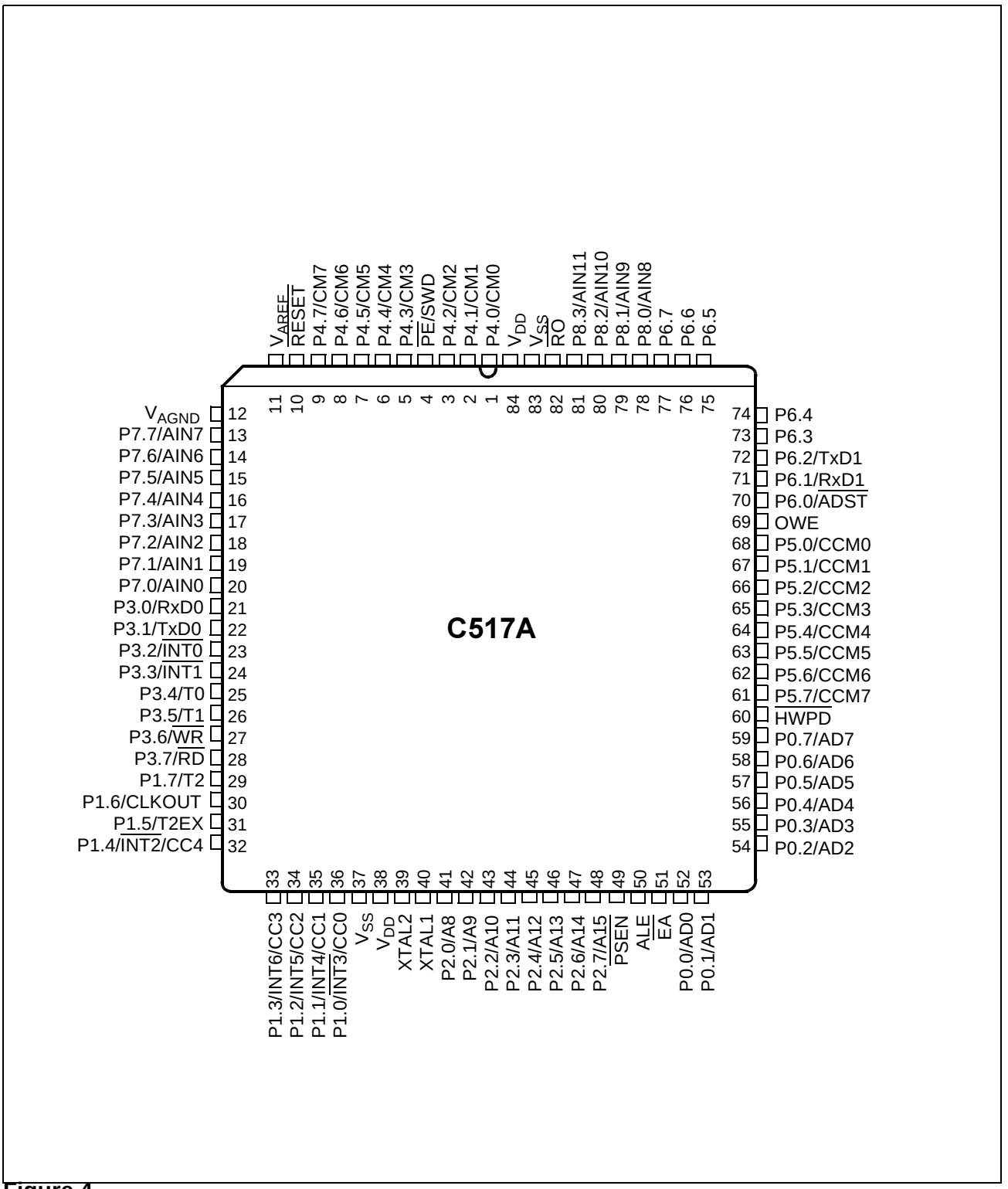


Figure 4
Pin Configuration P-LCC-84 Package (Top View)

Table 1
Pin Definitions and Functions

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
P1.0 - P1.7	9 - 6, 1, 100 - 98	36 - 29	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows :
	9	36		P1.0 / $\overline{\text{INT3}}$ / CC0 Interrupt 3 input / compare 0 output / capture 0 input
	8	35		P1.1 / INT4 / CC1 Interrupt 4 input / compare 1 output / capture 1 input
	7	34		P1.2 / INT5 / CC2 Interrupt 5 input / compare 2 output / capture 2 input
	6	33		P1.3 / INT6 / CC3 Interrupt 6 input / compare 3 output / capture 3 input
	1	32		P1.4 / $\overline{\text{INT2}}$ / CC4 Interrupt 2 input / compare 4 output / capture 4 input
	100	31		P1.5 / T2EX Timer 2 external reload / trigger input
	99	30		P1.6 / CLKOUT System clock output
	98	29		P1.7 / T2 Counter 2 input

*) I = Input,
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
V_{SS}	10, 62	37, 83	–	**Ground** (0V) during normal, idle, and power down operation.
V_{DD}	11, 63	38, 84	–	**Supply voltage** during normal, idle, and power down mode.
XTAL2	12	39	–	**XTAL2** is the input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. Minimum and maximum high and low times as well as rise/ fall times specified in the AC characteristics must be observed.
XTAL1	13	40	–	**XTAL1** is the output of the inverting oscillator amplifier. This pin is used for the oscillator operation with crystal or ceramic resonator.
P2.0 - P2.7	14 - 21	41 - 48	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
$\overline{\text{PSEN}}$	22	49	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. The signal remains high during internal program execution.
ALE	23	50	O	The **Address Latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	24	51	I	**External Access Enable** When held high, the C517A executes instructions from the internal ROM as long as the PC is less than 8000_H. When held low, the C517A fetches all instructions from external program memory. For the C517A-L this pin must be tied low. For the C517A-4R, if the device is protected (see section 4.6 in the User Manual) then this pin is only latched during reset.
P0.0 - P0.7	26, 27, 30 - 35	52 - 59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C517A-4R. External pullup resistors are required during program verification.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
$\overline{\text{HWPD}}$	36	60	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C517A. A low level for a longer period will force the part into hardware power down mode with the pins floating. There is no internal pullup resistor connected to this pin.
P5.0 - P5.7	44 - 37	68 - 61	I/O	**Port 5** is a quasi-bidirectional I/O port with internal pull-up resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. This port also serves the alternate function "Concurrent Compare" and "Set/Reset Compare". The secondary functions are assigned to the port 5 pins as follows: CCM0 to CCM7 P5.0 to P5.7 : concurrent compare or Set/Reset lines
OWE	45	69	I	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watchdog. When left unconnected this pin is pulled high by a weak internal pull-up resisitor. The logic level at OWE should not be changed during normal operation. When held at low level the oscillator watchdog function is turned off. During hardware power down the pullup resistor is switched off.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
P6.0 - P6.7	46 - 50, 54 - 56	70 - 77	I/O	**Port 6** is a quasi-bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 6 also contains the external A/D converter start control pin and the transmit and receive pins for the serial interface 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows : P6.0 $\overline{\text{ADST}}$ external A/D converter start pin P6.1 RxD1 receiver data input of serial interface 1 P6.2 TxD1 transmitter data input of serial interface 1
	46	70		
	47	71		
	48	72		
P8.0 - P8.3	57 - 60	78 - 81	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously. P8.0 - P8.3 AIN8 - AIN11 analog input 8 - 11
$\overline{\text{RO}}$	61	82	O	**$\overline{\text{Reset Output}}$** This pin outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watchdog reset. The $\overline{\text{RO}}$ output signal is active low.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
P4.0 - P4.7	64 - 66, 68 - 72	1 - 3, 5 - 9	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 4 also serves as alternate compare functions. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 4 as follows : P4.0 - P4.7 CM0 - CM7 Compare channel 0 - 7
$\overline{PE}$/SWD	67	4	I	**$\overline{\text{Power saving mode enable}}$ / Start watchdog timer** A low level at this pin allows the software to enter the power saving modes (idle mode, slow down mode, and power down mode). In case the low level is also seen during reset, the watchdog timer function is off on default. Usage of the software controlled power saving modes is blocked, when this pin is held at high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor. During hardware power down the pullup resisitor is switched off.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function	
	P-MQFP-100	P-LCC-84			
P3.0 - P3.7	90 - 97	21 - 28	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:	
	90	21		P3.0 / RxD0	Receiver data input (asynch.) or data input/output (synch.)of serial interface 0
	91	22		P3.1 / TxD0	Transmitter data output (asynch.) or clock output (synch.) of serial interface 0
	92	23		P3.2 / $\overline{\text{INT0}}$	External interrupt 0 input / timer 0 gate control input
	93	24		P3.3 / $\overline{\text{INT1}}$	External interrupt 1 input / timer 1 gate control input
	94	25		P3.4 / T0	Timer 0 counter input
	95	26		P3.5 / T1	Timer 1 counter input
	96	27		P3.6 / $\overline{\text{WR}}$	$\overline{\text{WR}}$ control output; latches the data byte from port 0 into the external data memory
	97	28		P3.7 / $\overline{\text{RD}}$	$\overline{\text{RD}}$ control output; enables the external data memory

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number		I/O*)	Function
	P-MQFP-100	P-LCC-84		
$\overline{\text{RESET}}$	73	10	I	**$\overline{\text{RESET}}$** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the C517A. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	78	11	–	**Reference voltage** for the A/D converter
V_{AGND}	79	12	–	**Reference ground** for the A/D converter
P7.0 - P7.7	87 - 80	20-13	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously. P7.0 - P7.7 AIN0 - AIN7 analog input0 - 7
N.C.	2 - 5, 25, 28, 29, 51 - 53, 74 - 77 88, 89	–	–	**Not connected** These pins of the P-MQFP-100 package must not be connected.

*) I = Input
O = Output

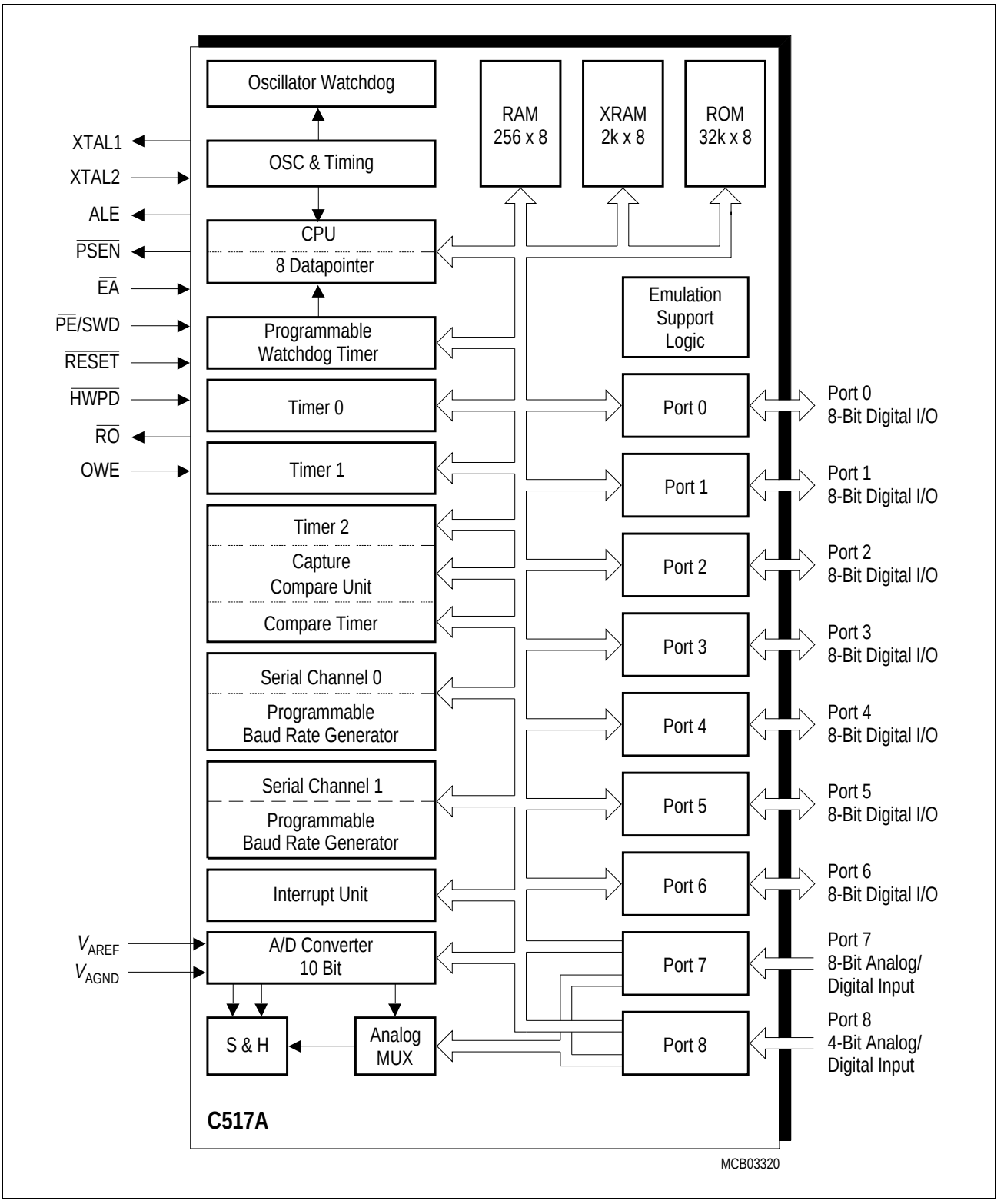


Figure 5
Block Diagram of the C517A

CPU

The C517A is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1µs (24 MHz : 500 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

Memory Organization

The C517A CPU manipulates operands in the following five address spaces:

- up to 64 Kbyte of program memory (32K on-chip program memory for C517A-4R)
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- 2K bytes of internal XRAM data memory
- a 128 byte special function register area

Figure 6 illustrates the memory address spaces of the C517A.

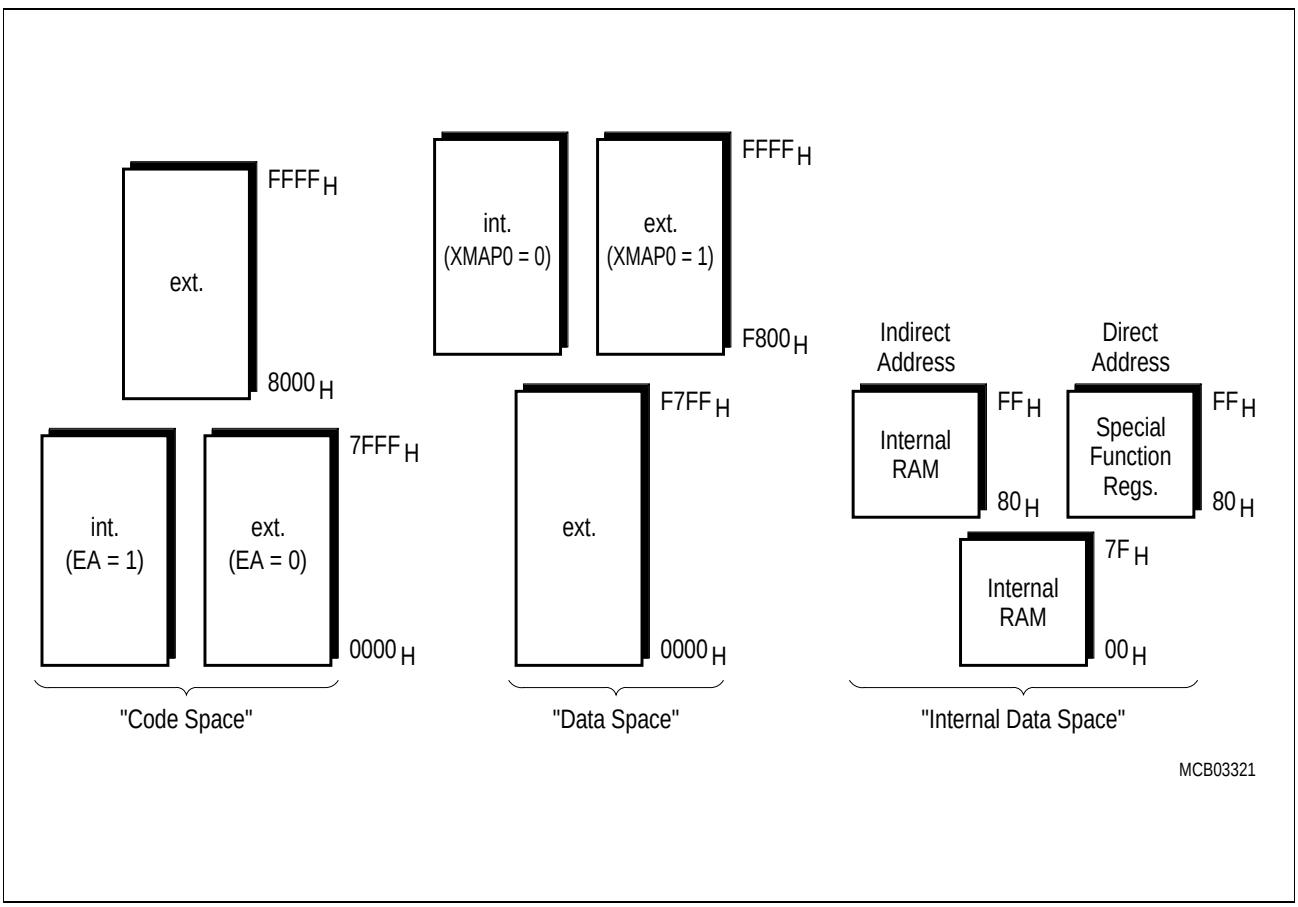


Figure 6
C517A Memory Map

Reset and System Clock

The reset input is an active low input at pin $\overline{\text{RESET}}$. Since the reset is synchronized internally, the $\overline{\text{RESET}}$ pin must be held low for at least two machine cycles (24 oscillator periods) while the oscillator is running. A pullup resistor is internally connected to V_{DD} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the $\overline{\text{RESET}}$ pin to V_{SS} via a capacitor. **Figure 7** shows the possible reset circuitries.

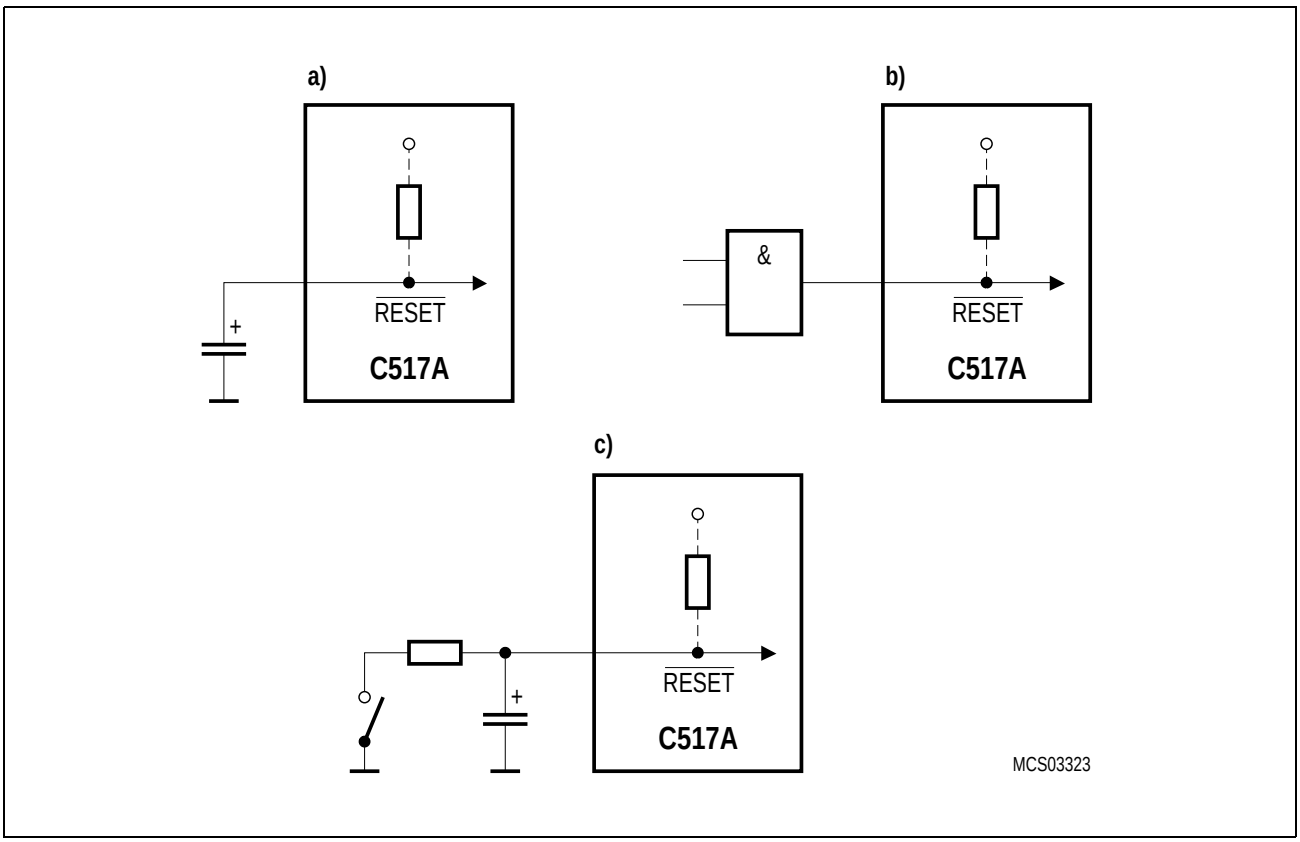


Figure 7
Reset Circuitries

Figure 8 shows the recommended oscillator circiutries for crystal and external clock operation.

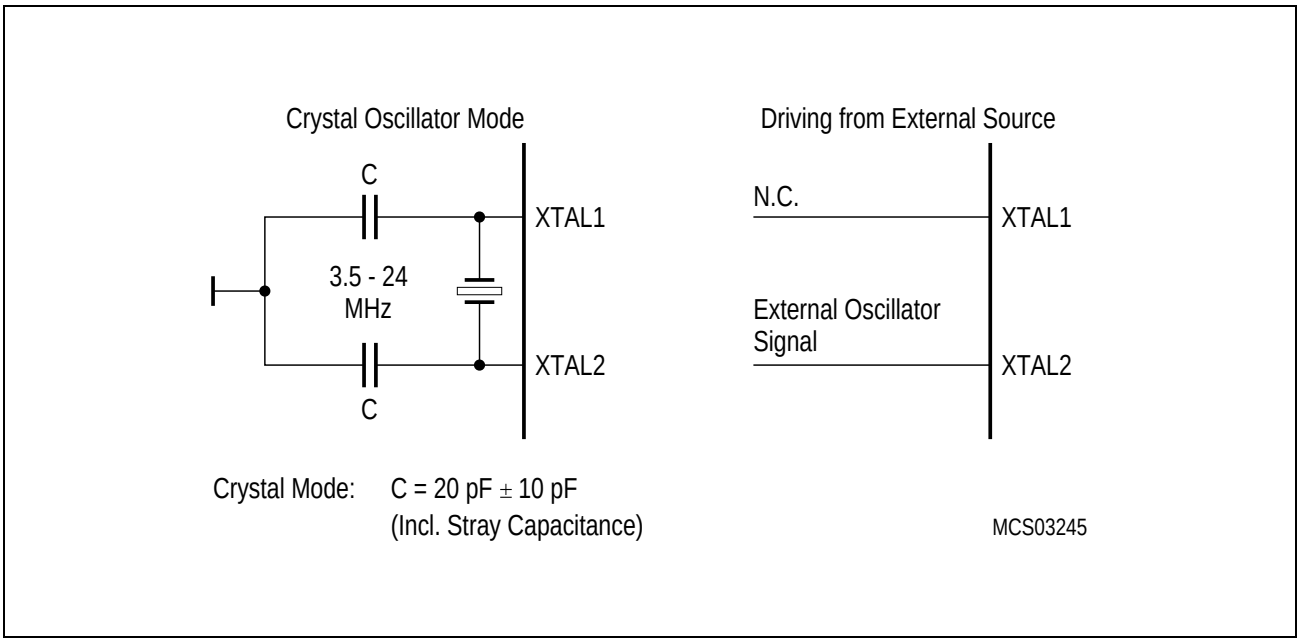


Figure 8
Recommended Oscillator Circuitries

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

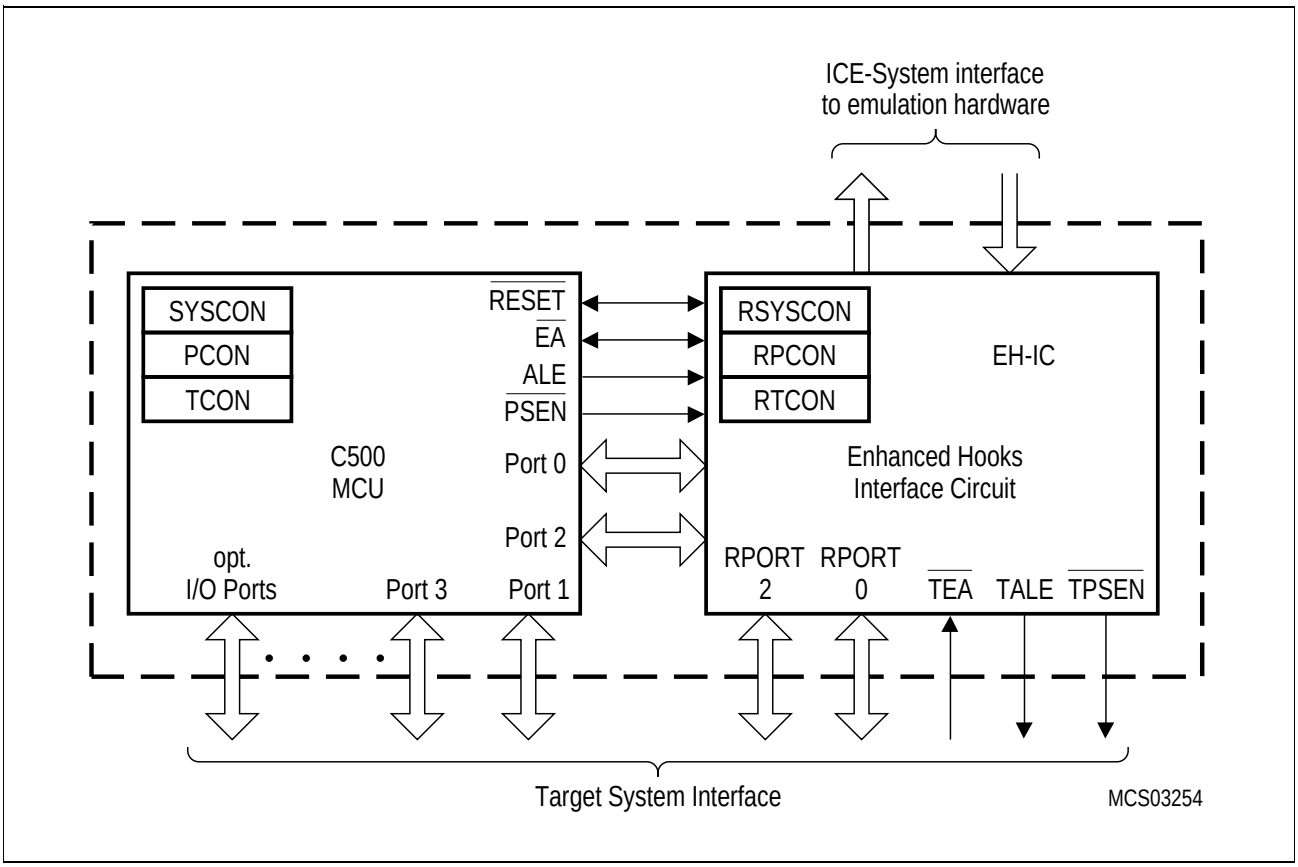


Figure 9
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

1 “Enhanced Hooks Technology“ is a trademark and patent of Metalink Corporation licensed to Siemens.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 94 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All SFRs with addresses where address bits 0-2 are 0 (e

.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable. The SFRs of the C517A are listed in **table 2** and **table 3**. In **table 2** they are organized in groups which refer to the functional blocks of the C517A. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXX\ X000_B$ [3]
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
A/D-Converter	ADCON0 [2]	A/D Converter Control Register 0	**$D8_H$** [1]	00_H
	ADCON1	A/D Converter Control Register 1	DC_H	$0XXX\ 0000_B$ [3]
	ADDATH	A/D Converter Data Register, High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Register, Low Byte	DA_H	$00XX\ XXXX_B$ [3]
Interrupt System	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IEN2	Interrupt Enable Register 2	$9A_H$	$XX00\ 00X0_B$ [3]
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX00\ 0000_B$ [3]
	IRCON0 [2]	Interrupt Request Control Register 0	**$C0_H$** [1]	00_H
	IRCON1	Interrupt Request Control Register 1	$D1_H$	00_H
	TCON [2]	Timer 0/1 Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	00_H
	S0CON [2]	Serial Channel 0 Control Register	**98_H** [1]	00_H
	CTCON [2]	Compare Timer Control Register	$E1_H$	$0X00\ 0000_B$ [3]
MUL/DIV Unit	ARCON	Arithmetic Control Register	EF_H	$0XXXXXXX_B$ [3]
	MD0	Multiplication/Division Register 0	$E9_H$	XX_H [3]
	MD1	Multiplication/Division Register 1	EA_H	XX_H [3]
	MD2	Multiplication/Division Register 2	EB_H	XX_H [3]
	MD3	Multiplication/Division Register 3	EC_H	XX_H [3]
	MD4	Multiplication/Division Register 4	ED_H	XX_H [3]
	MD5	Multiplication/Division Register 5	EE_H	XX_H [3]
Timer 0 / Timer 1	TCON [2]	Timer 0/1 Control Register	**88_H** [1]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X“ means that the value is undefined and the location is reserved

Table 2
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Compare/ Capture Unit (CCU) Timer 2	CCEN	Compare/Capture Enable Register	$C1_H$	00_H
	CC4EN	Compare/Capture 4 Enable Register	$C9_H$	00_H
	CCH1	Compare/Capture Register 1, High Byte	$C3_H$	00_H
	CCH2	Compare/Capture Register 2, High Byte	$C5_H$	00_H
	CCH3	Compare/Capture Register 3, High Byte	$C7_H$	00_H
	CCH4	Compare/Capture Register 4, High Byte	CF_H	00_H
	CCL1	Compare/Capture Register 1, Low Byte	$C2_H$	00_H
	CCL2	Compare/Capture Register 2, Low Byte	$C4_H$	00_H
	CCL3	Compare/Capture Register 3, Low Byte	$C6_H$	00_H
	CCL4	Compare/Capture Register 4, Low Byte	CE_H	00_H
	CMEN	Compare Enable Register	$F6_H$	00_H
	CMH0	Compare Register 0, High Byte	$D3_H$	00_H
	CMH1	Compare Register 1, High Byte	$D5_H$	00_H
	CMH2	Compare Register 2, High Byte	$D7_H$	00_H
	CMH3	Compare Register 3, High Byte	$E3_H$	00_H
	CMH4	Compare Register 4, High Byte	$E5_H$	00_H
	CMH5	Compare Register 5, High Byte	$E7_H$	00_H
	CMH6	Compare Register 6, High Byte	$F3_H$	00_H
	CMH7	Compare Register 7, High Byte	$F5_H$	00_H
	CML0	Compare Register 0, Low Byte	$D2_H$	00_H
	CML1	Compare Register 1, Low Byte	$D4_H$	00_H
	CML2	Compare Register 2, Low Byte	$D6_H$	00_H
	CML3	Compare Register 3, Low Byte	$E2_H$	00_H
	CML4	Compare Register 4, Low Byte	$E4_H$	00_H
	CML5	Compare Register 5, Low Byte	$E6_H$	00_H
	CML6	Compare Register 6, Low Byte	$F2_H$	00_H
	CML7	Compare Register 7, Low Byte	$F4_H$	00_H
	CMSEL	Compare Input Select	$F7_H$	00_H
	CRCH	Comp./Rel./Capt. Register High Byte	CB_H	00_H
	CRCL	Comp./Rel./Capt. Register Low Byte	CA_H	00_H
	COMSETL	Compare Set Register Low Byte	$A1_H$	00_H
	COMSETH	Compare Set Register, High Byte	$A2_H$	00_H
	COMCLRL	Compare Clear Register, Low Byte	$A3_H$	00_H
	COMCLRH	Compare Clear Register, High Byte	$A4_H$	00_H
	SETMSK	Compare Set Mask Register	$A5_H$	00_H
	CLRMSK	Compare Clear Mask Register	$A6_H$	00_H
	CTCON [2]	Compare Timer Control Register	$E1_H$	$0X00\ 0000_B$ [3]
	CTRELH	Compare Timer Rel. Register, High Byte	DF_H	00_H
	CTRELL	Compare Timer Rel. Register, Low Byte	DE_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	00_H
	IRCON0 [2]	Interrupt Request Control Register 0	**$C0_H$** [1]	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved

Table 2
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P4	Port 4	**$E8_H$** 1)	FF_H
	P5	Port 5	**$F8_H$** 1)	FF_H
	P6	Port 6	FA_H	FF_H
	P7	Port 7, Analog/Digital Input	DB_H	–
	P8	Port 8, Analog/Digital Input, 4-bit	DD_H	–
XRAM	XPAGE	Page Address Register for Extended On-Chip RAM	91_H	00_H
	SYSCON 2)	System/XRAM Control Register	$B1_H$	XXXX $XX01_B$ 3)
Serial Channels	ADCON0 2)	A/D Converter Control Register	**$D8_H$** 1)	**00_H**
	PCON 2)	Power Control Register	87_H	00_H
	S0BUF	Serial Channel 0 Buffer Register	99_H	XX_H 3)
	S0CON	Serial Channel 0 Control Register	**98_H** 1)	**00_H**
	S0RELL	Serial Channel 0 Reload Reg., Low Byte	AA_H	$D9_H$
	S0RELH	Serial Channel 0 Reload Reg., High Byte	BA_H	XXXX $XX11_B$ 3)
	S1BUF	Serial Channel 1 Buffer Register	$9C_H$	XX_H 3)
	S1CON	Serial Channel 1 Control Register	$9B_H$	0X00 0000_B 3)
	S1RELL	Serial Channel 1 Reload Reg., Low Byte	$9D_H$	00_H
	S1RELH	Serial Channel 1 Reload Reg., High Byte	BB_H	XXXX $XX11_B$ 3)
Watchdog	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
	WDTREL	Watchdog Timer Reload Register	86_H	00_H
Pow. Sav. Modes	PCON 2)	Power Control Register	87_H	00_H

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved.

Table 3
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	WDTREL	00_H	WDT-PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	T2	CLK-OUT	T2EX	$\overline{INT2}$	INT6	INT5	INT4	$\overline{INT3}$
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	XXXX-X000_B	–	–	–	–	–	.2	.1	.0
98_H [2)]	S0CON	00_H	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0
99_H	S0BUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9A_H$	IEN2	XX00-00X0_B	–	–	ECR	ECS	ECT	ECMP	–	ES1
$9B_H$	S1CON	0X00-0000$_B$	SM	–	SM21	REN1	TB81	RB81	TI1	RI1
$9C_H$	S1BUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9D_H$	S1RELL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A1_H$	COMSETL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A2_H$	COMSETH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A3_H$	COMCLRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Shaded registers are bit-addressable special function registers

Table 3
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$A4_H$	COMCLRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A5_H$	SETMSK	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A6_H$	CLRMSK	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$[2)]	IEN0	00_H	EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA_H	S0RELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0
$B0_H$[2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
$B1_H$	SYSCON	XXXX-$XX01_B$	–	–	–	–	–	–	XMAP1	XMAP0
$B8_H$[2)]	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
$B9_H$	IP1	XX00-0000_B	–	–	.5	.4	.3	.2	.1	.0
BA_H	S0RELH	XXXX-$XX11_B$	–	–	–	–	–	–	.1	.0
BB_H	S1RELH	XXXX-$XX11_B$	–	–	–	–	–	–	.1	.0
$C0_H$[2)]	IRCON0	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	00_H	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
$C9_H$	CC4EN	00_H	COCOEN1	COCON2	COCON1	COCON0	COCOEN0	COCAH4	COCAL4	COMO

1) X means that the value is undefined and the location is reserved
2) Shaded registers are bit-addressable special function registers

Table 3
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CE_H	CCL4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CF_H	CCH4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$ [2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D1_H$	IRCON1	00_H	ICMP7	ICMP6	ICMP5	ICMP4	ICMP3	ICMP2	ICMP1	ICMP0
$D2_H$	CML0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D3_H$	CMH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D4_H$	CML1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CMH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D6_H$	CML2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D7_H$	CMH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D8_H$ [2)]	ADCON0	00_H	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DB_H	P7	–	.7	.6	.5	.4	.3	.2	.1	.0
DC_H	ADCON1	$0XXX\text{-}0000_B$	ADCL	–	–	–	MX3	MX2	MX1	MX0
DD_H	P8	–	–	–	–	–	.3	.2	.1	.0
DE_H	CTRELL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
DF_H	CTRELH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E0_H$ [2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E1_H$	CTCON	$0X00.0000_B$	T2PS1	–	ICR	ICS	CTF	CLK2	CLK1	CLK0
$E2_H$	CML3	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Shaded registers are bit-addressable special function registers

Table 3
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$E3_H$	CMH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E4_H$	CML4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E5_H$	CMH4	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E6_H$	CML5	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E7_H$	CMH5	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	FF_H	CM7	CM6	CM5	CM4	CM3	CM2	CM1	CM0
$E9_H$	MD0	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EA_H	MD1	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EB_H	MD2	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EC_H	MD3	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
ED_H	MD4	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EE_H	MD5	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
EF_H	ARCON	$0XXX.XXXX_B$	MDEF	MDOV	SLR	SC.4	SC.3	SC.2	SC.1	SC.0
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F2_H$	CML6	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F3_H$	CMH6	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F4_H$	CML7	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F5_H$	CMH7	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F6_H$	CMEN	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7_H$	CMSEL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	P5	FF_H	CCM7	CCM6	CCM5	CCM4	CCM3	CCM2	CCM1	CCM0
FA_H	P6	FF_H	.7	.6	.5	.4	.3	TxD1	RxD1	ADST

1) X means that the value is undefined and the location is reserved
2) Shaded registers are bit-addressable special function registers

Digital I/O Ports

The C517A allows for digital I/O on 56 lines grouped into 7 bidirectional 8-bit ports. Each port bit consists of a latch, an output driver and an input buffer. Read and write accesses to the I/O ports P0 through P6 are performed via their corresponding special function registers P0 to P6.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents.

Analog Input Ports

Ports 7 (8-bit) and 8 (4-bit) are input ports only and provide two functions. When used as digital inputs, the corresponding SFR P7 and P8 contains the digital value applied to the port 7/8 lines. When used for analog inputs the desired analog channel is selected by a four-bit field in SFR ADCON1. Of course, it makes no sense to output a value to these input-only ports by writing to the SFR P7 or P8. This will have no effect.

If a digital value is to be read, the voltage levels are to be held within the input voltage specifications (V_{IL}/V_{IH}). Since P7 and P8 are not bit-addressable, all input lines of P7 and P8 are read at the same time by byte instructions.

Nevertheless, it is possible to use port 7 and 8 simultaneously for analog and digital input. However, care must be taken that all bits of P7 and P8 that have an undetermined value caused by their analog function are masked.

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4** :

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{OSC}/12x32	f_{OSC}/24x32
1	16-bit timer/counter	1	1	f_{OSC}/12	f_{OSC}/24
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is f_{OSC}/12.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{OSC}/24. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

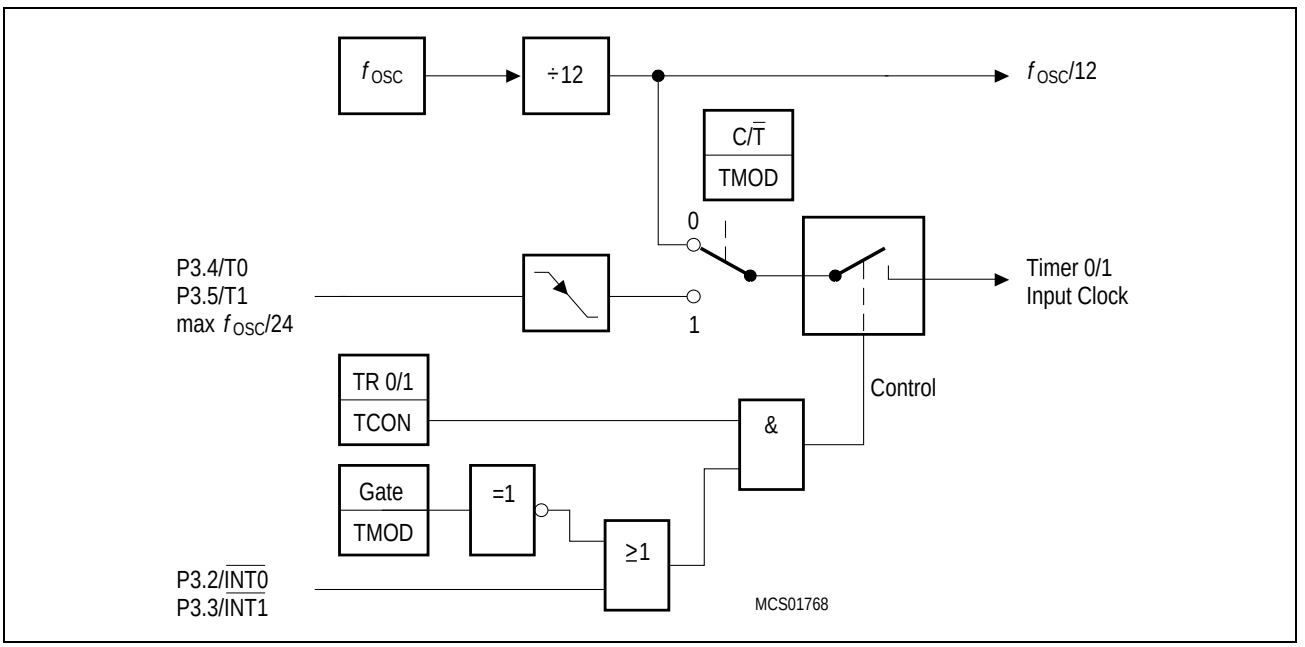


Figure 10
Timer/Counter 0 and 1 Input Clock Logic

Cpmpare / Capture Unit (CCU)

The compare/capture unit is one of the C517A's most powerful peripheral units for use in all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. The CCU consists of two 16-bit timer/counters with automatic reload feature and an array of 13 compare or compare/capture registers. A set of six control registers is used for flexible adapting of the CCU to a wide variety of user's applications.

The block diagram in **figure 11** shows the general configuration of the CCU. All CC1 to CC4 registers and the CRC register are exclusively assigned to timer 2. Each of the eight compare registers CM0 through CM7 can either be assigned to timer 2 or to the faster compare timer, e.g. to provide up to 8 PWM output channels. The assignment of the CMx registers - which can be done individually for every single register - is combined with an automatic selection of one of the two possible compare modes.

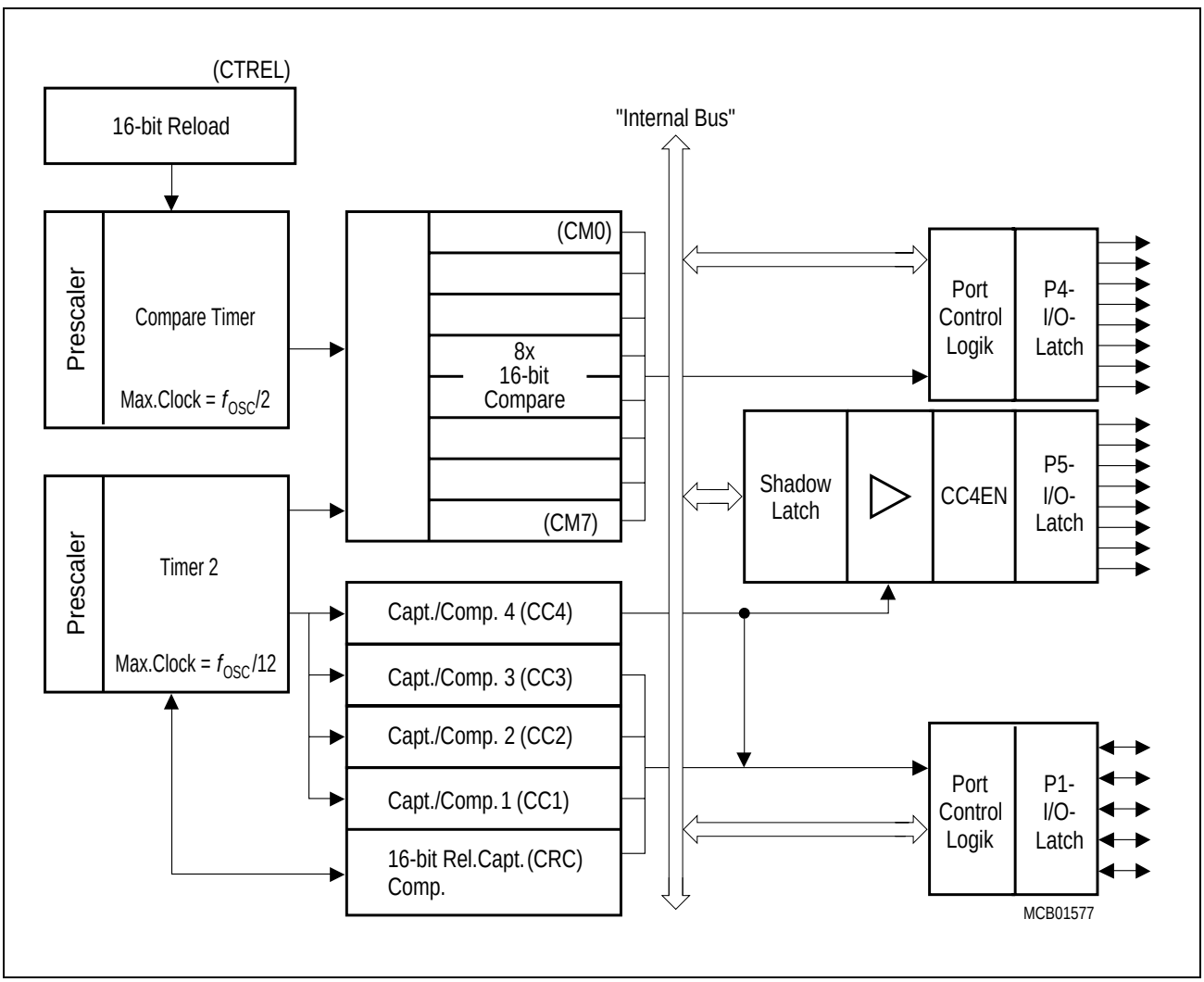


Figure 11
Timer 2 Block Diagram

The main functional blocks of the CCU are :

- Timer 2 with $f_{OSC}/12$ input clock, 2-bit prescaler, 16-bit reload, counter/gated timer mode and overflow interrupt request.
- Compare timer with $f_{OSC}/2$ input clock, 3-bit prescaler, 16-bit reload and overflow interrupt request.
- Compare/(reload/)capture register array consisting of four different kinds of registers:
  one 16-bit compare/reload/capture register,
  three 16-bit compare/capture registers,
  one 16-bit compare/capture register with additional "concurrent compare" feature,
  eight 16-bit compare registers with timer-overflow controlled loading.

Table 5 shows the possible configurations of the CCU and the corresponding compare modes which can be selected. The following sections describe the function of these configurations.

Table 5
CCU Configurations

Assigned Timer	Compare Register	Compare Output at	Possible Modes
Timer 2	CRCH/CRCL CCH1/CCL1 CCH2/CCL2 CCH3/CCL3 CCH4/CCL4	P1.0/$\overline{\text{INT3}}$/CC0 P1.1/INT4/CC1 P1.2/INT5/CC2 P1.3/INT6/CC3 P1.4/$\overline{\text{INT2}}$/CC4	Compare mode 0, 1 + Reload Compare mode 0, 1 / capture Compare mode 0, 1 / capture Compare mode 0, 1 / capture Compare mode 0, 1 / capture
	CCH4/CCL4	P1.4/$\overline{\text{INT2}}$/CC4 P5.0/CCM0 to P5.7/CCM7	Compare mode 1 “Concurrent compare“
	CMH0/CML0 to CMH7/CML7	P4.0/CM0 to P4.7/CM7	Compare mode 0
	COMSET COMCLR	P5.0/CCM0 to P5.7/CCM7	Compare mode 2
Compare Timer	CMH0/CML0 to CMH7/CML7	P4.0/CM0 to P4.7/CM7	Compare mode 1

Timer 2 Operation

Timer Mode : In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/12 or 1/24 of the oscillator frequency.

Gated Timer Mode : In gated timer function, the external input pin P1.7/T2 operates as a gate to the input of timer 2. lf T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. The external gate signal is sampled once every machine cycle.

Event Counter Mode : In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin P1.7/T2. In this function, the external input is sampled every machine cycle. The maximum count rate is 1/24 of the oscillator frequency.Reload of Timer 2 : Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.
In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX.

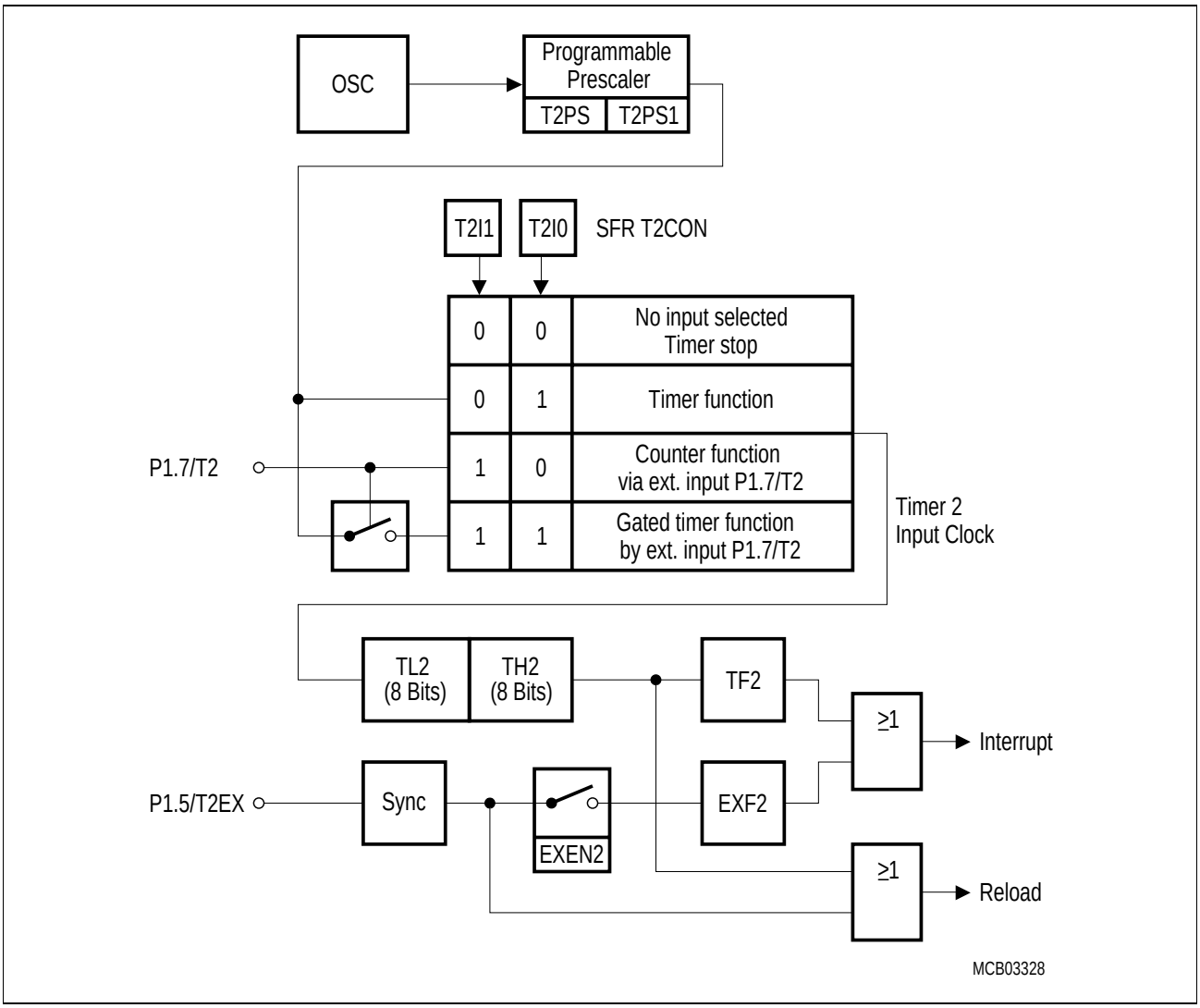


Figure 12
Block Diagram of Timer 2

Compare Timer Operation

The compare timer receives its input clock from a programmable prescaler which provides input frequencies, ranging from $f_{OSC}/2$ up to $f_{OSC}/256$. The compare timer is, once started, a free-running 16-bit timer, which on overflow is automatically reloaded by the contents of a 16-bit reload register. The compare timer has - as any other timer in the C517A - their own interrupt request flags CTF. These flags are set when the timer count rolls over from all ones to the reload value. **Figure 13** shows the block diagram of compare timer and compare timer 1.

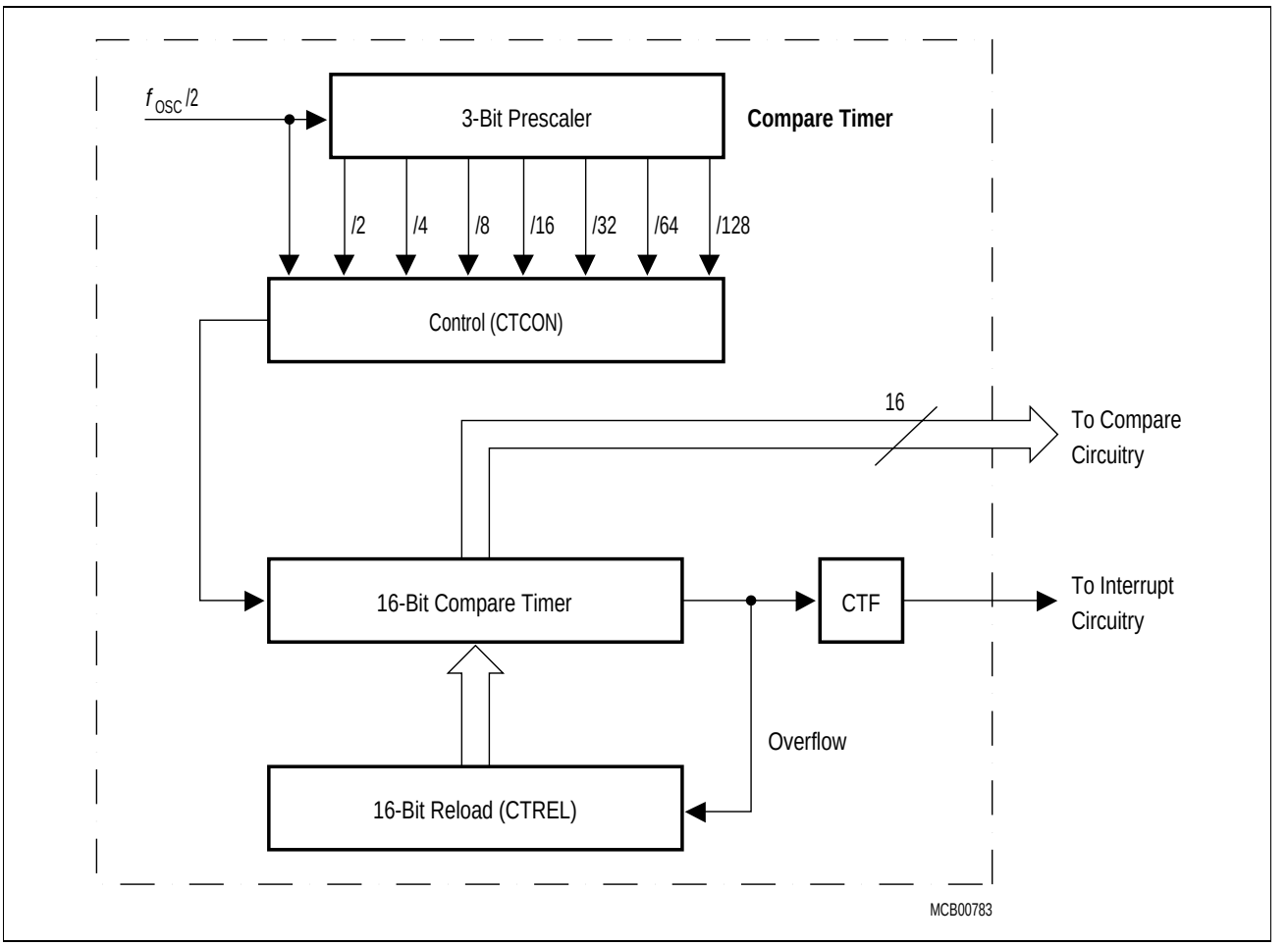


Figure 13
Compare Timer Block Diagram

Compare Modes

The compare function of a timer/register combination operates as follows : the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 14** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

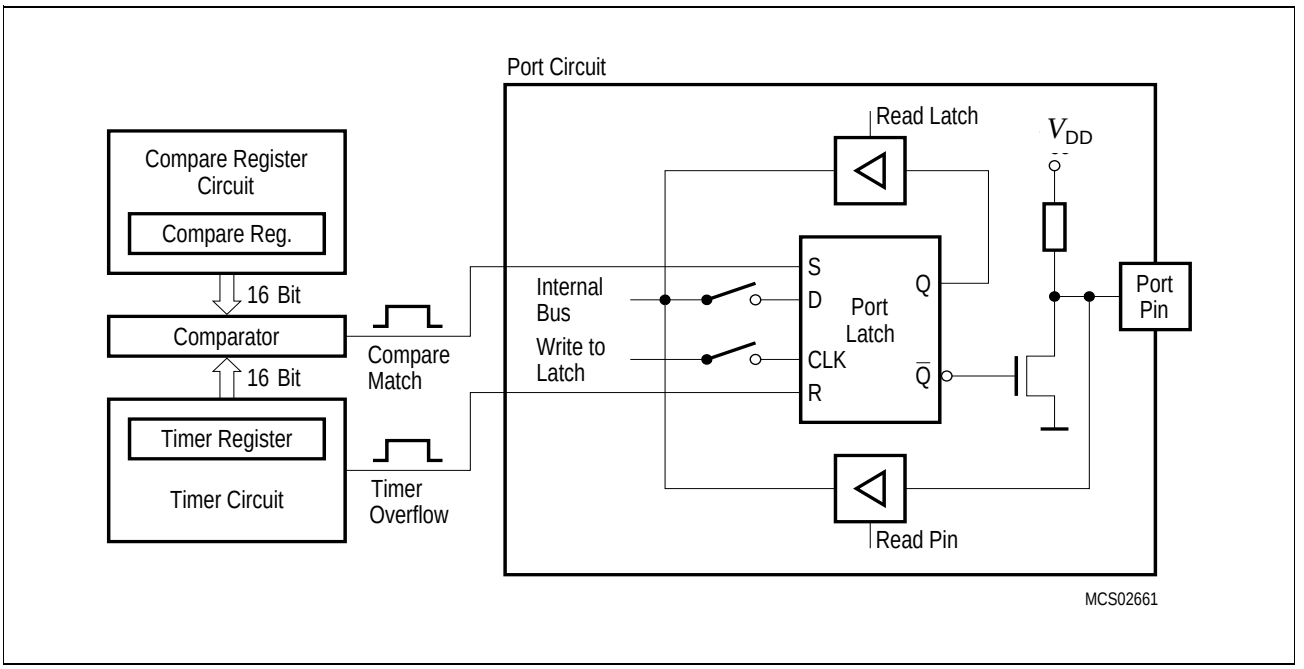


Figure 14
Port Latch in Compare Mode 0

Compare Mode 1

If compare mode 1 is enabled and the software writes to the appropriate output latch at the port, the new value will not appear at the output pin until the next compare match occurs. Thus, it can be choosen whether the output signal has to make a new transition (1-to-0 or 0-to-1, depending on the actual pin-level) or should keep its old value at the time when the timer value matches the stored compare value.

In compare mode 1 (see **figure 15**) the port circuit consists of two separate latches. One latch (which acts as a "shadow latch") can be written under software control, but its value will only be transferred to the port latch (and thus to the port pin) when a compare match occurs.

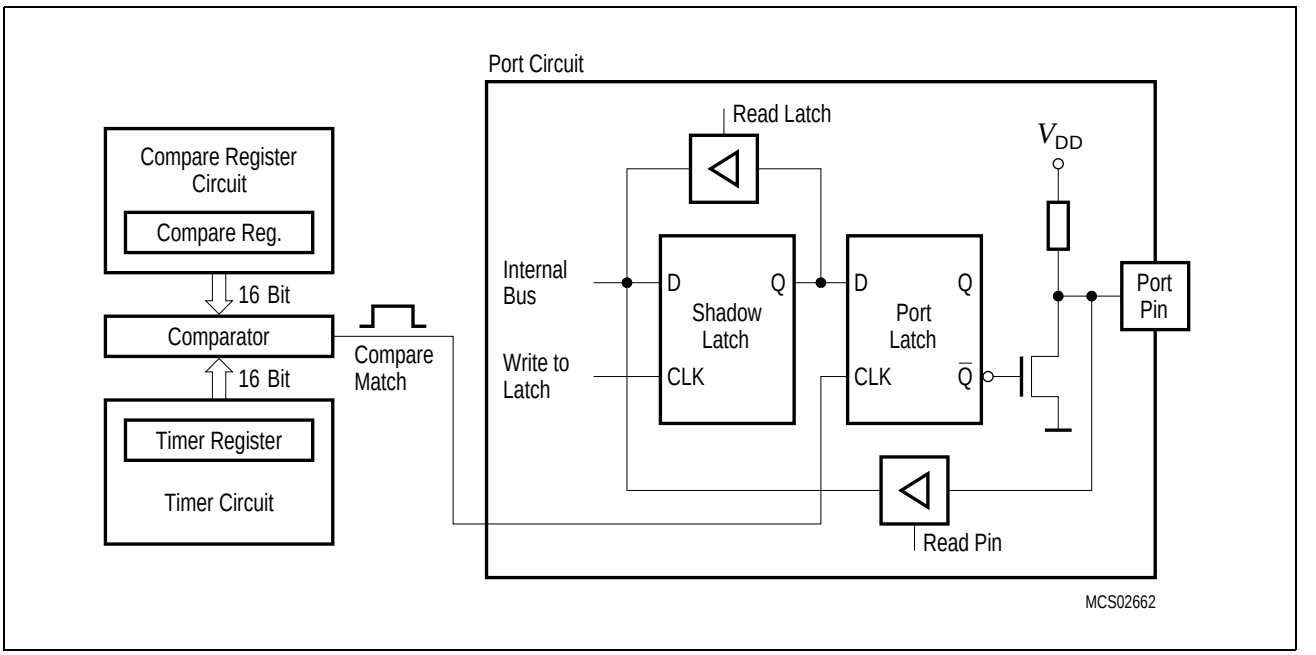


Figure 15
Compare Function in Compare Mode 1

Compare Mode 2

In the compare mode 2 the port 5 pins are under control of compare/capture register CC4, but under control of the compare registers COMSET and COMCLR. When a compare match occurs with register COMSET, a high level appears at the pins of port 5 when the corresponding bits in the mask register SETMSK are set. When a compare match occurs with register COMCLR, a low level appears at the pins of port 5 when the corresponding bits in the mask register CLRMSK are set.

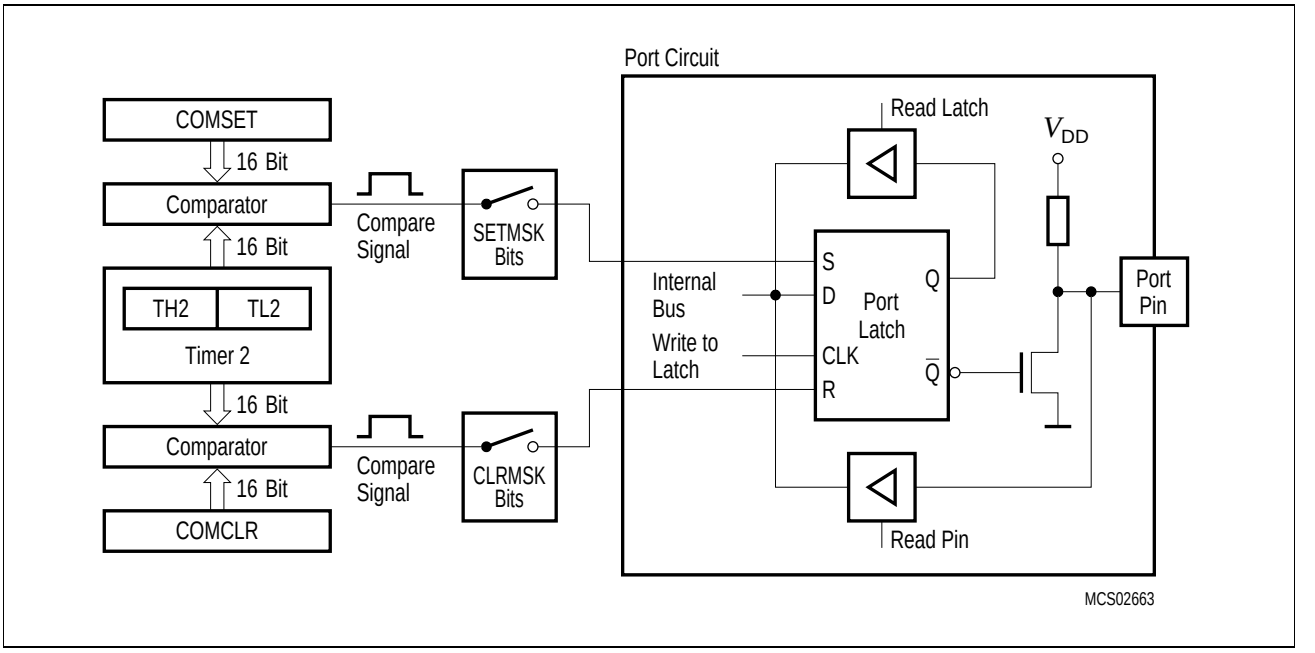


Figure 16
Compare Function of Compare Mode 2

Multiplication / Division Unit (MDU)

This on-chip arithmetic unit of the C517A provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are unsigned integer operations. **Table 6** describes the five general operations the MDU is able to perform.

Table 6
MDU Operation Characteristics

Operation	Result	Remainder	Execution Time
32bit/16bit	32bit	16bit	6 t_{CY} 1)
16bit/16bit	16bit	16bit	4 t_{CY} 1)
16bit x 16bit	32bit	–	4 t_{CY} 1)
32-bit normalize	–	–	6 t_{CY} 2)
32-bit shift L/R	–	–	6 t_{CY} 2)

1) 1 t_{CY} = 12 t_{CLCL}= 1 machine cycle = 500 ns at 24 MHz oscillator frequency
2) The maximal shift speed is 6 shifts per machine cycle

The MDU consists of seven special function registers (MD0-MD5, ARCON) which are used as operand, result, and control registers. The three operation phases are shown in **figure 17**.

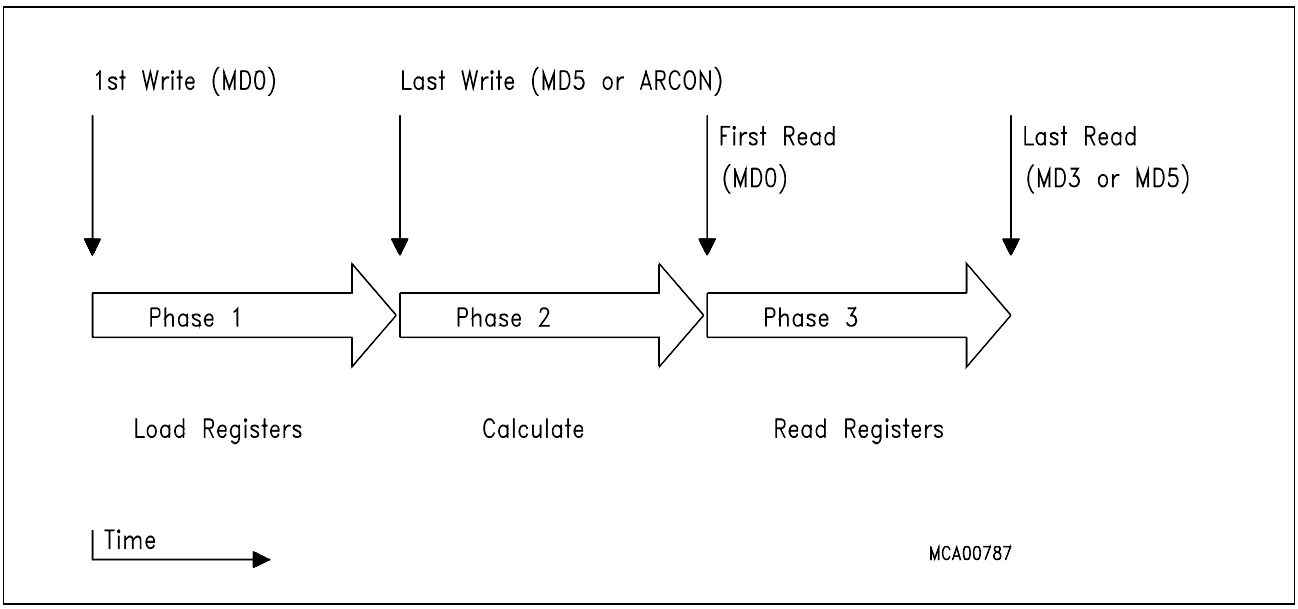


Figure 17
Operating Phases of the MDU

For starting an operation, registers MD0 to MD5 and ARCON must be written to in a certain sequence according **table 7** and **8**. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to SFR ARCON.

Table 7
Programming the MDU for Multiplication and Division

Operation	32Bit/16Bit		16Bit/16Bit		16Bit x 16Bit	
First Write	MD0	D'endL	MD0	D'endL	MD0	M'andL
	MD1	D'end	MD1	D'endH	MD4	M'orL
	MD2	D'end				
	MD3	D'endH	MD4	D'orL	MD1	M'andH
	MD4	D'orL				
Last Write	MD5	D'orH	MD5	D'orH	MD5	M'orH
First Read	MD0	QuoL	MD0	QuoL	MD0	PrL
	MD1	Quo	MD1	QuoH	MD1	
	MD2	Quo				
	MD3	QuoH	MD4	RemL	MD2	
	MD4	RemL				
Last Read	MD5	RemH	MD5	RemH	MD3	PrH

Abbrevations :

D'end	:	Dividend, 1st operand of division
D'or	:	Divisor, 2nd operand of division
M'and	:	Multiplicand, 1st operand of multiplication
M'or	:	Multiplicator, 2nd operand of multiplication
Pr	:	Product, result of multiplication
Rem	:	Remainder
Quo	:	Quotient, result of division
...L	:	means, that this byte is the least significant of the 16-bit or 32-bit operand
...H	:	means, that this byte is the most significant of the 16-bit or 32-bit operand

Table 8
Programming athe MDU for a Shift or Normalize Operation

Operation	Normalize, Shift Left, Shift Right	
First write	MD0	least significant byte
	MD1	.
	MD2	.
	MD3	most significant byte
Last write	ARCON	start of conversion
First read	MD0	least significant byte
	MD1	.
	MD2	.
Last read	MD3	most significant byte

Serial Interfaces 0 and 1

The C517A has two serial interfaces which are functionally nearly identical concerning the asynchronous modes of operation. The two channels are full-duplex, meaning they can transmit and receive simultaneously. The serial channel 0 is completely compatible with the serial channel of the C501 (one synchronous mode, three asynchronous modes). Serial channel 1 has the same functionality in its asynchronous modes, but the synchronous mode and the fixed baud rate UART mode is missing.

The operating modes of the serial interfaces is illustrated in **table 9**. The possible baudrates can be calculated using the formulas given in **table 10**.

Table 9
Operating Modes of Serial Interface 0 and 1

Serial Interface	Mode	S0CON		S1CON	Description
		SM0	SM1	SM	
0	0	0	0	–	Shift register mode Serial data enters and exits through R×D0; T×D0 outputs the shift clock; 8-bit are transmitted/received (LSB first); fixed baud rate
	1	0	1	–	8-bit UART, variable baud rate 10 bits are transmitted (through T×D0) or received (at R×D0)
	2	1	0	–	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D0) or received (at R×D0)
	3	1	1	–	9-bit UART, variable baud rate Like mode 2
1	A	–	–	0	9-bit UART; variable baud rate 11 bits are transmitted (through T×D1) or received (at R×D1)
	B	–	–	1	8-bit UART; variable baud rate 10 bits are transmitted (through T×D1) or received (at R×D1)

For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **figure 18** and **figure 19**) to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface 0 can be derived from either timer 1 or a decdicated baud rate generator (see **figure 18**). The variable baud rates for modes A and B of the serial interface 1 are derived from a decdicated baud rate generator as shown in **figure 19**.

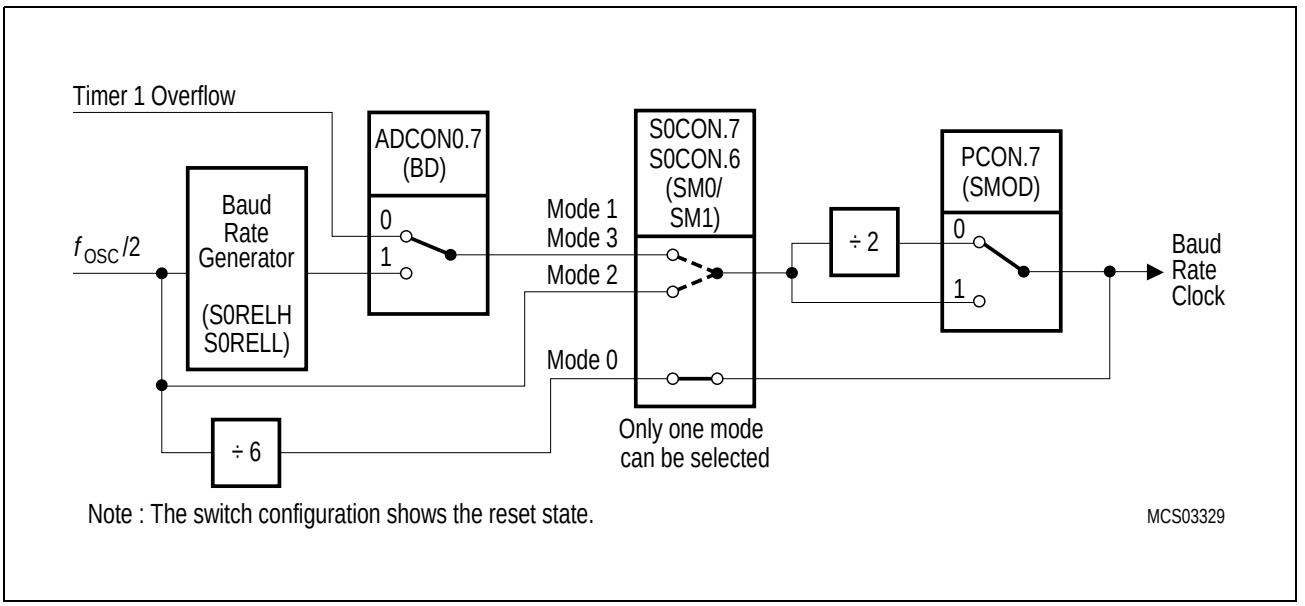


Figure 18
Serial Interface 0 : Baud Rate Generation Configuration

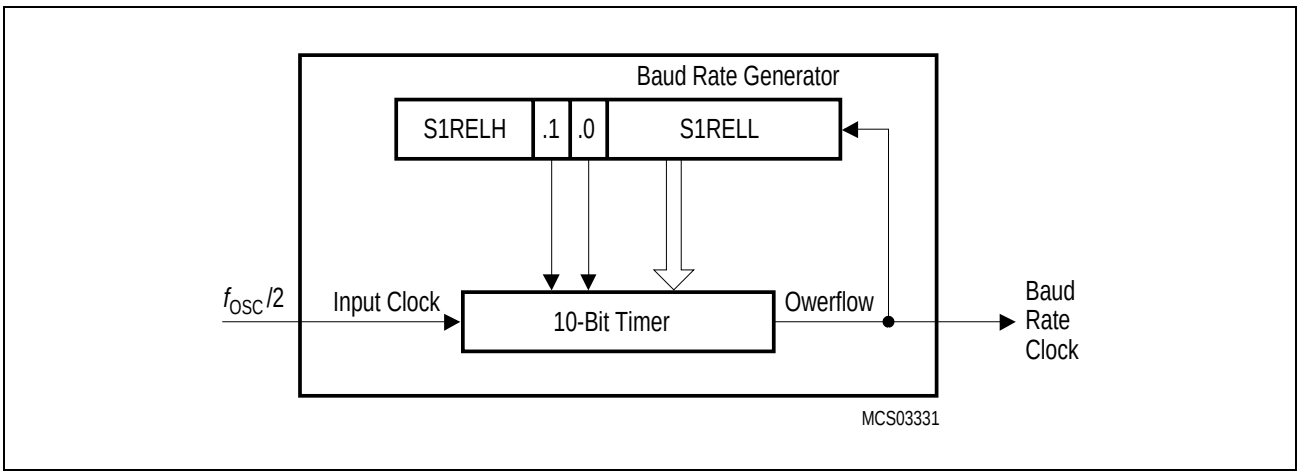


Figure 19
Serial Interface 1 : Baud Rate Generator Configuration

The baud rate generator block in **figure 18** has the same structure (10-bit auto-reload timer) as the baud rate generator block which is shown in detail in **figure 19**.

Table 10 below lists the values/formulas for the baud rate calculation of serial interface 0 and 1 with its dependencies of the control bits BD and SMOD.

Table 10
Serial Interfaces - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rates
	SMOD	BD	
Mode 0 (Shift Register)	–	–	Fixed baud rate clock fosc/12
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	X	0	Timer 1 overflow is used for baud rate generation; SMOD controls a divide-by-2 option. Baud rate = 2^{SMOD} x timer 1 overflow rate / 32
		1	Baud rate generator is used for baud rate generation; SMOD controls a divide-by-2 option Baud rate = 2^{SMOD} x oscillator frequency / 64 x (baud rate gen. overflow rate)
Mode 2 (9-bit UART)	X	–	Fixed baud rate clock fosc/32 (SMOD=1) or fosc/ 64 (SMOD=0)
Mode A (9-bit UART) Mode B (8-bit UART)	–	–	Baud rate generator is used for baud rate generation; SMOD controls a divide-by-2 option Baud rate = oscillator frequency / 32 x (baud rate gen. overflow rate)

10-Bit A/D Converter

The C517A provides an A/D converter with the following features:

- 12 multiplexed input channels (port 7, 8), which can also be used as digital inputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal or external start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The A/D converter operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The externally applied reference voltage range has to be held on a fixed value within the specifications. The main functional blocks of the A/D converter are shown in **figure 20**.

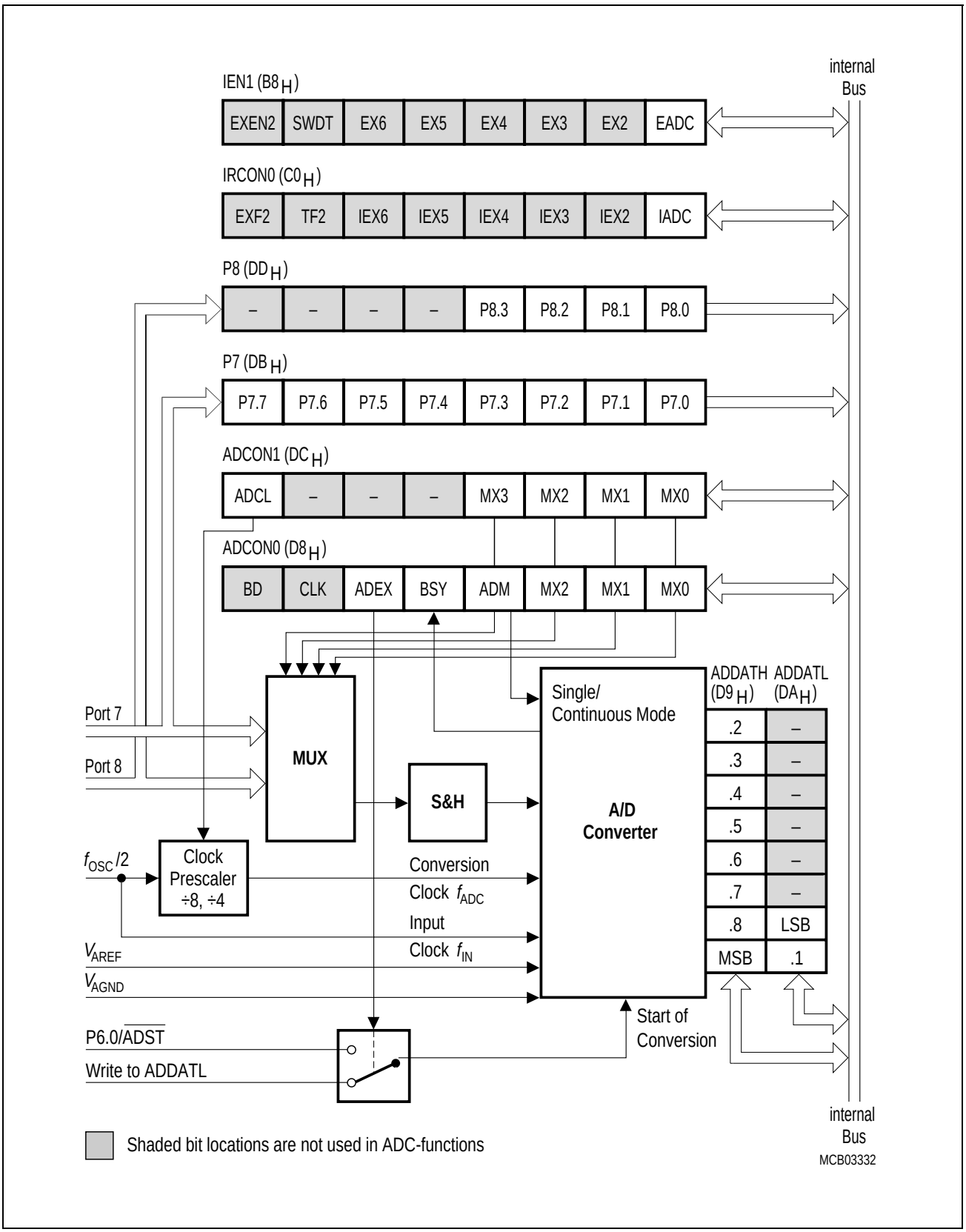


Figure 20
A/D Converter Block Diagram

Interrupt System

The C517A provides 17 interrupt sources with four priority levels. Ten interrupts can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, compare timer, compare match/set/clear, A/D converter, and serial interface 0 and 1) and seven interrupts may be triggered externally (P3.2/$\overline{\text{INT0}}$, P3.3/$\overline{\text{INT1}}$, P1.4/$\overline{\text{INT2}}$, P1.0/$\overline{\text{INT3}}$, P1.1/INT4, P1.2/INT5, P1.3/INT6).

This chapter shows the interrupt structure, the interrupt vectors and the interrupt related special function registers. **Figure 21** to **23** give a general overview of the interrupt sources and illustrate the request and the control flags which are described in the next sections.

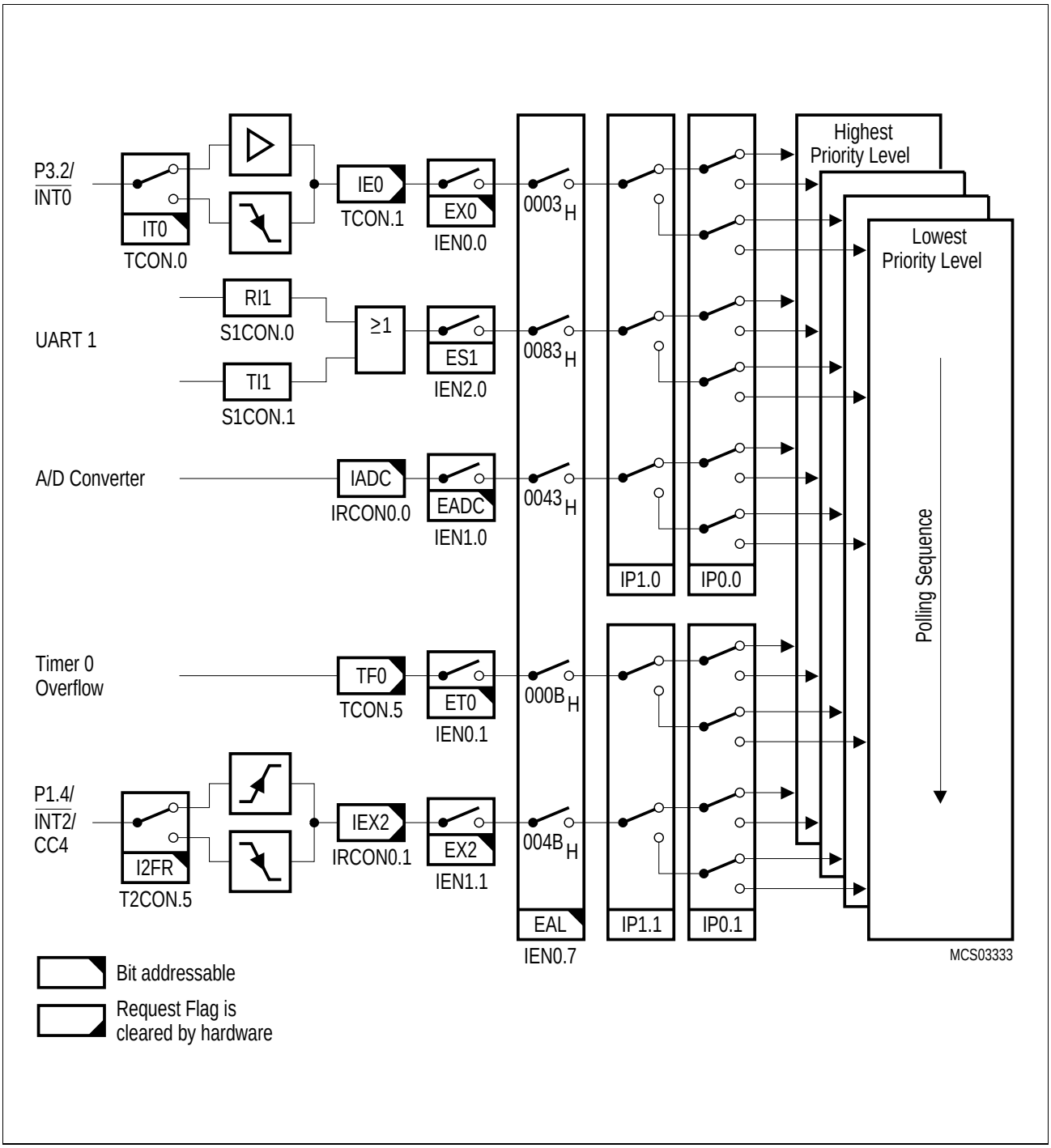


Figure 21
Interrupt Structure, Overview (Part 1)

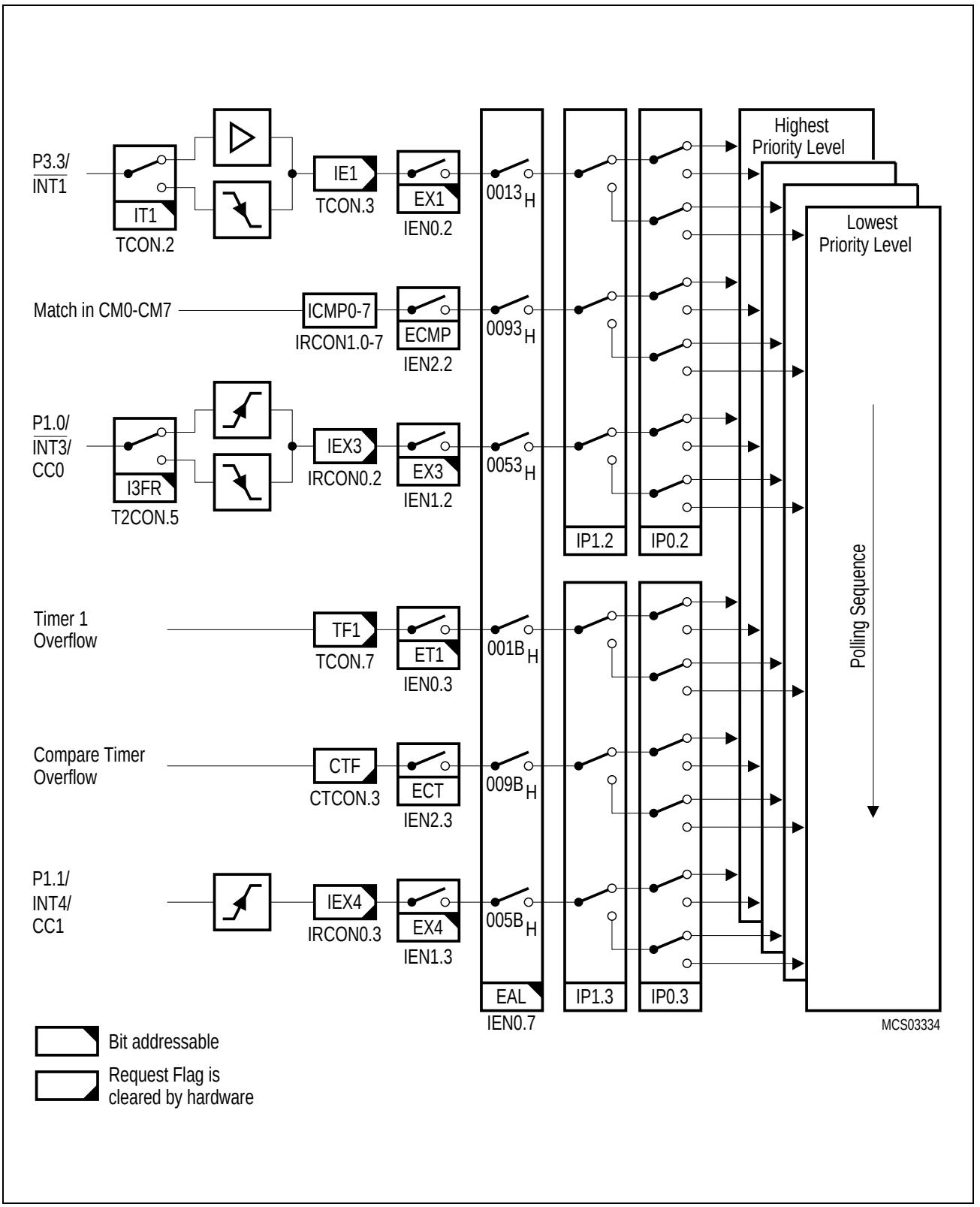


Figure 22
Interrupt Structure, Overview (Part 2)

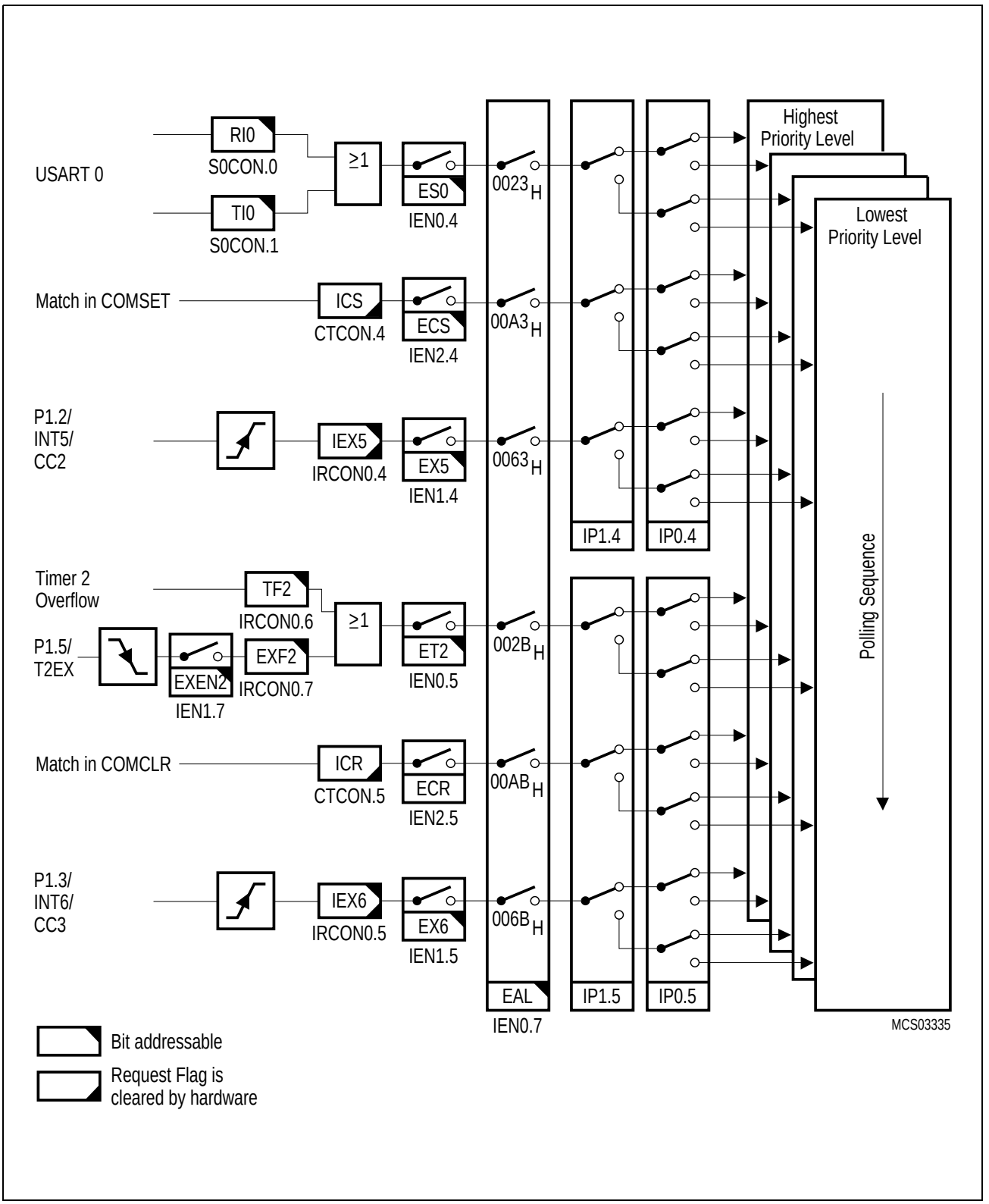


Figure 23
Interrupt Structure, Overview (Part 3)

Table 11
Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel 0	0023_H	RI0 / TI0
Timer 2 Overflow / Ext. Reload	$002B_H$	TF2 / EXF2
A/D Converter	0043_H	IADC
External Interrupt 2	$004B_H$	IEX2
External Interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External Interrupt 6	$006B_H$	IEX6
Serial Channel 1	0083_H	RI1 / TI1
Compare Match Interupt of Compare Registers CM0-CM7 assigned to Timer 2	0093_H	ICMP0 - ICMP7
Compare Timer Overflow	$009B_H$	CTF
Compare Match Interupt of Compare Register COMSET	$00A3_H$	ICS
Compare Match Interupt of Compare Register COMCLR	$00AB_H$	ICR

Fail Save Mechanisms

The C517A offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

- a programmable watchdog timer (WDT), with variable time-out period from 512 µs up to approx. 1.1 s at 12 MHz. (256 µs up to approx. 0.65 s at 24 MHz)
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C517A is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/24$ up to $f_{OSC}/384$. The system clock of the C517A is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 24** shows the block diagram of the watchdog timer unit.

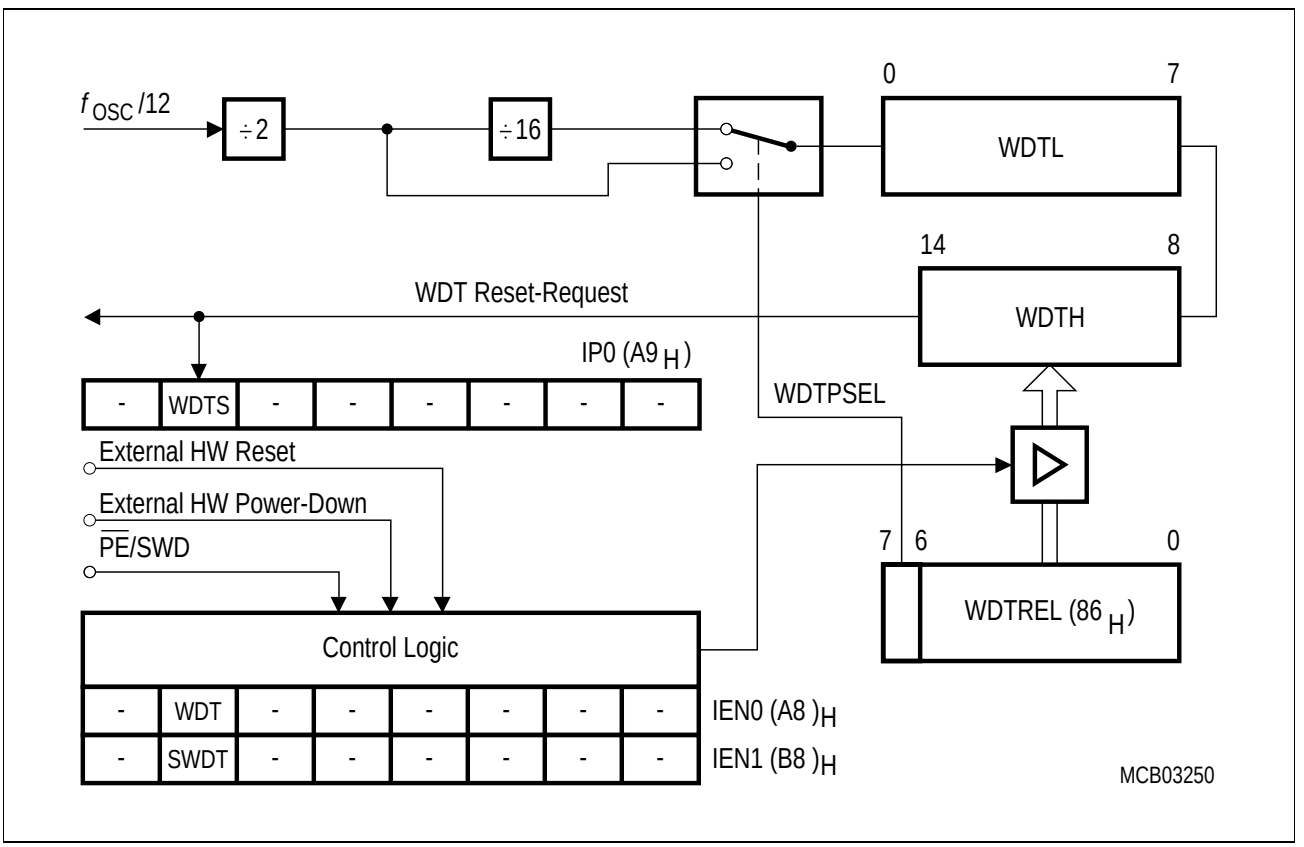


Figure 24
Block Diagram of the Watchdog Timer

The watchdog timer can be started by software (bit SWDT) or by hardware through pin $\overline{PE}$/SWD, but it cannot be stopped during active mode of the C517A. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transfered to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consequtive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog unit serves for four functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Restart from the hardware power down mode.**
  If the hardware power down mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete hardware power down sequence; however, the watchdog works identically to the monitoring function.

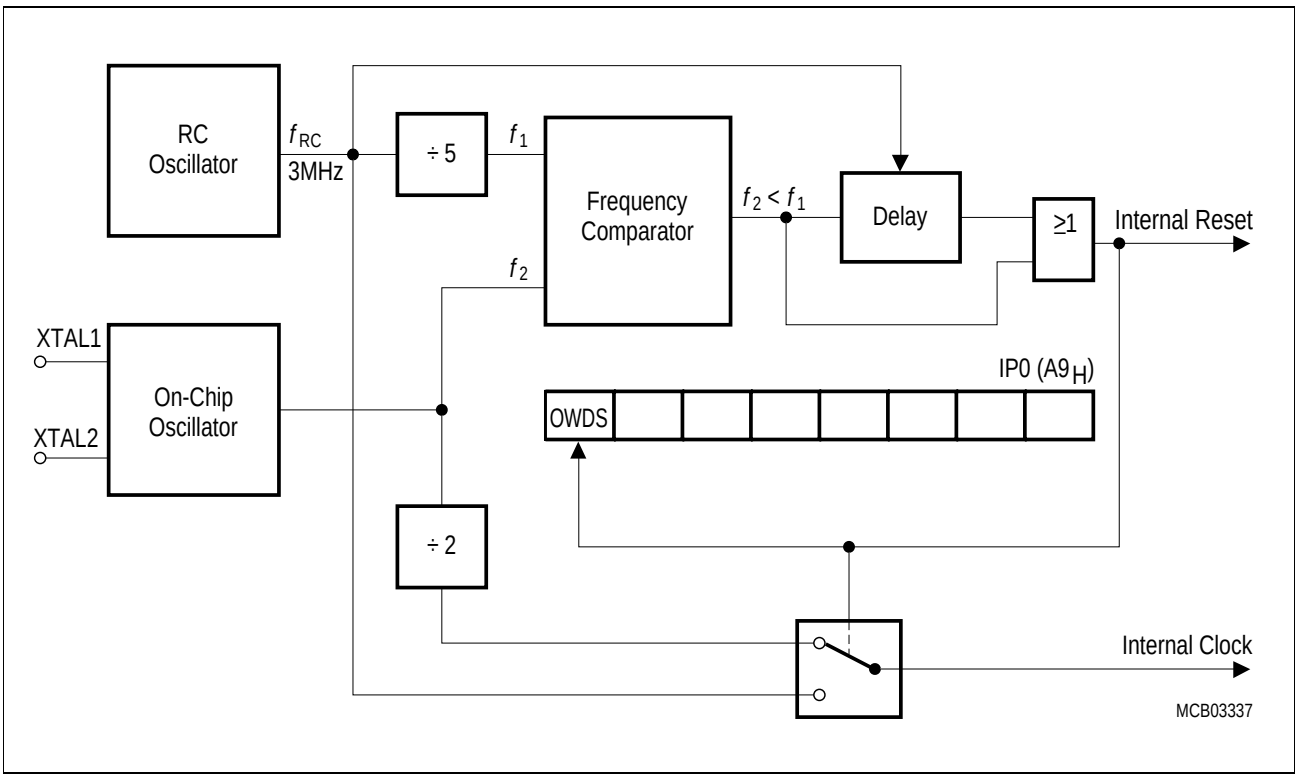


Figure 25
Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C517A provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**
  The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work. Idle mode is entered by software and can be left by an interrupt or reset.
- **Slow down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 8. This slows down all parts of the controller, the CPU and all peripherals, to 1/8th of their normal operating frequency and also reduces power consumption.
- **Software power down mode**
  The operation of the C517A is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. This power down mode is entered by software and can be left by reset.
- **Hardware Power down mode**
  If pin $\overline{\text{HWPD}}$ gets active (low level) the part enters the hardware power down mode and starts a complete internal reset sequence. Thereafter, both oscillators of the chip are stopped and the port pins and several control lines enter a floating state.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated. **Table 12** gives a general overview of the entry and exit procedures of the power saving modes.

Table 12
Power Saving Modes Overview

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Slow Down Mode	In normal mode : ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Internal clock rate is reduced to 1/8 of its nominal frequency
	With idle mode : ORL PCON,#01H ORL PCON, #30H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with 1/8 of its nominal frequency
		Hardware reset	
Software Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Rising edge at $\overline{PE}$/SWD	
Hardware Power Down Mode	$\overline{HWPD}$ = 0	$\overline{HWPD}$ = 1	Oscillator is stopped; internal reset is executed;

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	– 65	150	℃	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	–0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	–0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition		–10	10	mA	–
Absolute sum of all input currents during overload condition		–	| 100 |	mA	–
Power dissipation	P_{DISS}	–	TBD	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	–
Ground voltage	V_{SS}	0		V	–
Ambient temperature					
SAB-C517A	T_A	0	70	℃	18 and 24 MHz
SAF-C517A	T_A	–40	85	℃	18 and 24 MHz
SAH-C517A	T_A	–40	110	℃	18 MHz
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} - 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	–
CPU clock	f_{CPU}	3.5	24	MHz	–

DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage					
Pins except $\overline{EA}$,$\overline{RESET}$,$\overline{HWPD}$	V_{IL}	– 0.5	0.2 V_{DD} – 0.1	V	–
$\overline{EA}$ pin	V_{IL1}	– 0.5	0.2 V_{DD} – 0.3	V	–
$\overline{HWPD}$ and $\overline{RESET}$ pins	V_{IL2}	– 0.5	0.2 V_{DD} + 0.1	V	–
Input high voltage					
pins except $\overline{RESET}$, XTAL2 and $\overline{HWPD}$	V_{IH}	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
XTAL2 pin	V_{IH1}	0.7 V_{DD}	V_{DD} + 0.5	V	–
$\overline{RESET}$ and $\overline{HWPD}$ pin	V_{IH2}	0.6 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage					
Ports 1, 2, 3, 4, 5, 6	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Port 0, ALE, $\overline{PSEN}$, $\overline{RO}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage					
Ports 1, 2, 3, 4, 5, 6	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
		0.9 V_{DD}	–	V	I_{OH} = – 10 µA
Port 0 in external bus mode,	V_{OH1}	2.4	–	V	I_{OH} = – 800 µA [2]
ALE, $\overline{PSEN}$, $\overline{RO}$		0.9 V_{DD}	–	V	I_{OH} = – 80 µA [2]
Logic 0 input current					
Ports 1, 2, 3, 4, 5, 6	I_{LI}	– 10	– 70	µA	V_{IN} = 2 V
Logical 0-to-1 transition current,					
Ports 1, 2, 3, 4, 5, 6	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current					
Port 0, 7 and 8, $\overline{EA}$, $\overline{HWPD}$	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{DD}
Input low current					
to $\overline{RESET}$ for reset	I_{IL2}	– 10	– 100	µA	V_{IN} = 0.45 V
XTAL2	I_{IL3}	–	– 15	µA	V_{IN} = 0.45 V
$\overline{PE}$/SWD, OWE	I_{IL4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25°C
Overload current	I_{OV}	–	± 5	mA	[7] [8]

Notes see next page

Power Supply Current

Parameter		Symbol	Limit Values		Unit	Test Condition
			typ. 9)	max. 10)		
Active mode	18 MHz 24 MHz	I_{DD} I_{DD}	21.3 27.3	29.2 37.6	mA mA	4)
Idle mode	18 MHz 24 MHz	I_{DD} I_{DD}	11.6 14.6	16.2 20.4	mA mA	5)
Active mode with slow-down enabled	18 MHz 24 MHz	I_{DD} I_{DD}	9.5 10.7	13.1 14.9	mA mA	6)
Power-down mode		I_{PD}	15	50	µA	V_{DD} = 2…5.5 V 3)

Notes:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{\text{PSEN}}$ to momentarily fall below the 0.9 V_{DD} specification when the address lines are stabilizing.

3) I_{PD} (power-down mode) is measured under following conditions:
$\overline{\text{EA}}$ = $\overline{\text{RESET}}$ = Port 0 = Port 7 = Port 8 = V_{DD} ; XTAL1 = N.C.; XTAL2 = V_{SS} ; $\overline{\text{PE}}$/SWD = OWE = V_{SS} ; $\overline{\text{HWPD}}$ = V_{DD} for software power-down mode; V_{AGND} = V_{SS} ; V_{AREF} = V_{DD} ; all other pins are disconnected.
I_{PD} (hardware power-down mode) is independent of any particular pin connection.

4) I_{DD} (active mode) is measured with:
XTAL2 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL1 = N.C.;
$\overline{\text{EA}}$ = $\overline{\text{PE}}$/SWD == V_{SS} ; Port 0 = Port 7 = Port 8 = V_{DD} ; $\overline{\text{HWPD}}$ = V_{DD} ; $\overline{\text{RESET}}$ = V_{DD} ; all other pins are disconnected.

5) I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH} , t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL1 = N.C.;
$\overline{\text{RESET}}$ = V_{DD} ; $\overline{\text{HWPD}}$ = Port 0 = Port 7 = Port 8 = V_{DD} ; $\overline{\text{EA}}$ = $\overline{\text{PE}}$/SWD = V_{SS} ;
all other pins are disconnected;

6) I_{DD} (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} – 0.5 V; XTAL1 = N.C.;
$\overline{\text{HWPD}}$ = V_{DD} ; $\overline{\text{RESET}}$ = V_{DD} ; Port 7 = Port 8 = V_{DD} ;; $\overline{\text{EA}}$ = $\overline{\text{PE}}$/SWD == V_{SS} ; all other pins are disconnected.

7) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. V_{OV} > V_{DD} + 0.5 V or V_{OV} < V_{SS} - 0.5 V). The absolute sum of input currents on all port pins may not exceed 50 mA. The supply voltage V_{DD} and V_{SS} must remain within the specified limits.

8) Not 100% tested, guaranteed by design characterization

9) The typical I_{DD} values are periodically measured at T_A = +25 °C and V_{DD} = 5 V but not 100% tested.

10) The maximum I_{DD} values are measured under worst case conditions (T_A = 0 °C or -40 °C and V_{DD} = 5.5 V)

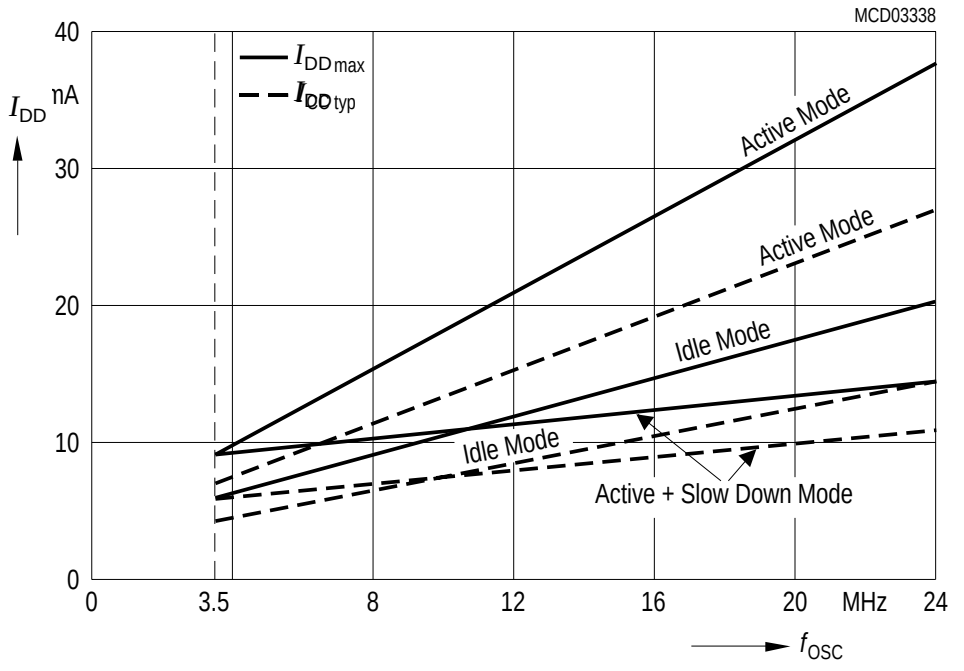


Figure 26
IDD Diagram

Table 13
Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\,typ}$ $I_{DD\,max}$	$1 * f_{OSC} + 3.3$ $1.4 * f_{OSC} + 4.0$
Idle mode	$I_{DD\,typ}$ $I_{DD\,max}$	$0.5 * f_{OSC} + 2.6$ $0.7 * f_{OSC} + 3.6$
Active mode with slow-down enabled	$I_{DD\,typ}$ $I_{DD\,max}$	$0.25 * f_{OSC} + 4.95$ $0.3 * f_{OSC} + 7.7$

Note : f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

A/D Converter Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{IN} ≤ V_{DD}-0.5V 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL	t_{ADC}	t_S	t_{ADCC}
÷ 8	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
$t_{IN} = 2 / f_{OSC} = 2\ t_{CLCL}$

Notes:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (18 MHz)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	71	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	26	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	26	–	t_{CLCL} – 30	–	ns
ALE low to valid instruction in	t_{LLIV}	–	122	–	4 t_{CLCL} – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	31	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	132	–	3 t_{CLCL} – 35	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	92	–	3 t_{CLCL} – 75	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	46	–	t_{CLCL} – 10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	48	–	t_{CLCL} – 8	–	ns
Address to valid instr in	t_{AVIV}	–	180	–	5 t_{CLCL} – 98	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C517A to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

CLKOUT Characteristics

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
ALE to CLKOUT	t_{LLSH}	349	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	71	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	516	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns

AC Characteristics (18 MHz, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		18 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 18 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	233	–	6 t_{CLCL} – 100	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	233	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	81	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	128	–	5 t_{CLCL} – 150	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	2 t_{CLCL} – 60	ns
ALE to valid data in	t_{LLDV}	–	294	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	335	–	9 t_{CLCL} – 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	117	217	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	92	–	4 t_{CLCL} – 130	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	16	96	t_{CLCL} – 40	t_{CLCL} + 40	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	11	–	t_{CLCL} – 45	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	239	–	7 t_{CLCL} – 150	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	16	–	t_{CLCL} – 40	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 18 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	55.6	285.7	ns
High time	t_{CHCX}	15	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	15	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns

AC Characteristics (24 MHz)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	$2\,t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	17	–	$t_{CLCL} - 25$	–	ns
Address hold after ALE	t_{LLAX}	17	–	$t_{CLCL} - 25$	–	ns
ALE low to valid instruction in	t_{LLIV}	–	80	–	$4\,t_{CLCL} - 87$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	22	–	$t_{CLCL} - 20$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	95	–	$3t_{CLCL} - 30$	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	60	–	$3\,t_{CLCL} - 65$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	32	–	$t_{CLCL} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	37	–	$t_{CLCL} - 5$	–	ns
Address to valid instr in	t_{AVIV}	–	148	–	$5\,t_{CLCL} - 60$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C517A to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

CLKOUT Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE to CLKOUT	t_{LLSH}	252	–	$7\,t_{CLCL} - 40$	–	ns
CLKOUT high time	t_{SHSL}	43	–	$2\,t_{CLCL} - 40$	–	ns
CLKOUT low time	t_{SLSH}	377	–	$10\,t_{CLCL} - 40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	2	82	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

AC Characteristics (24 MHz, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	6 t_{CLCL} – 70	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	6 t_{CLCL} – 70	–	ns
Address hold after ALE	t_{LLAX2}	53	–	2 t_{CLCL} – 30	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	118	–	5 t_{CLCL} – 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	2 t_{CLCL} – 20	ns
ALE to valid data in	t_{LLDV}	–	200	–	8 t_{CLCL} – 133	ns
Address to valid data in	t_{AVDV}	–	220	–	9 t_{CLCL} – 155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	67	–	4 t_{CLCL} – 97	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	t_{CLCL} – 25	t_{CLCL} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	t_{CLCL} – 37	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	–	7 t_{CLCL} – 122	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	–	t_{CLCL} – 27	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

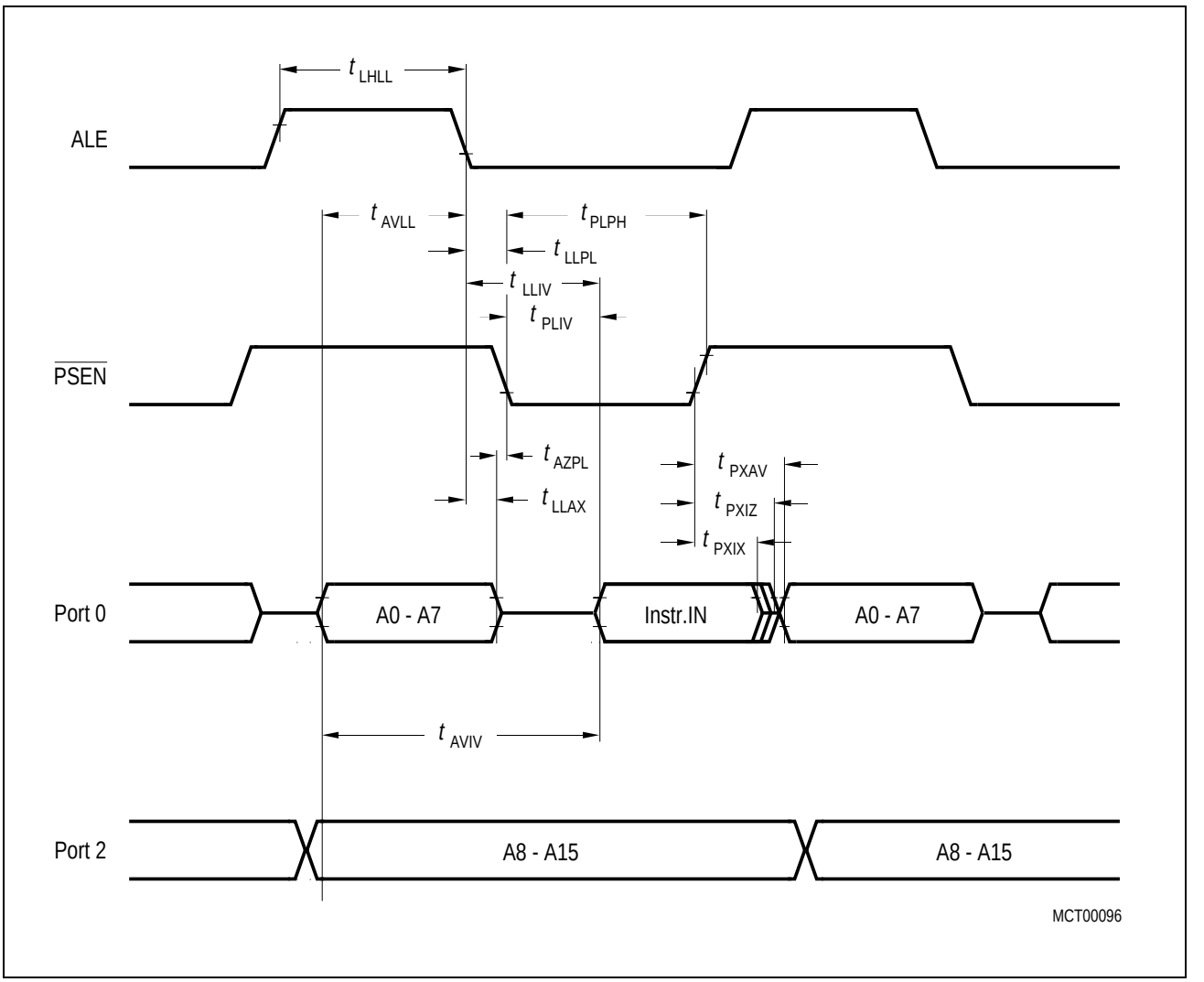


Figure 27
Program Memory Read Cycle

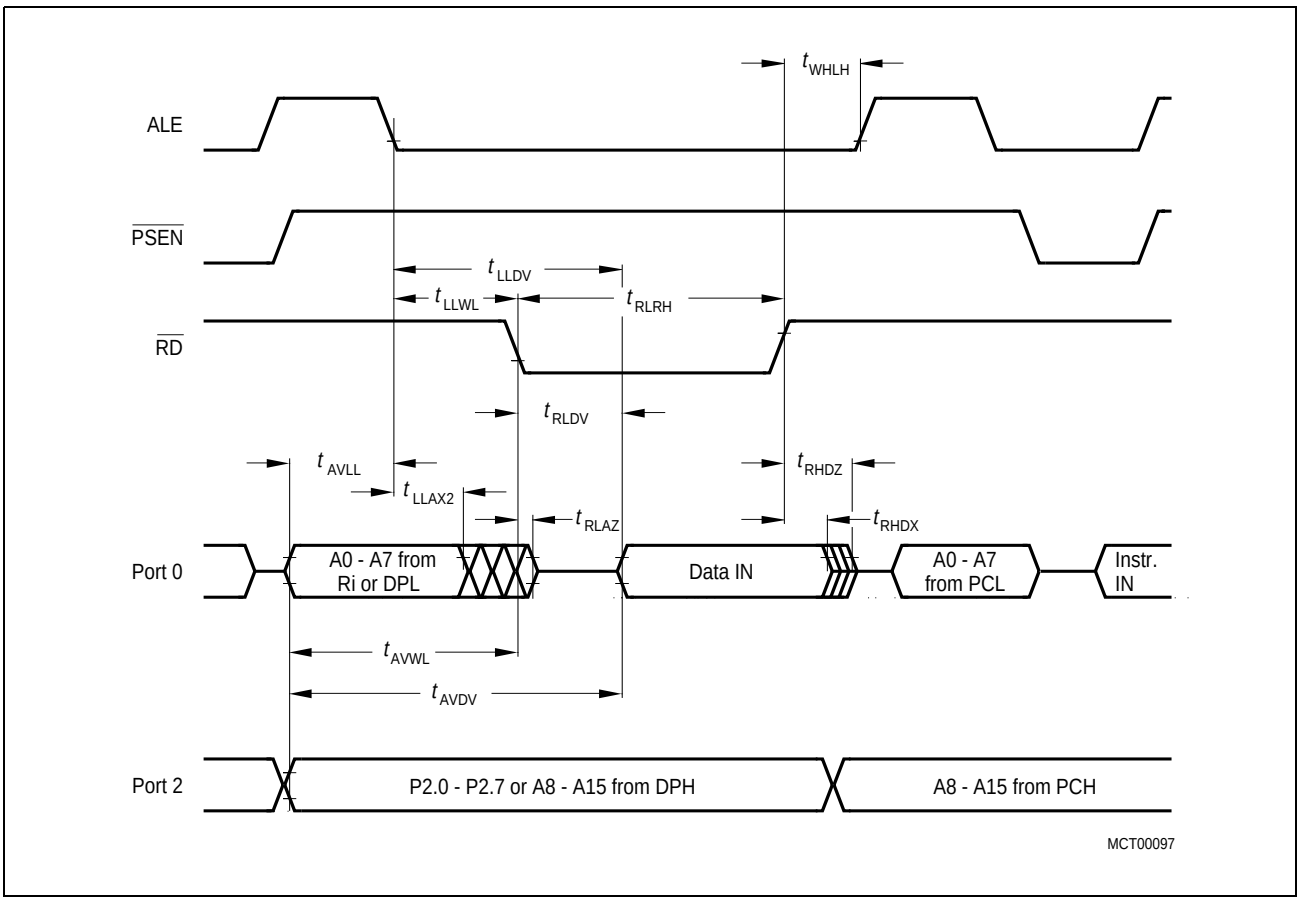


Figure 28
Data Memory Read Cycle

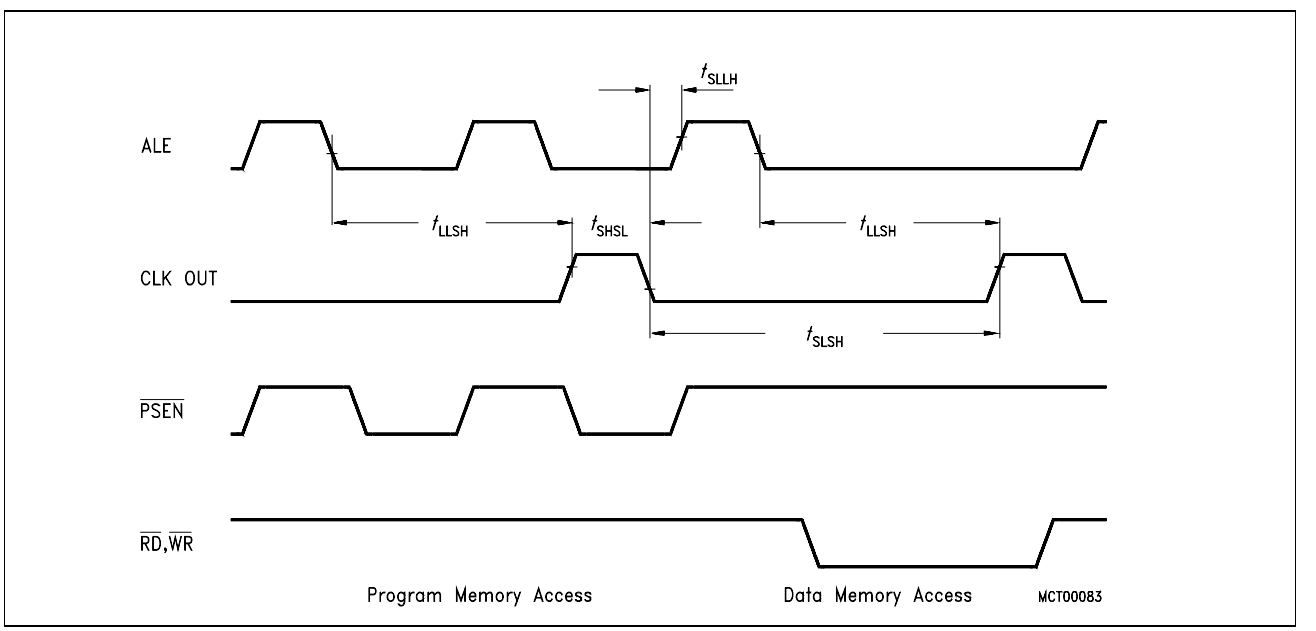


Figure 29
CLKOUT Timing

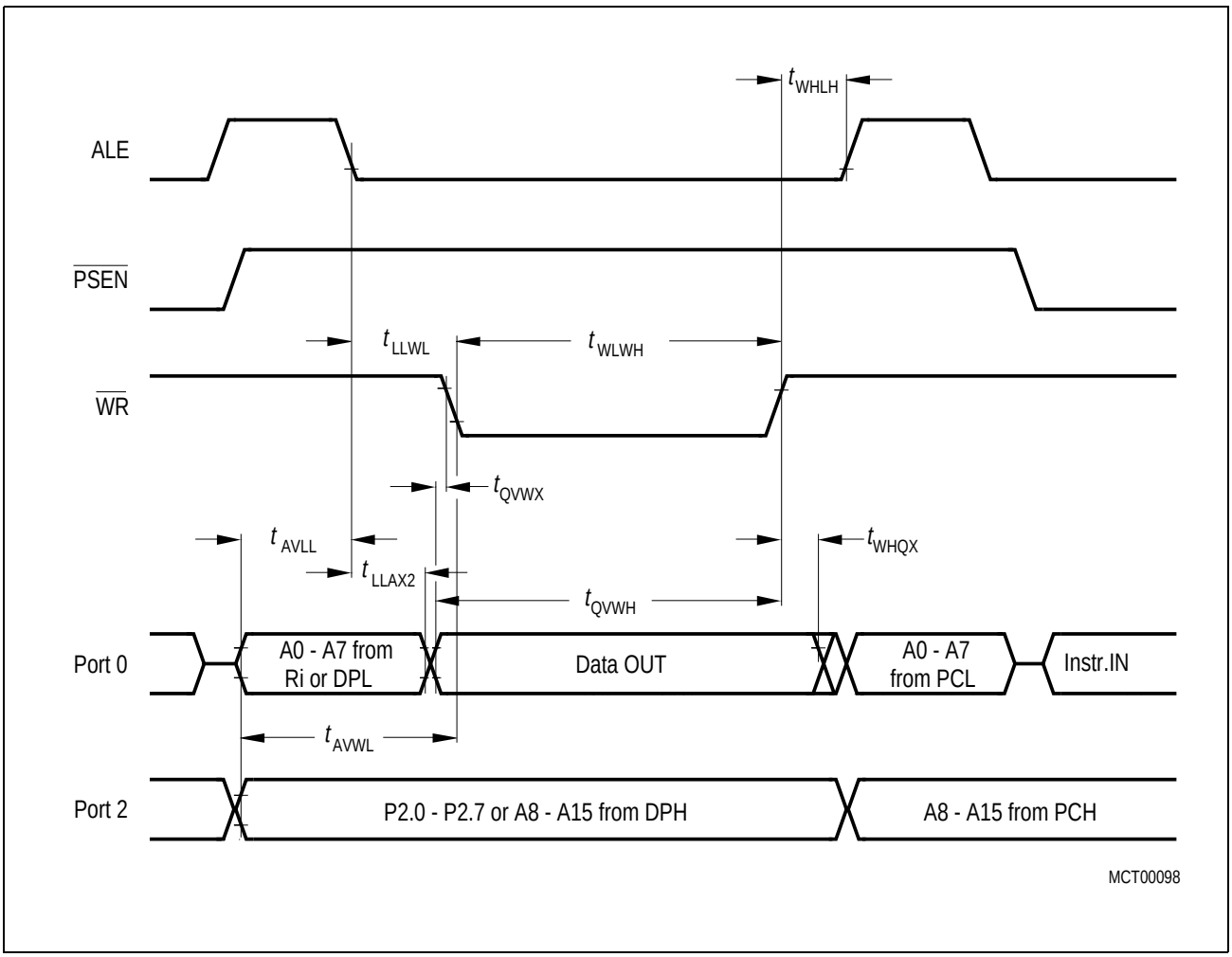


Figure 30
Data Memory Write Cycle

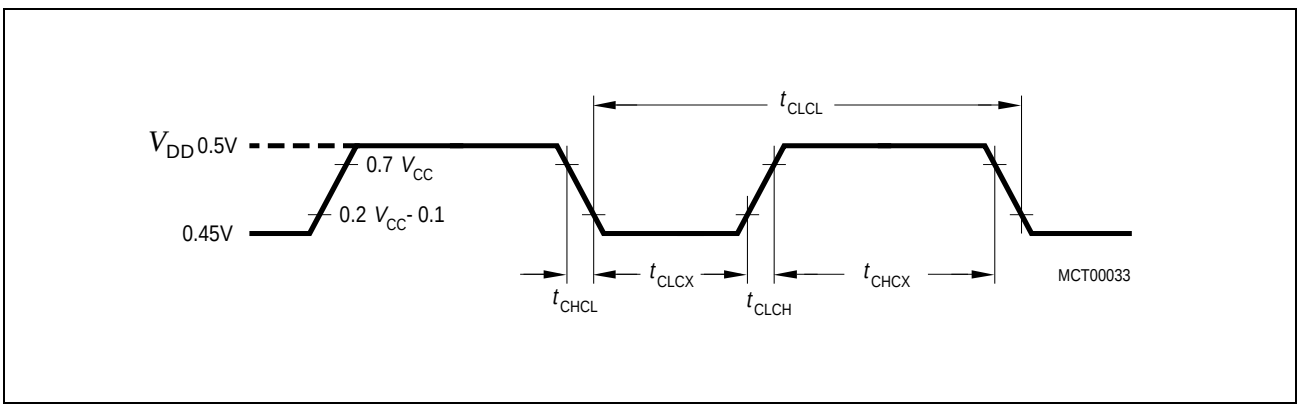


Figure 31
External Clock Drive on XTAL2

ROM Verification Characteristics for the C517A-4RM/4RN

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	10 t_{CLCL}	ns

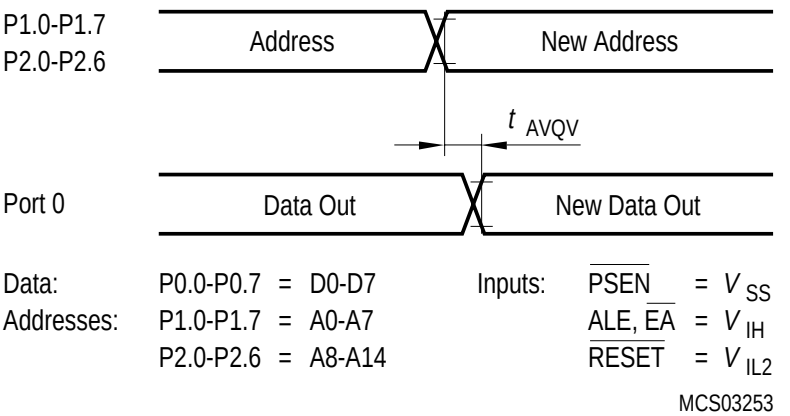


Figure 32
ROM Verification Mode 1

ROM Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	2 t_{CLCL}	–	ns
ALE period	t_{ACY}	–	12 t_{CLCL}	–	ns
Data valid after ALE	t_{DVA}	–	–	4 t_{CLCL}	ns
Data stable after ALE	t_{DSA}	8 t_{CLCL}	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CLCL}	–	ns
Oscillator frequency	1/ t_{CLCL}	3.5	–	24	MHz

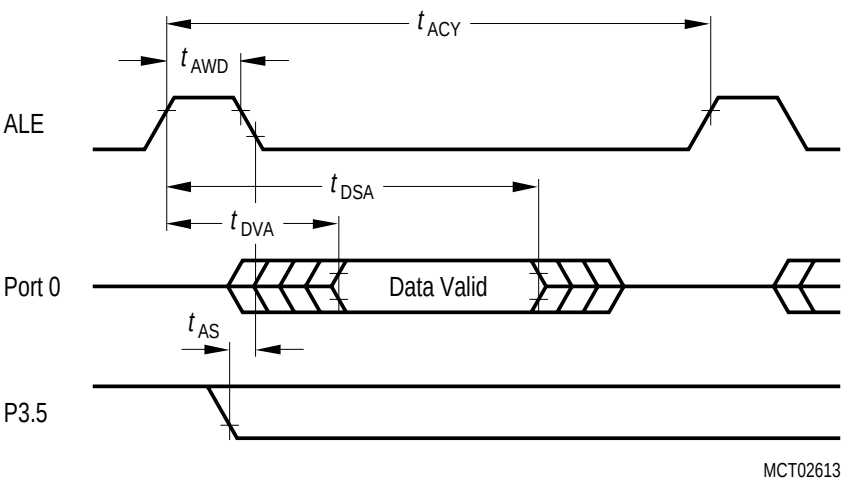
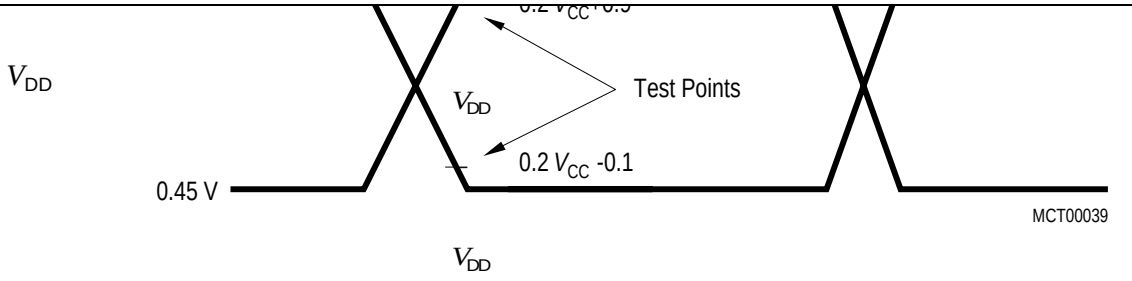
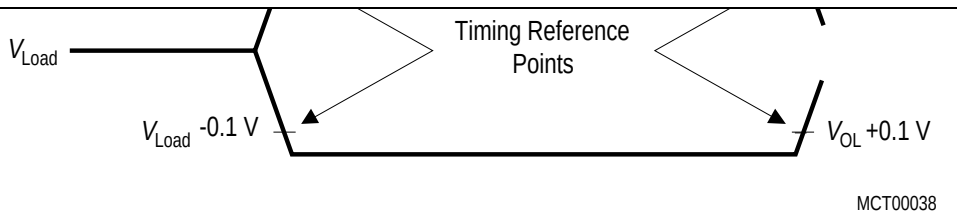


Figure 33
ROM Verification Mode 2



AC Inputs during testing are driven at V_{DD} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 34
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 35
AC Testing : Float Waveforms

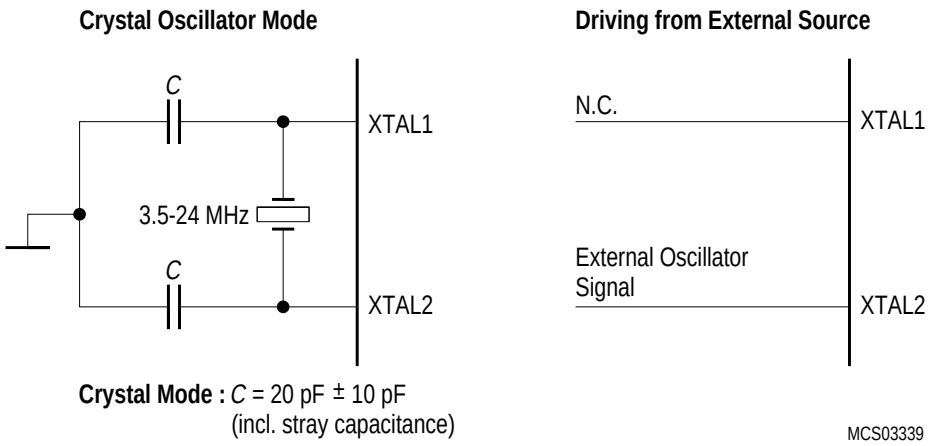


Figure 36
Recommended Oscillator Circuits for Crystal Oscillator

Plastic Package, P-MQFP-100-2 (SMD)
(Plastic Metric Quad Flat Package)

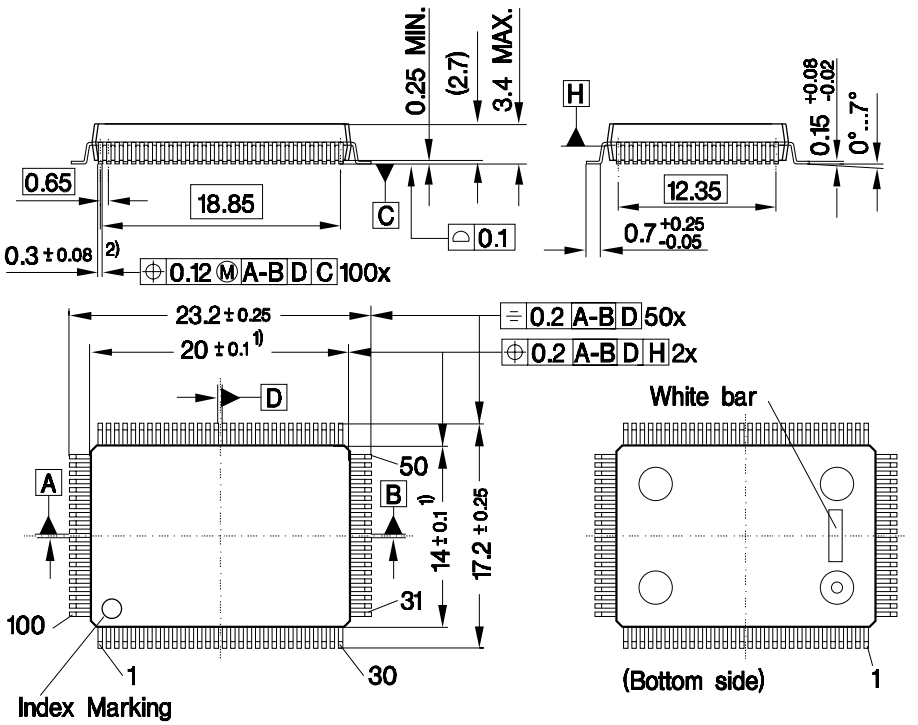
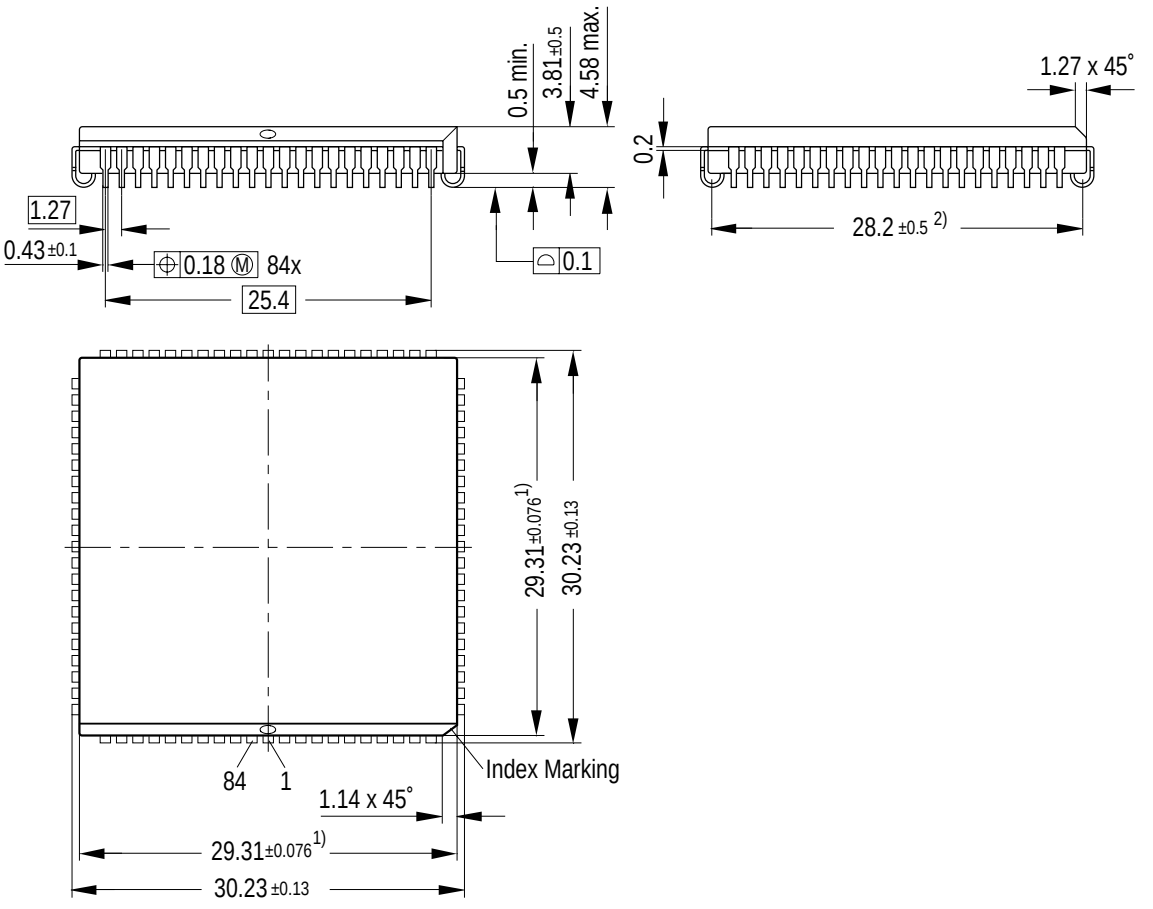


Figure 37
P-LCC-100-2 Package Outlines

Plastic Package, P-LCC-84-2 (SMD)
(Plastic Leaded Chip-Carrier)



1) Does not include plastic or metal protrusions of 0.25 max. per side

2) Dimension from center to center

Figure 38
P-LCC-84-2 Package Outline

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm