PHYTEC

microMODUL-8051 Low Power

Hardware Manual

Edition May 2003

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Preface

This microMODUL-8051 Low Power Hardware Manual describes the board's design and functions. Precise specifications for the 80C32-derivative microcontrollers can be found in the enclosed microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding EMV-Conformity of the PHYTEC microMODUL-8051 Low Power

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnatic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The microMODUL-8051 Low Power is one of a series of PHYTEC Single Board Computers (SBCs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional micro- / mini- and phyCORE OEM modules which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The microMODUL-8051 Low Power is a matchbox-size (51 x 36 mm) microcontroller board. Its various low power modes and optional external 11-channel A/D-converter with 12-bit resolution make the board particularly suitable for long-term data acquisition and applications requiring minimal power consumption. The board typically draws power via 3 - 4 mignon cells. It can be populated with various 8051-compatible microcontrollers (i.e. Dallas 80C323, OKI MSM 80C154S) These controllers generally offer special features, such as special on-chip peripherals.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. No description of compatible 80C32-derivative microcontroller functions is included, as such functions are not relevant for the basic operation of the microMODUL-8051 Low Power.

The microMODUL-8051 Low Power offers the following features:

- SBC in matchbox-size dimensions (51 x 36 mm) achieved through modern SMD technology
- improved interference safety through multi-layer technology
- controller signals and ports extend to standard-width (2.54 mm) pins aligning the edges of the board, allowing the board to be plugged into any target application like a “big chip”
- requires a single power supply of 2 – 6 V +10 %
- 128 (up to 512) kByte Flash on-board (TQFP)
- on-board Flash-programming
- no dedicated programming voltage through use of 3.3 V-Flash-devices
- 32 (up to 512) kByte RAM on-board (SMD)
- flexible software-configured address decoding through a complex logic device
- bank latches for Flash and RAM integrated in address decoder
- optional external 11-channel A/D-converter with 12-bit resolution and 10µs conversion time
- two free Chip Select signals for simple I/O connection to external peripherals
- Real-Time Clock (RTC 8583)
- Real-Time Clock and SRAM with an external battery buffer runs with up to 16 Mhz CPU clock (Dallas 80C323 only)

1.1 Block Diagram

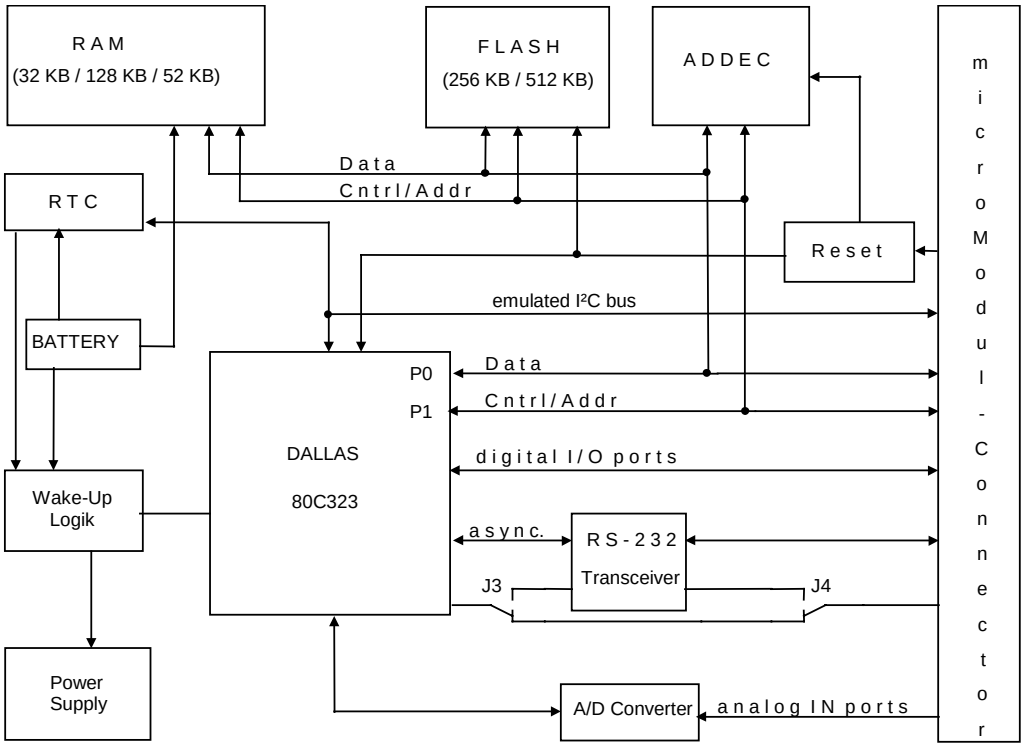


Figure 1: microMODUL-8051 Low Power Block Diagram

1.2 Overview of the microMODUL-8051 Low Power

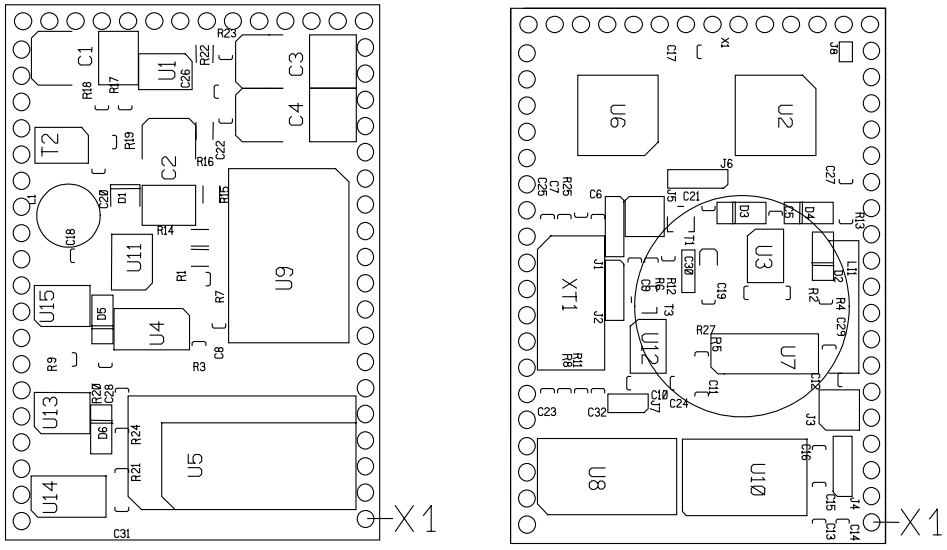


Figure 2: Overview of the microMODUL-8051 Low Power

2 Pin Layout

Please note that all module connections are not to exceed their expressed maximum voltage (3.3 V) or current. Maximum input values are indicated in the corresponding controller manuals. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to standard-width (2.54 mm / 0.10 in.) pin rows lining three sides of the board (referred to as microMODUL-connector). This allows the board to be plugged into any target application like a "big chip".
Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software. *Table 1* provides an overview of the pinout of the microMODUL-connector.

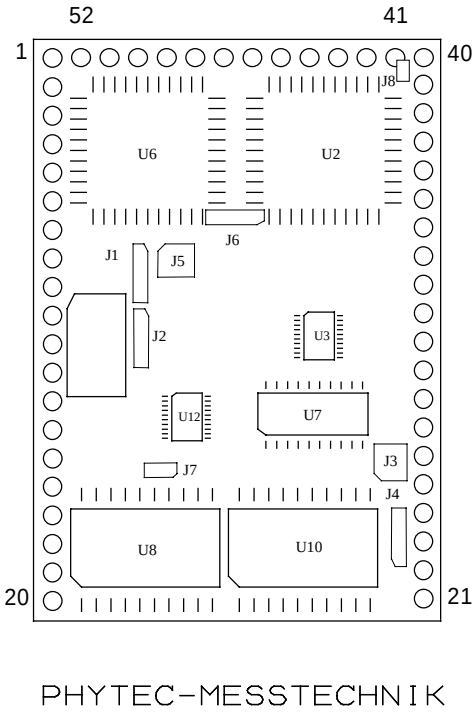


Figure 3: Pin Layout of the microMODUL-8051 Low Power

Pin #	Connection	Description
1	ALE	address latch enable
2...9	D0...D7	data bus (port 0 of the controller)
10[1]	/PON	power on
11	/Reset	/Reset input port of the module
12...19	AIN0...AIN7	analog inputs 0 – 7
20	GND	ground potential 0 V
21...28	P1.0...P1.7	port 1
29	P3.7 /RD	port 3.7 or /RD signal
30	P3.6 /WR	port 3.6 or /WR signal
31	P3.5 T1	port 3.5 or Timer 1
32	SDA	data line of the I²C bus
33	P3.3 INT1	port 3.3 or external INT1
34	SCL	clock of the **EMULATED** I²C bus
35[2]	P3.1 TXD	Port 3.1 or TXD (RS-232)
36[2]	P3.0 RXD	port 3.0 or RXD (RS-232)
37	/CS1	pre-decoded Chip Select signal #1
38	/CS2	pre-decoded Chip Select signal #2
39	VBAT	battery voltage
40	VCC	supply voltage 2-6 V=
41	AGND	analog ground (GND) 0 V
42	A_{ref}/ AIN10	analog reference voltage/ analog input 10
43...44	AIN9...AIN8	analog inputs 9-8
45...52	A8...A15	address bus (high byte)

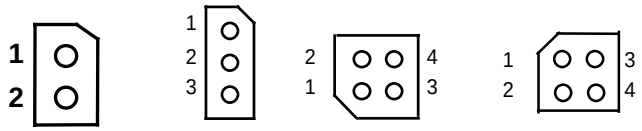
Table 1: Pinout of the microMODUL-Connector

1: OFF-Mode only functions properly if the module is mounted with a battery or if a 3 to 3.3 V. power supply is connected at VBAT (Pin 39).
If OFF-Mode is not used, module pin 10 (/PON) should be connected to GND in order to prevent an unintended shut-down of the microMODUL-8051 Low Power.

2: Following a Reset, the signal /SER_SHDN = Low. This means that the RS-232 transceiver must be initialized prior to beginning a serial transmission.

3 Jumpers

For configuration purposes, the microMODUL-8051 Low Power has 8 solder jumpers, some of which have been configured prior to delivery. *Figure 4* illustrates the numbering of the jumper pads, while *Figure 5* indicates the location of the jumpers on the board.



e. g. J7, J8 *e.g. J1, J2* *e.g: J3,* *e.g. J5*

Figure 4: Numbering of the Jumper Pads

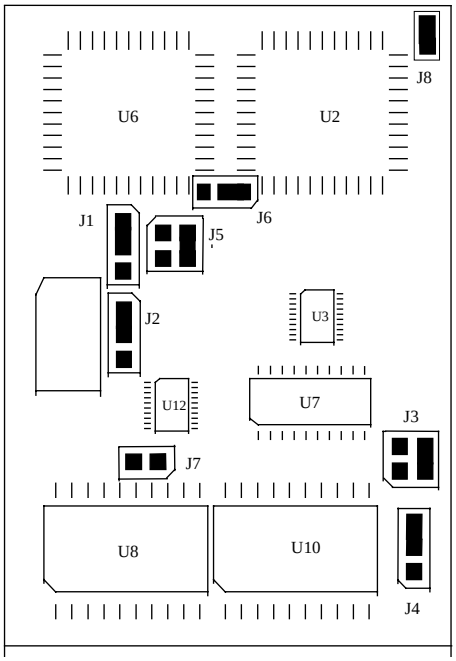


Figure 5: Location of the Jumpers (Top View)

The jumpers (J = solder jumper) have the following functions:

	Default Setting		Alternate Setting	
J1	(1+2)	external ROM active	(2+3)	internal ROM active
J2	(1+2)	RAM-size, 32 kByte and 128 kByte	(2+3)	RAM size 512 kByte
J3	(3+4)	Port pins 1.2 freely available	(1+3) (2+4)	Port pin 1.2 as RxD of the second RS-232
J4	(2+3)	Port pin 1.3 freely available	(1+2)	Port pin 1.3 as TxD of the second RS-232
J5	(1+2) (3+4) 232	open closed Data transfer via RS- as Wake-Up source	(1+2) (3+4)	Interrupt output of RTC as Wake-Up source open
J6	(1+2)	no power down of the address decoder Port P1.1 is not used.	(2+3)	Port P1.1 controls power down modes of the EPM7032V address decoder
J7	(open)	module pin 42= analog input 10	(closed)	Module pin 42 = external reference voltage
J8	(closed)	Connection between analog Ground to digital Ground	(open)	no connection from analog Ground to digital Ground Pin 41= external analog G round

Table 2: Jumper Settings Overview

3.1 J1 Internal or External Program Memory

At the time of delivery, Jumper J1 is closed at pads 1+2. This default configuration means that the program stored in the external program memory is executed after a Reset. In order to allow the execution of a specific controller's internal program memory, Jumper J1 must be closed at pads 2+3.

The following configurations are possible:

Code Execution	J1
from external program memory	1 + 2*
from internal program memory	2 + 3

*= Default setting

Table 3: J1 Access to External or Internal Program Memory

3.2 J2 Memory Size Selection

The microMODUL-8051 Low Power is designed to house either a 32, 128 or 512 kByte RAM memory device (U5). Jumper J2 has been pre-configured in accordance to the particular RAM chip populating the module:

The following configurations are possible:

RAM Device Size	J2
32 and 128 kByte RAM	1 + 2*
512 kByte RAM	2 + 3

*= Default setting

Table 4: J2 RAM Size Configuration

3.3 J3, J4 Special Features

If populated with the Dallas DS80C323 controller, jumpers J3 and J4 enable configuration of a second RS-232 interface at port pins P1.2 and P1.3.

The following configurations are possible:

Configuration P1.2 / P1.3	J3	J4
Port P1.2/P1.3 used as port pins	3 + 4*	2 + 3*
Port P1.2/P1.3 used as second RS-232 interface	1 + 3 2 + 4	1 + 2

*= Default setting

Table 5: J3 and J4 Second RS-232 Interface Configuration

3.4 J5 Wake-Up Source

Jumper J5 selects the signals that switch the board from power save mode to normal operation (Wake-Up source).

The following configurations are possible:

Wake-up Source	J5
no Wake-up source	open
Real-Time Clock interrupt	1 + 2
RS-232 data transfer	3 + 4*

*= Default setting

Table 6: J5 Wake-up Source Configuration

Note:
It is also possible to combine both Wake-Up sources.

Connecting the external signal /PON always results in Wake-Up of the microMODUL-8051 Low Power from OFF-Mode.

3.5 J6 Address Decoder Power-Down

Jumper J6 determines the function of the controller port pin P1.1 in conjunction with the address decoder populating the microMODUL-8051 Low Power.

The following configurations are possible:

Address Decoder Power Down	J6
Board populated with a PZ3032Device or P1.1 freely available	1 + 2*
Board populated with EPM7032V, P1.1 used for PLD power down	2 + 3

*= Default setting

Table 7: J6 Address Decoder Power-Down Configuration

3.6 J7 Configuration of Connector Pin 42

Jumper J7 determines the function of connector pin 42 on the microMODUL-8051 Low Power.

The following configurations are possible:

microMODUL-connector Pin 42	J7
Analog Input 10	open*
external Analog Reference Voltage	closed

*= Default setting

Table 8: J7 Connector Pin 42 Configuration

3.7 J8 Analog Ground

At the time of delivery, this jumper is closed by a short wire trace connecting the analog Ground and digital Ground. This connection can be separated using a scalpel or other suitable tool if analog to digital Ground connection is not desired. Analog Ground must be connected to microMODUL-connector pin 41 in this latter case.

The following configurations are possible:

Supply Voltage for U10	J8
analog Ground connected to digital Ground	closed*
analog Ground must be connected to connector pin 41	open

*= Default setting

Table 9: J8 Analog Ground Configuration

4 Memory Model

The microMODUL-8051 Low Power allows flexible address decoding which can be adjusted by software to different memory models. A hardware reset activates a default memory configuration that is suitable for a variety of applications. However, this memory model can be changed or adjusted at the beginning of a particular application.

Configuration of the memory is done within the address decoder by means of 4 internal decoder registers: two Control Registers, one Address Register and one Mask Register. All registers are carried out as write-only registers with access through the controller's XDATA memory space. There are two distinct address areas - selectable by means of the bit IO-SW in Control Register 1 - by which the registers can be accessed (*refer to the description of the bit IO-SW below*). Due to a lack of read access, a copy of all register contents should be maintained within your application. Reserved bits may not be changed during the writing of the register; contents must remain at 0. A hardware reset erases all registers while preserving the configuration of the default memory model.

The Input/Output registers are located within the I/O area. The register configures the communication with the A/D-converter as well as the power-down function. *Please refer to section 4.5 fore more details on* the Input/Output register.

Note:
In the event that you use FlashTools – PHYTEC's proprietary firmware allowing convenient on-board Flash programming - the address FA16 is preset at the start of your application software (*refer to section 4.1, "Control Register 1"*). This is to be noted upon installation of the software copy of the register contents.

The following figure illustrates the default memory model:

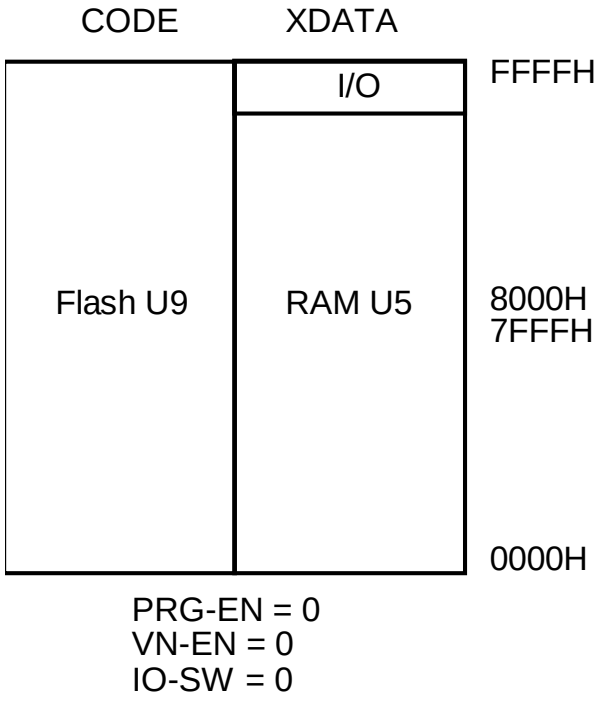


Figure 6: Default Memory model after Hardware-Reset

It should be noted that in case of modules equipped with only 32 kByte RAM, the RAM memory block U5 is mirrored in the XDATA area starting at 8000H. In this case U5 is located in the XDATA address range from 0000H - 7FFFH, as well as from 8000H - FFFFH. The corresponding I/O area is mapped to the XDATA memory space. Within this I/O area; there is no access to any available RAM.

The following sections describe the address decoder's registers for configuration of the memory model.

4.1 Control Register 1

Control Register 1 (Address 7C00H / FC00H)							
Bit 7							Bit 0
PRG-EN	IO-SW	*Res.*	VN-EN	FA18	FA17	FA16[1]	FA15
Default Value:							
Reset Value:				0000 0000 b			
Run Time Model				0000 0010 b			

Table 10: Control Register 1 of the Address Decoder

Bit invalid in programming-model (refer to PRG-EN)
Bit valid only in programming-model (refer to PRG-EN)

PRG-EN: Can be used to activate the special Flash programming memory model (PRG-EN = 1). This model is used within FlashTools[2] for Flash programming purposes and is of limited use within user applications because of its special restrictions.

In this model, 32 kByte Flash memory located within the address range 0000H - 7FFFH is accessible, as well as 32 kByte RAM within the range 8000H - FFFFH. The Flash memory can only be written in the XDATA memory space and can only be read from the CODE memory space. The RAM can be read from and written to in the XDATA memory space. RAM can also be read from the CODE memory space. The address line A15 of the Flash is derived from the Control Register 1 (Bit 0, FA15) only in the programming configuration. In the Runtime configuration (PRG-EN = 0), the address line A15 of the controller leads directly to the Flash device.

1: If using FlashTools - a firmware allowing convenient on-board Flash-programming - it should be noted that the bit FA16 will be preset at the start of user code. This is to be noted upon installation of the software copy of the register contents.

2: The FlashTools firmware is pre-installed in the external Flash device upon delivery of the module.

The bit IO-SW is also relevant to the programming model; whereas the bit VN-EN is not relevant. The following figure illustrates the programming model (the I/O area is not represented):

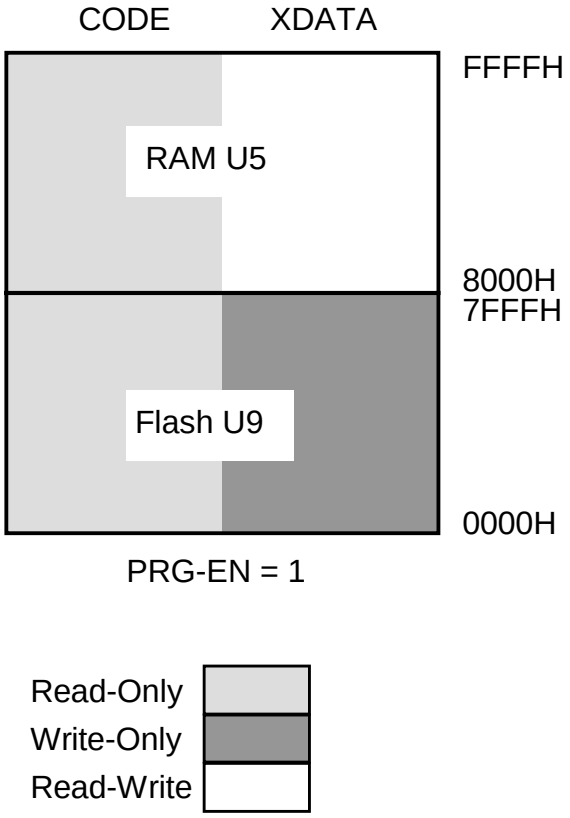


Figure 7: Memory Model for Flash Programming

IO-SW: By means of this bit the I/O area of the module can be mapped either to the upper or to the lower 32 kByte of the address space. With IO-SW = 0 following a hardware reset, the I/O area is accessible in the range between FC00H - FFFFH. Setting bit IO-SW = 1 maps the I/O area to 7C00H - 7FFFH.

This I/O area generally consists of 4 blocks of 256 bytes each. In three of these blocks, the address decoder provides a pre-decoded Chip Select signal that simplifies the connection of peripheral hardware to the module.

These Chip Select signals will be activated on read/write access to the XDATA memory space within the appropriate address range. The third block is reserved for generation of the power save signals as well as communication with the external A/D converter. The fourth block is reserved for internal access to the decoder's internal register (write-only access). This block is **not** available for use of connecting external devices.

The I/O area configuration is shown in the picture below:

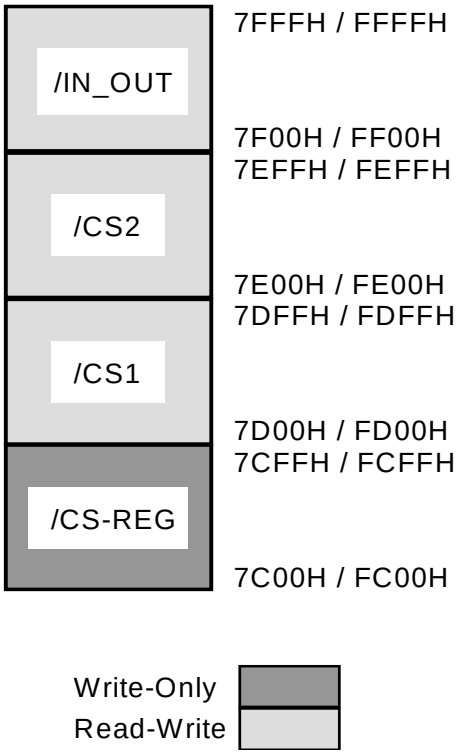


Figure 8: Configuration of the I/O Area

The areas referred to as /CS1 to /CS2 are the freely available Chip Select signals; while the signals /IN_OUT and /CS-REG is the decoder's internal signal. The signal IN_OUT is required to access the A/D converter, /CS-REG is required to access the internal registers. These latter signals are not available to the user and no external circuitry should be connected within the address area valid for the /IN_OUT and /CS-REG signals. In order to ensure proper functioning of FlashTools[1] firmware, enabling on-board programming of the Flash memory, it is essential that the /IN_OUT and /CS-REG signals be used as described herein. These internal registers are located at address 7C00H - 7C03H (IO-SW = 1) or FC00H - FC03H (IO-SW = 0). The rest of the /CS-REG block remains unused and is reserved for future expansion.

VN-EN: This bit enables free selection of von Neumann memory[2] within the address space of the controller. Following a hardware reset, the Harvard[3] architecture is configured as default. The von Neumann memory is especially useful when programming code is to be downloaded and subsequently run during runtime, as is the case with a Monitor program. The location of the optional von Neumann memory areas is defined by the Address and Mask Registers (*see below*).

1: Firmware portion of the utility program for on-board Flash programming and is pre-installed in the Flash at time of delivery.

2: Memory area in which no difference is made between CODE- and XDATA-access. This means that both accesses use the same physical memory device, usually a RAM.

3: Memory space in which CODE and XDATA accesses use physical different memory devices. CODE access typically uses a ROM or Flash device, whereas XDATA access uses a RAM.

Following a hardware reset (VN-EN = 0), the settings in the Address and Mask Registers are not released. The von Neumann memory is not available at this time. Setting bit VN-EN = 1 activates the Address and Mask Registers and incorporates their settings into access control for von Neumann memory areas. This bit is only relevant in the runtime model (PRG-EN = 0). In the programming model (PRG-EN = 1) bit VN-EN is unimportant and will be ignored.

FA[18..15]: The module can be optionally populated with a Flash device of 512 kByte capacity. Because of the limited 64 kByte address space of the microcontroller, the remainder of the Flash memory can only be accessed by bank switching.

In the runtime model (PRG-EN = 0), 64 kByte banks can be switched by controlling the upper address lines A[18..16] for the Flash through software. For this purpose, register bits FA[18..16] of the address decoder provide a latch to which the desired upper addresses can be written.

Of particular note is the bit FA15, which is solely relevant in the programming model (PRG-EN = 1). As in this model only 32 kByte of Flash can be accessed, it serves as address line A15 for the Flash memory. In the runtime model (PRG-EN = 0) with a 64 kByte Flash memory area, to contrast, the address line A15 of the controller is attached directly to the Flash.

The function of the bits FA[18..16] depends on the hardware configuration of the module. As described above, these bits are only relevant if the microMODUL-8051 Low Power is populated with a Flash device of 512 kByte capacity.

4.2 Control Register 2

Control Register 2 (Address 7C01H / FC01H)							
Bit 7							Bit 0
N/A[1]	*N/A*	*N/A*	*N/A*	*N/A*	RA18	RA17	RA16

Table 11: Control Register 2 of the Address Decoder

RA16: The module can accommodate a 512 kByte RAM. As the address space is limited to 64 kByte in the XDATA memory space of the controller, the remainder of the RAM can only be accessed by bank switching.

64 kByte banks can be switched by setting the high address lines A[18..16] through software. For this purpose, register bits RA[18..16] of the address decoder provides a latch to which the desired upper addresses can be written.

The purpose of these bits depends on the hardware configuration of the module. As described above, these bits are only relevant if the microMODUL-8051 Low Power is populated with a RAM device of 512 kByte capacity.

[1]: N/A: Not Accessible

4.3 Address Register

The Address Register 7C02H / FC02H functions in conjunction with the Mask Register (*see section 4.4*) to define the von Neumann[1] and Harvard[2] memory area in the controller's memory space. By setting the bit VN-EN in Control Register 1, the values of the Address and the Mask Register become valid for the definition of von Neumann and Harvard memory areas and will be incorporated in address decoding. (*refer to section 4.1, "Control Register 1"*)

The location of one or more Harvard memory areas can be configured with both registers. The remaining areas of the memory space are configured as von Neumann memory in which RAM is accessible in both XDATA and CODE memory space.

The mechanism for the memory space distinction is based on a comparison of the current address with a pre-defined address pattern of variable width. If the relevant bit positions of the address matches the pre-defined address pattern, memory access occurs according to the Harvard architecture. If the current address is different to the pre-defined address pattern, memory access occurs according to the von Neumann architecture.

Address Register (Address 7C02H / FC02H)							
Bit 7							Bit 0
HA15	HA14	HA13	HA12	HA11	HA10	*N/A*[3]	*N/A*

Table 12: Address Register of the Address Decoder

1: Memory space in which no difference exists between CODE and XDATA access. This means that both accesses use the same physical memory device, usually a RAM.

2: Memory space in which CODE and XDATA accesses use different physical memory devices, usually CODE access uses a ROM or Flash device, whereas XDATA access uses a RAM.

3: N/A: Not Accessible

The Address Register holds the address pattern mentioned above. Each bit of the pattern is compared with the corresponding address line of the controller (HA15 with A15, ..., HA10 with A10). As address lines A15 .. A10 are used to define Harvard memory space, only Harvard areas of at least 1 kByte can be configured. Memory areas smaller than 1 kByte can not be configured.

4.4 Mask Register

The Mask Register (7C03H / FC03H) can be used to mask single bits in the Address Register (see above). Following a hardware reset, all bits within the Address Register are relevant. By setting the individual bits in the Mask Register, all corresponding bits in the Address Register will no longer be regarded in the address comparison.

Mask Register (Address 7C03H / FC03H)							
Bit 7							Bit 0
MA15	MA14	MA13	MA12	MA11	MA10	*N/A*	*N/A*

Table 13: Mask Register of the Address Decoder

Note:
On modules populated with only 32 kByte of SRAM installed, the RAM device is mirrored within the XDATA memory space of the controller. Due to the fact that address line A15 is not recognized in this configuration, access to memory addresses above 8000H will result in physical access of memory addresses starting at 0H. This should be taken into consideration when configuring the memory model and the application software. Otherwise, functional failures could result from overlapping access.

The following examples of different combinations of the Address and Mask Registers illustrate these functions (only A15 to A8 are shown):

Address Reg.	**Mask Reg.**	**Comments (only for VN-EN = 1)**	
1XXXXX00 b	01111100 b	Harvard von Neumann	8000H-FFFFH, 0000H-7FFFH
0XXXXX00 b	01111100 b	Harvard von Neumann	0000H-7FFFH, 8000H-FFFFH
11111100 b	00000000 b	Harvard von Neumann	FC00H-FFFFH, 0000H-FBFFH
010X0000 b	00010000 b	Harvard and von Neumann and	4000H-43FFH 5000H-53FFH, 0000H-3FFFH, 4400H-4FFFH 5400H-FFFFH
10000000 b	00000000 b	Harvard von Neumann and	8000H-83FFH, 0000H-7FFFH 8400H-FFFFH
10100X00 b	00000100 b	Harvard von Neumann and	A000H-A7FFH, 0000H-9FFFH A800H-FFFFH

Table 14: Examples of Different Combinations of the Address- and Mask Registers

Reserved bits without function for address decoding (*refer to description of the register*).

X = irrelevant (on account of a bit set in the Mask Register)

The last example from the above table is further illustrated by the following figure:

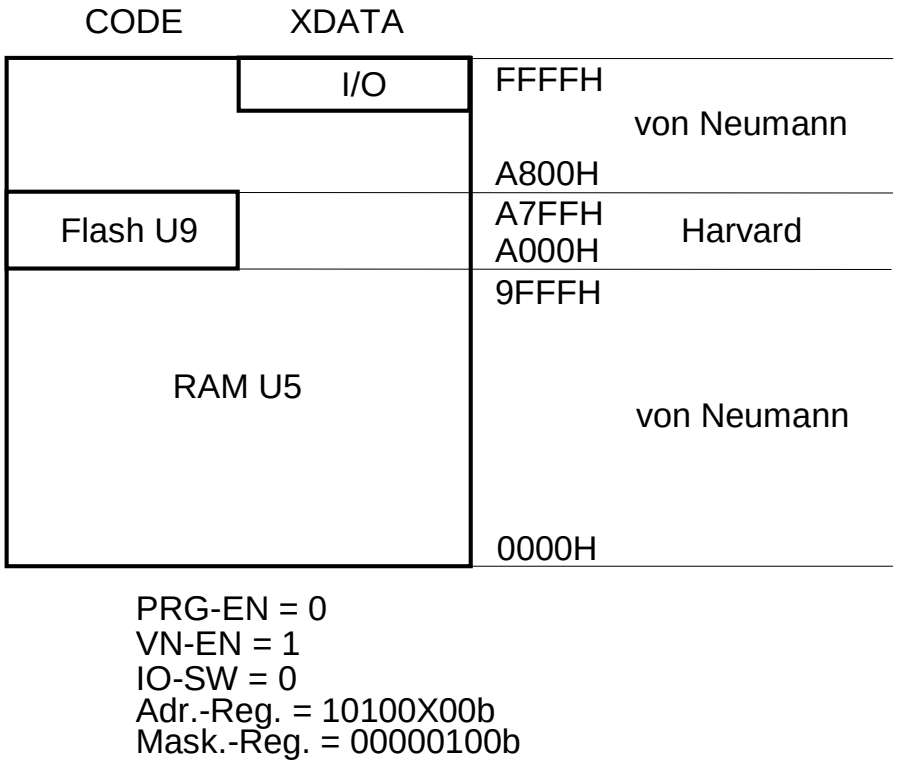


Figure 9: Example of a Memory Model

4.5 Input/Output Register

The Input/Output Register provides two separate registers enabling write-only access (Output Register) or read-only access (Input Register). The functions shown below in *Table 15* are executed during a write access to the Output Register. The contents of the Output Register cannot be read back. This means that a copy of the register contents should be maintained within the user code.

Output Register (Addresses 7F00H / FF00H) **Write Access!**							
BIT 7							BIT 0
/AD_CS	SCL	A/D_CLK	A/D_IN	Res.	/SER_SHDN	/SER_EN	POFF

Table 15: Output Register of the Address Decoder (Write Access Only)

Note
All bits are set to “0” following a hardware reset.

/AD_CS:	Chip Select signal for the A/D converter.
A/D_CLK:	This bit creates the clock for data transfer to and from the A/D-converter.
A/D_IN:	This bit transmits configuration data to the A/D-converter.
Res.:	This bit is reserved for future use.
/SER_SHDN:	If this bit is set to “0”, the voltage generator of the RS-232 transceiver is shut off and no data transfer is possible.
/SER_EN:	If this bit is set to “0”, the receiver circuit of the serial interface is on and data receipt is possible.
POFF:	If this it is set to “1”, the microMODUL-8051 Low Power is set to OFF-Mode.

All data shown below in *Table 16* is read during a read access from the Input Register.

Input Register (Addresses 7F00H / FF00H) **Read Access**							
BIT 7							BIT0
N/A	*N/A*	*N/A*	*N/A*	*N/A*	/PFO	A/D_EOC	A/D_OUT

Table 16: Input Register of the Address Decoder (Read Access Only)

/PFO: If the voltage of the battery buffer drops below 2.474 V, this bit will be set to “0”.

A/D_EOC: If this bit is set to “1”, the A/D-converter indicates the end of a data conversion cycle.

A/D_OUT: This bit outputs the conversion result of the A/D-converter over a serial data stream.

5 Flash Memory

Flash, as non-volatile memory on the microMODUL-8051 Low Power, provides an easily reprogrammable means of code storage to the user. The microMODUL-8051 Low Power can be populated at U9 by a single Flash device of type 29F010 with two banks of 64 kByte each or device type 29F040 with 8 banks of 64 kByte each.

Flash memory devices offer up to 100,000 reprogramming cycles, and enable on-board programming of user code. These Flash devices are programmable with 3.3 VDC. No dedicated programming voltage is required. All standard versions of the microMODUL-8051 Low Power feature a programming utility firmware – FlashTools (*refer to applicable QuickStart Instruction for more details*) – resident in the Flash device.

This firmware enables on-board download, as well as subsequent erasure and reprogramming, of user code into the Flash with the help of an intuitive PC-side software. The FlashTools firmware portion resides in the initial bank of Flash memory, which is not available for storage of user code. The total memory available for user programs is 64 kByte (29F010) or 448 kByte (29F040) *(refer to Figure 10)*.

Note:
Should the FlashTools firmware portion be erased from the Flash device without having a back-up or an equivalent replacement, reprogramming is no longer possible!

Please note that this firmware protects itself against any intentional or accidental erasure or overwriting. As the Flash device's hardware protection mechanism is not utilized, protection is limited to the software level. In the event that a user wishes to download his or her own programming algorithms or tools into the Flash, the user must ensure that a programming tool remains in the Flash memory. *Refer to the "QuickStart Instructions" for a detailed description of the on-board programming procedure.*

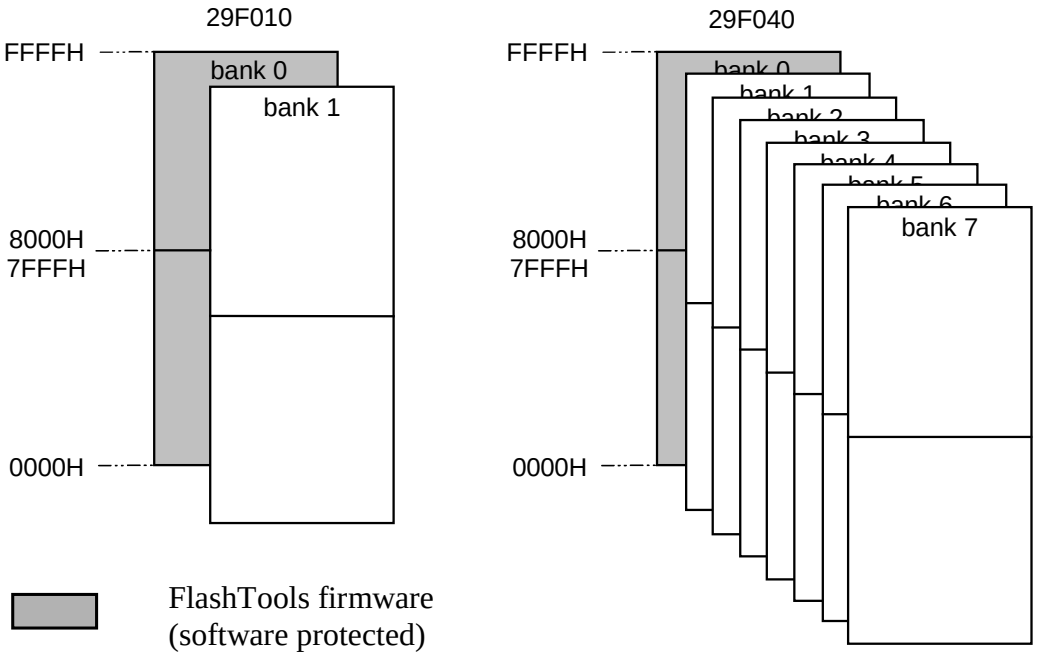


Figure 10: Memory Areas of the Flash Device

Use of a Flash device as the only code memory results in limited usability of the Flash as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash's internal programming process, the reading of data from Flash is not possible. For Flash programming, program execution must be transferred out of Flash (such as into von Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

6 Battery Buffer

The microMODUL-8051 Low Power can accommodate an external battery that connects to the board via pin 39. This battery buffer serves two purposes:

1) Back-up of data contents in the RAM device at U5

2) Provision of a power supply for Wake-Up logic (at U11 and U13) of the board when it is in OFF-Mode

In OFF-Mode, the board consumes approximately 10 µA. Such use gives the battery (lithium type CR2032) a life expectancy of approximately 2 years. As of the printing of this manual, a CR2032 lithium battery is recommended as it offers relatively high capacity at low discharge.

Note:
Be advised that despite the battery buffer, changes in the data content within the RAM can occur. The battery buffer does not completely remove the danger of data destruction.
Use of the OFF-Mode on the microMODUL-8051 Low Power requires use of a battery buffer. Otherwise the Shut-Down signal (SHDN) remains undefined The Shut-Down signal is generated by setting bit POFF in the Output Register (*refer to 4.5*).

Should the on-board Real-Time Clock not be initializes, then an interrupt occurs in a one second interval. This results in higher power consumption and faster discharge of the battery. For this reason we recommend that the Real-Time Clock be initialized prior to use of the OFF-Mode. The RTC can be initialized by setting bit 2 in the Control/Status Register (address 00) of the RTC. This must be done by user code.

7 Power Saving Modes

Various features to increase the battery lifetime are provided on the microMODUL-8051 Low Power. Please refer to the corresponding controller User's Manual for specific details on the controller's power down / idle mode. Additional devices supporting power saving modes are mounted on the module, such as ICs at U2, U10, U12 and U8. *Refer to the corresponding Data Sheets for details on their power saving modes.*

- Address decoder at U2
- RS-232 transceiver at U10
- Reference Voltage Device at U12 and
- optional A/D-converter at U8

Refer to the corresponding Data Sheets for details on their power saving modes.

7.1 OFF-Mode

The OFF-Mode of the microMODUL-8051 Low Power offers maximum power saving capabilities. If the module operates in this mode, the power supply via VCC is shut off and only essential board components (RAM, RTC and the Wake-Up logic at U2, U10, U12 and U8 are supplied via the battery buffer. Power consumption in OFF-Mode is approximately 10 µA.)

Note:
Please be advised that in OFF-Mode the controller is also disconnected from the supply voltage. During Wake-Up, a hardware reset is executed during power-on. For this reason, it is important that all register contents is copied into the battery-buffered RAM!

The microMODUL-8051 Low Power is switched into OFF-Mode by setting bit "0" to address FF00H. Depending on the configuration of Jumper J5, the module can be woken up via an interrupt of the RTC, an external /PON signal or data received via the RS-232 interface.

Caution:
OFF-Mode only functions properly if the module is mounted with a battery or if a 3 to 3.3 V power supply is connected at VBAT (Pin 39). If OFF-Mode is not used, module pin 10 (/PON) should be connected to GND in order to prevent an unintended shut-down of the microMODUL-8051 Low Power.

7.2 Power-Down Mode

Power-Down mode only switches the controller into Low Power mode and is a function of the underlying controller mounted on the board. *Precise specifications can be found in the corresponding controller User's Manual.*

7.3 IDLE-Mode

The IDLE-Mode is also a function of the controller mounted on the microMODUL-8051 Low Power. While IDLE-Mode offers less power savings, it offers the advantage that the microMODUL can quickly react to interrupts or other external events.

The following table summarizes the various Low Power modes:

	Invoked via:	**Comments:**	**Wake-Up via:**
1. OFF-Mode	MOV DPTR,#0FF00H MOVX DPTR,#xxxxxxx1B	RTC, RAM, U13, U11 supplied via the battery buffer. All other devices are not supplied.	Interrupt output of the RTC, external /PON-Signal or data flow via the RS-232.
2. Power-Down mode	SETB PCON.1	The controller is in PD-/Stop mode; while the Clock is shut off. The supply at VCC is active.	Interrupt output of the RTC, external /PON-Signal, external event at /INT1 or data received via RS-232.
3. IDLE mode	SETB PCON.0	The controller is in Idle-mode. The Clock is active and supply at VCC is active.	release of any interrupt

Table 17: Power Saving Modes of the microMODUL-8051 Low Power

7.4 RS-232, Address Decoder, Reference Voltage Source and A/D-Converter Power-Down

The RS-232 transceiver at U10, the EPM7032V address decoder at U2 and the A/D-converter at U8 have internal power saving features as described below:

RS-232 Transceiver

The signal /SER_SHDN, which is generated by erasing bit 2 at address FF00H, can shut down the RS-232 transceiver's voltage generator. In this case, the device consumes less that 1µA of power.

Note:
Following a hardware reset, the signal /SER_SHDN = Low. This means that the RS-232 transceiver must be initialized prior to start of any serial transmission.

Address Decoder

If mounted with a EPM7032V address decoder and if Jumper J6 is closed at pads 2+3, the address decoder can be switched into Power-Down mode via port pin P1.1. In Power-Down mode, the microMODUL can only access controller-internal functions (such as RS-232) and the Flash device.

If a PZ3032 address decoder populates the module, no Power-Down mode can be invoked as the decoder already offers minimal power consumption.

A/D-Converter

The A/D-converter can be switched into Power Down mode via transmission of the status message E0h into its data input register. No subsequent conversion is then possible and the power consumption of the IC drops to typically 4 µA.

8 A/D-Converter U8

The micoMODUL-8051 can be populated with an optional TLV2543 A/D-converter in order to support data acquisition. This device offers the following features:

- 11 input channels
- 12-bit resolution
- 10 µs conversion time over the specified temperature range
- integrated “Sample and Hold” function
- “Power Down” function
- configurable data length (8, 12 or 16-bit)

An on-board reference voltage also supports analog input signals in a range between 0 and 2.5 V. The LT1004CS8-2.5 reference voltage device features a stable conversion temperature characteristic of 20 ppm/°C.

Closing Jumper 7 allows connection of an external reference voltage to connector pin 42.

Communication with the A/D-converter is enabled via the Input/Output Register (*refer to section 4.5 of this manual*).

The following table indicates the conversion time of a 12-bit value via any of the available channels and its subsequent storage in memory. These conversion times were obtained using the included ***adc.inc*** test program.

Controller Type	Quartz Frequency	Conversion and Storage Time
Dallas 80C323	16 MHz	177 µs
Dallas 80C323	11.05 MHz	256 µs
Oki80C154	11.05 MHz	504 µs
Oki80C154	3.686 MHz	1.51 ms

Table 18: Sample Times of the A/D-Converter

9 Real-Time Clock RTC-8583 (U7)

For real-time or time-driven applications the microMODUL-8051 Low Power is equipped with an RTC-8583 Real-Time Clock (RTC) at U7. This RTC device provides the following features:

- serial input/output bus (I^2C)
- power consumption (f = 0 Hz) max. 50 µA (important for battery buffer)
- clock function with four year calendar
- universal timer with alarm and overflow indication
- 24- and 12-hour format
- automatic word address incrementing
- programmable alarm, timer and interrupt function

If the microMODUL-8051 Low Power is equipped with a battery, the Real-Time Clock runs independently of the module's power supply.

Programming of the Real-Time Clock is done via the I^2C bus by means of the Output Registers bit 6 (SCL) and port P3.4 (SDA) on the controller. The Real-Time Clock also provides an interrupt output which extends to the Wake-Up logic on the board as well as to /INT0.

An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. All interrupts must then be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. For more information on the features of the RTC-8583, refer to the corresponding Data Sheet located on the Spectrum CD.

Note:
Following attachment of a power supply to the board, the RTC generates **no** interrupts, as the RTC is not yet initialized.

10 Technical Specifications

The physical dimensions of the microMODUL-8051 Low Power are represented in *Figure 11*. The module's profile is about 11.5 mm thick, with a maximum component height of 4 mm on the back-side of the PCB and approximately 5 mm on the front-side. The PCB itself is approximately 1.5 mm thick.

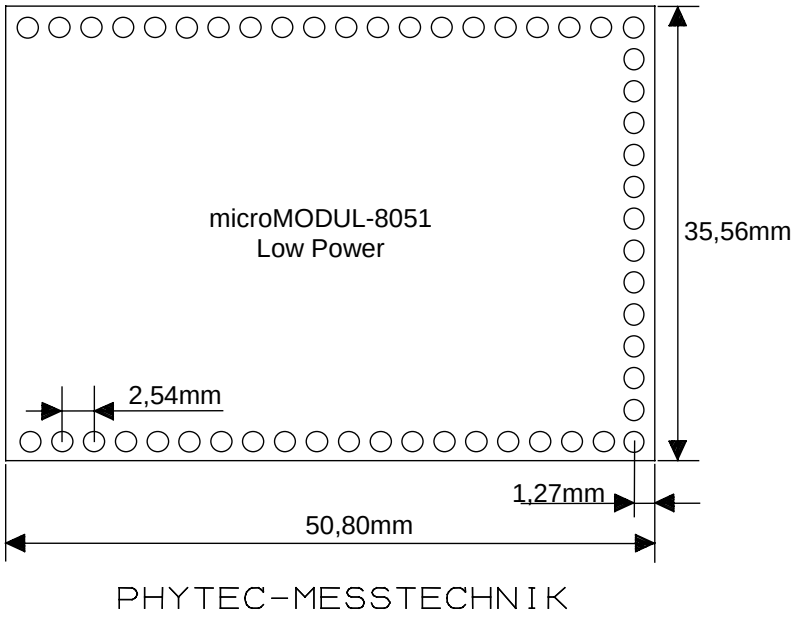


Figure 11: Physical Dimensions (not Shown at Scale)

Caution:
The microMODUL-8051 Low Power is a 3,3 V device. Attaching a higher supply voltage than 3,3 V to any of the modules pins will destroy the microMODUL-8051 Low Power!

Additional specifications:

- Dimensions: 50.8 x 35.56 mm., ±0,01 mm
- Weight: approximately 18 g with 512 kByte RAM
- Storage temperature: -40°C to +90°C
- Operating temperature: standard 0°C to +70°C
- Humidity: maximum 95 % r.F. not condensed
- Operating voltage: 2 - 6 V ±10 %, VBAT 3 V ±20 %
- Power consumption: *refer to Figure 12*
- Power Consumption in OFF-Mode: V_{BAT} <10µA (typ.)

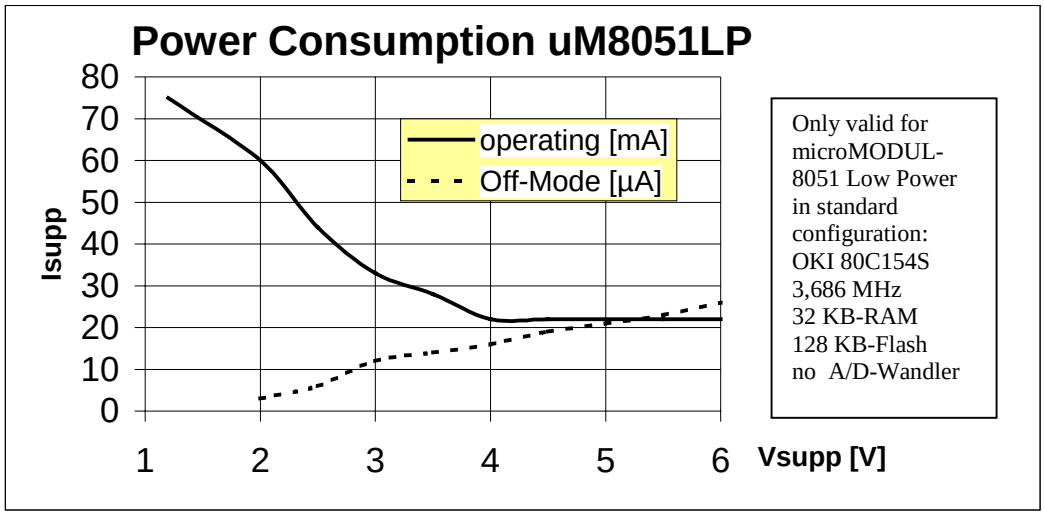


Figure 12: Power Consumption of the microMODUL-8051 Low Power

11 Hints for Handling the Module

Removal of the standard quartz or oscillator is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board remains undamaged while removing components. Overheating the PCB can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

When changing the controller it has to be taken care that the controller to be used is pin-compatible to the 8051 controller and that special hardware features are compatible with the layout of the module.

Appendice A Summary of Useful Hints

The microMODUL-8051 Low Power features some specific characteristics that should be taken into consideration before starting operation of the module and especially before writing application software. The following summary just highlights these special features. More information can be found in the appropriate sections within this manual.

- The internal execution speed of the controller can be calculated as follows: quartz frequency / 12. This means that the controller needs 1µs per instruction cycle at 12 MHz.
- Due to the fact that the microMODUL-8051 Low Power is designed as 3.3 V-only board, it is essential that no voltages higher than 3.3 V are attached to the module as this will destroy the board!
- Following a Reset, the serial interface device is shut down as default. If the RS-232 interface is used in your application, the transceiver needs to be activated as described in *section 4.5*.
- The on-board Real-Time Clock generates an interrupt every second in the default configuration. This causes an increased power consumption which can be avoided by initializing the RTC at the beginning of an application program. We recommed initialization of the RTC no matter if it is used or not. Refer to *section 9* for details.
- If OFF-Mode is not used, module pin 10 (/PON) should be connected to GND (module pin 20) in order to prevent an unintended shut-down of the microMODUL-8051 Low Power.
- If a Philips 80C51RA+ controller populates the microMODUL-8051 Low Power we recommend setting the bit LPEP in special function register AUX1 (to logic 1) during initialization of your application code. This results in lower power consumption.
- In the event that you use Control Register 1 at address FC00H, note that the address FA16 is preset (logic 1) at the start of your application software (*refer to section 4.1, "Control Register 1"*). Erase this bit only if you are familiar with its function.

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Document number: **L-305e_3, May 2003**

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