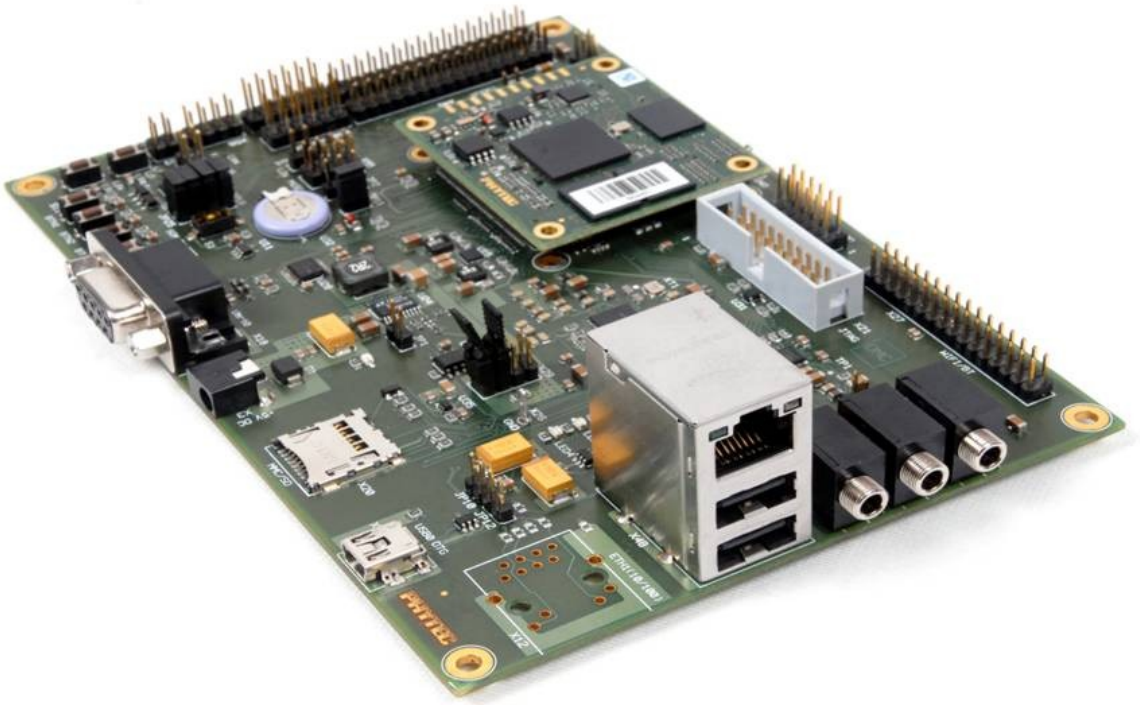
OpenBoard-phyCORE-AM335x

Hardware Manual

SOM Product No: PCM-051

Carrier Board Product No: PCM-950



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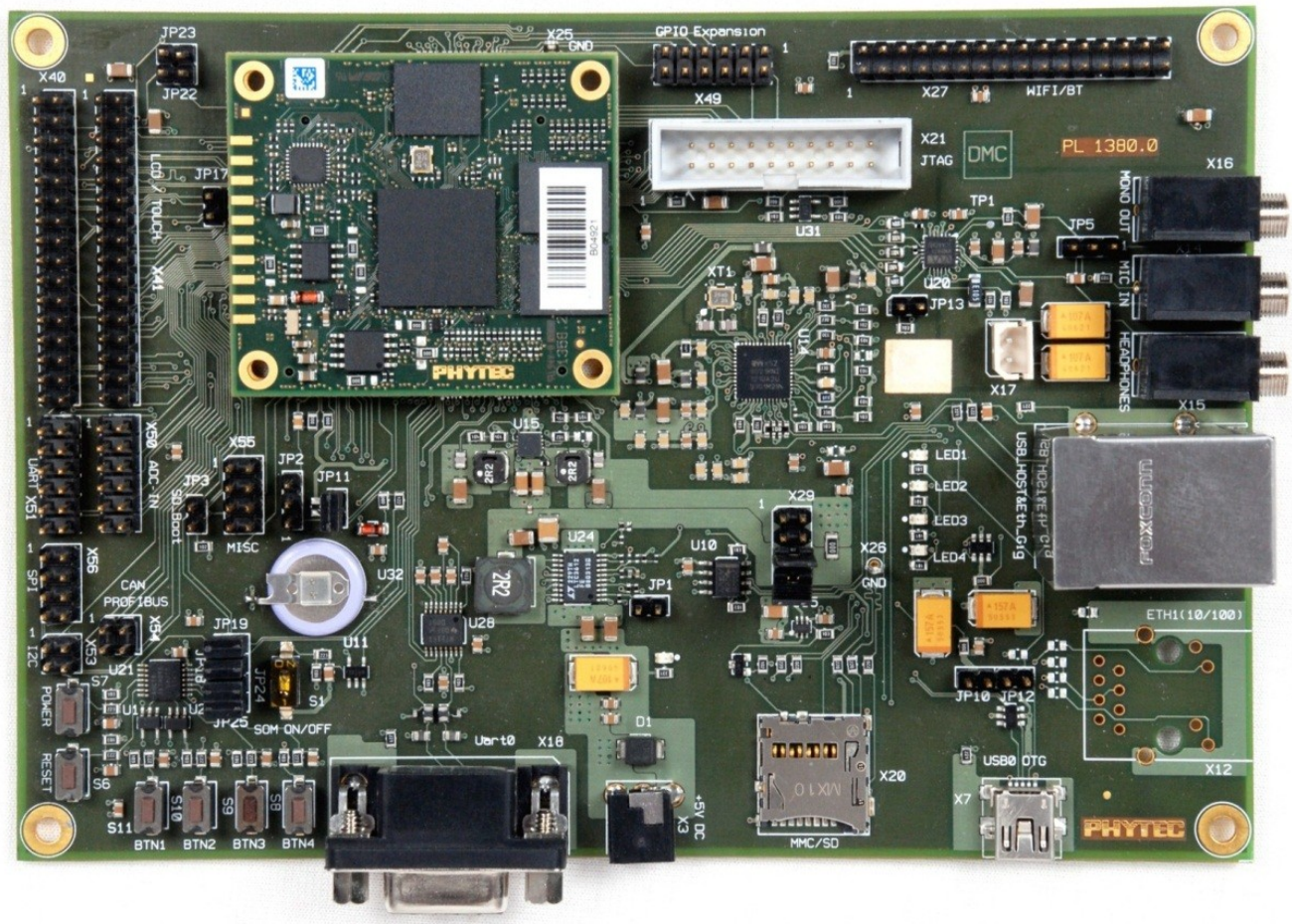

Figure 1: open board-AM335x

Open Board-AM335x with phyCORE-AM335x SOM

PHYTEC Open board-AM335x are equipped with all mechanical and electrical components necessary for the rapid start-up of the phyCORE-AM335x SOM. The Open board-AM335x is designed for evaluation, testing and prototyping of the phyCORE-AM335x in development environments prior to use in customer designed applications.

The Open board-AM335x has the following features for supporting the phyCORE-AM335x modules:

- Power supply circuits to supply power to the SOM and peripheral devices.
- RS-232 transceiver supporting data rates of up to 1Mbps with female DB9 connector.
- Audio codec and jacks for mono microphone input, mono audio output and Headphones.
- USB-A port supporting USB Host mode.
- 10/100/1000 Mbps Ethernet PHY and RJ-45 jack.
- RJ45 jack for 10/100 Mbps Ethernet (optional).
- USB Mini-AB port supporting USB OTG.
- Secure Digital Memory Card / MultiMedia Card Interface (SD/MMC).
- Four user buttons.
- Four user Leds.
- Gpio Expansion connectors.
- CAN Profibus connector.
- SPI connectors.
- I2C connectors.
- misc connectors.
- UART connectors.
- ADC connectors.
- LVDS LCD connector with touch support.
- Connector for a WiFi / Bluetooth module.
- Jumpers to configure interface options.
- SD_boot jumper to configure the boot order of the AM335x processor.
- Backup battery to power the SOM RTC.

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This modular development platform concept includes the following components:

- The phyCORE-AM335x System on Module populated with the AM335x processor and all applicable SOM circuitry including local power supplies, DDR3 SDRAM, NAND Flash, and an Ethernet PHY
- The Open board-AM335x which offers all essential components and connectors for start-up including a power socket which enables connection to an external power adapter, interface connectors such as RS-232, USB, CAN, SD, and Ethernet, allowing for use of the SOM's interfaces with standard cables.

Open board-AM335x Power

The Open Board is powered from the +5 VDC power input connector at X3. The VCC_5V0 power input from X3 routes to the phyCORE connector to provide power to the SOM, and also routes to voltage regulators on the open Board which supply its 1.2 V and 3.3 V local power rails.The open Board's 1.2 V and 3.3 V local power rails are enabled by the VAUX2_3P3V reference voltage from the SOM rather than powering up immediately with the VCC_5V0 input. This is so that the open Board does not drive signals into the AM335x processor when the SOM's local power supplies are off.

The open Board's 3.3 V power rail, VCC_3V3, is sourced from either an 800 mA or 3000 mA voltage regulator. This is selected at connector X29. Jumper pins 1+2 together and pins 3+4 together on X29 to select the 3.3 V supply with 800 mA capacity. Jumper X29 pins 5+6 and X29 pins 7+8 to select the 3.3 V supply capable of sourcing 3000 mA. By default, the 3.3 V power rail is connected to the 3000 mA supply. The VCC_1V2 local power supply is used by the Ethernet and EtherCAT PHYs. The VCC_3V3 local power supply is used by all of the Carrier Board interfaces.

In addition to the 1.2 V and 3.3 V voltages, the open Board has a +3.0 V battery. The always-on voltage from this battery routes to the phyCORE connector to power the Real-Time Clock (RTC) on the SOM. The battery voltage can be disconnected from the SOM with jumper JP2.

See for more information about the jumpers on the Carrier Board.

Overview of the Open Board-AM335x Peripherals

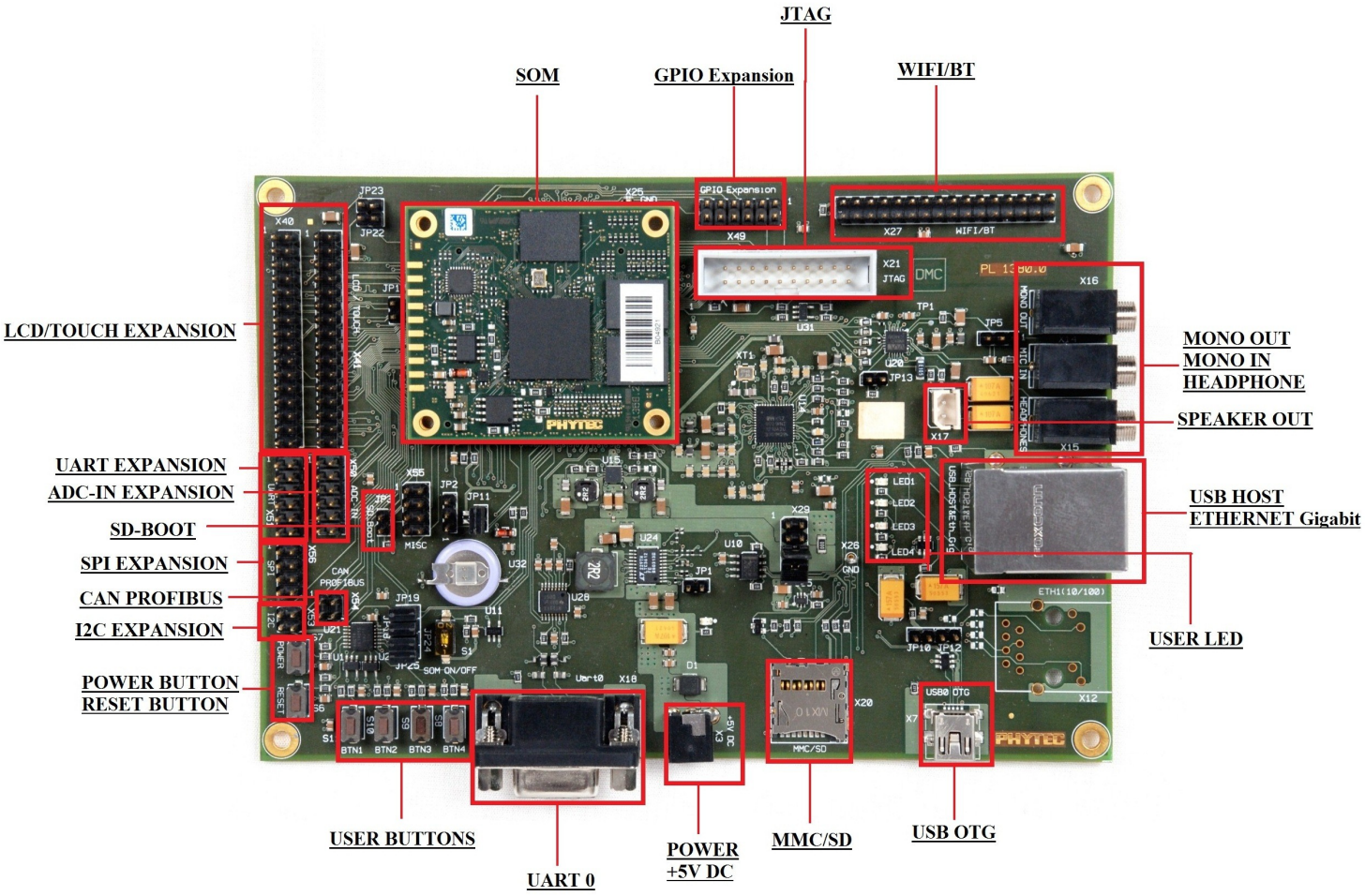


Figure 2: open board-AM335x peripherals

Connectors and Pin Headers

Reference Designator	Description	See Section
X1	phyCORE connector #2, 2x50 pins	
X2	phyCORE connector #1, 2x60 pins	
X3	+5VDC power input	
X7	USB0 OTG	
X12	Ethernet 1 (10/100 Mbps) (optional)	
X14	Mono audio input	
X15	Headphone output	
X16	Mono audio output	
X17	Loudspeaker output	
X18	RS232	
X20	SD / MMC	
X21	JTAG	
X25	GND	
X26	GND	
X27	WiFi/BT module	
X29	3.3 V power supply selection (3 Amp or 800 mA)	
X40	LCD/Touch	
X41	LCD/Touch	
X48	USB1 Host, Ethernet (10/100/1000 Mbps)	
X49	GPIO Expansion	
X50	ADC Expansion	
X51	UART Expansion	
X53	I2C Expansion	
X54	CAN PROFIBUS Expansion	
X55	MISC Expansion	
X56	SPI Expansion	

Table 1: Connector and pin description of the Open Board

User Buttons

The Open Board-AM335x includes six buttons. These are essential for the operation of the phyCORE-AM335x module on the Open Board. The button descriptions are in Table 23

Button	Description	Muxxing
S6 (Reset)	System Reset Button – issues a system warm-reset, must include a debounce circuit	
S7 (Power)	Power Button – issues a system power on/off event to the PMIC on the SOM	
S11 (Button1)	User button BTN1	X_RMII1_RXD1/_GPIO2_20
S10 (Button2)	User button BTN2	X_RMII1_RXD0/_GPIO2_21
S9 (Button3)	User button BTN3	X_GPIO3_7
S8 (Button1)	User button BTN4	X_GPIO3_8

Table 2: User buttons pin description of the Open Board

User LEDs

The Open Board-AM335x includes several LEDs. Their functions are listed in Table 24

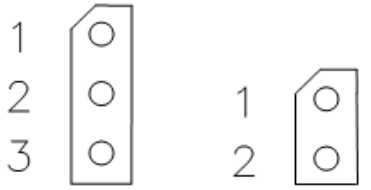
LED	Color	Description	Muxxing
D2 (5V Power)	Red	+5 VDC input power	
D14 (LED1)	Green	User LED 1/GPIO1_30	X_GPIO1_30
D19 (LED2)	Green	User LED 2/GPIO1_31	X_GPIO1_301
D15 (LED3)	Yellow	User LED 3/GPIO1_8	X_I2C1_SDA/_GPIO1_8
D20 (LED4)	Yellow	User LED 4/GPIO1_9	X_I2C1_SCL/_GPIO1_9

Table 3: User led's pin description of the Open Board

Jumpers

The phyCORE Carrier Board comes pre-configured with removable jumpers (JP) and solder jumpers (J).The jumpers allow the user to configure some of the features for development purposes. Table below lists the jumpers, their default positions, and their functions in each position. Before making connections to peripheral connectors, consult the applicable sections in this manual for setting the associated jumpers.

Figure depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board. The beveled edge in the silkscreen around the jumper indicates the location of pin.



e.g.: JP7 e.g.: JP1

Figure 3: Jumper Numbering Scheme

If manual modification of the solder jumpers is required, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

The following conventions were used in naming jumpers on the Carrier Board:

- J = solder jumper
- JP = removable jumper

Jumper	Setting	Description
J1	1+2	TOUCH_Y+ connects to AIN2
	2+3	Touch_Y+ connects to AIN1
J2	1+2	TOUCH_X- connects to AIN1
	2+3	Touch_X- connects to AIN2
JP1	Open	Enable the LTC 3612 (VCC_3V3_3000mA)
	closed	Disable the LTC 3612 (VCC_3V3_3000mA)
JP2	1+2	Backup battery voltage routes to the SOM to power the RTC
	2+3	Backup battery voltage does not route to the SOM
JP3	Open	Not to boot from SD card in first stage
	closed	To boot from SD card in first stage
JP5	1+2	U20 WM8974 Audio Codec's MICN input connects to X14 MIC IN connector pin "T".
	2+3	U20 WM8974 Audio Codec's MICN input connects to X14 MIC IN connector pin "R"
JP10	Open	USB0_VBUS signal has 4.7uF capacitance,OTG or device mode
	closed	USB0_VBUS signal has 150uF capacitance, use for dedicated embedded host mode

JP11	Open	USB1_ID is floating (or pulled up to 1.8V if R184 is populated). Use for OTG or device modes.
	closed	USB1_ID is connected to GND. Use for dedicated host mode.
JP12	Open	USB0_ID is floating (or pulled up to 1.8V if R46 is populated). Use for OTG or device modes.
	closed	USB0_ID is connected to GND. Use for dedicated host mode.
JP13	Open	U20 WM8974 Audio Codec's CSB/GPIO pin is pulled high.
	closed	U20 WM8974 Audio Codec's CSB/GPIO pin is connected to GND.
JP17	Open	SPI0_CS0 disconnected from LCD connector
	closed	SPI0_CS0 connects to LCD connector
JP18	Open	BTN3 (S8) is disconnected. GPIO3_7 can be accessed at JP18 as an input or output.
	closed	BTN3 (S8) is connect to GPIO3_7
JP19	Open	BTN4 (S9) is disconnected. GPIO3_8 can be accessed at JP19 as an input or output.
	closed	BTN4 (S9) is connect to GPIO3_8
JP22	Open	SPI Flash on SOM is not write protected
	closed	Write protect SPI Flash on SOM
JP23	Open	Access RTC interrupt output INT_RTCn and microcontroller interrupt input XDMA_EVENT_INTR1
	closed	Connect RTC interrupt output INT_RTCn to microcontroller interrupt input XDMA_EVENT_INTR1
JP24	Open	BTN2 (S10) is disconnected. GPIO2_21 can be accessed at JP24 as an input or output.
	closed	BTN2 (S10) is connect to GPIO2_21
JP25	Open	BTN1 (S11) is disconnected. GPIO2_20 can be accessed at JP25 as an input or output.
	closed	BTN1 (S11) is connect to GPIO2_20

Table 4: Open Board Jumper Descriptions
Defaults are in blue text

Open-Board Switch S1

The Open Board-AM335x has a switch to disable the power supply to the SOM. It basically enable PMIC_PWRHOLD so that the SOM Power is on hold.

Ethernet 1 (X12) (optional)

The connector for the Ethernet 1 port of the AM335x is at X12. The phyCORE-AM335x SOM comes populated with an Ethernet PHY at U3 supporting 10/100 Mbps Ethernet. The Ethernet differential signals are terminated on the SOM and routed through the phyCORE connector to RJ45 jack X12. This PHY on the SOM supports the HP Auto-MDIX function, eliminating the need for considerations of a direct connect LAN cable or a cross-over patch cable. The PHY detects the TX and RX signals of the connected device and automatically configures its TX and RX pins accordingly.

Ethernet 2 (X48)

The connector for the Ethernet 2 port of the AM335x is at X48. The Open Board-AM335x comes populated with an Ethernet PHY at U14 supporting 10/100/1000 Mbps Ethernet. The Ethernet differential signals are terminated and routed to RJ45 jack X48. The differential pairs from the Ethernet PHY are connected through a gigabit magnetics module to an RJ-45 Ethernet jack.

RS-232 (X18)

The RS-232 connector is at X18. This is the primary console UART for this board. The Open Board uses the AM335x UART0_TXD/RXD pins for the RS-232 port. The signals route from the phyCORE connector, through a transceiver to the female DB9 connector at X18.

USB0 OTG (X7)

The USB Mini-AB connector for USB0 (OTG) is at X7. The phyCORE-AM335x SOM comes with integrated On-The-Go (OTG) interfaces. This support high-speed, full-speed, and low-speed transactions.The Open Board-AM335x uses USB0 as an OTG port. By default, an embedded USB OTG host only needs to supply 8 mA of current to a connecting device on the port's VBUS signal. However, the phyCORE AM335x processors are not capable of supplying this much current, so if designing one of these ports as a dedicated host, the Carrier Board must provide a VBUS supply with at least 8 mA capacity. It should be noted that the maximum capacitance a USB OTG device can add to its VBUS signal is 6.5uF. This can be increased to the typical 120uF minimum required by the USB specifications for dedicated host devices if OTG mode is not required. On the PHYTEC Open Board, by default the USB0 port is configured as OTG, including having under 6.5uF capacitance on VBUS. It can be configured as a dedicated host instead by installing jumper JP10, to add 150uF additional capacitance to VBUS, and installing jumper JP12, to pull the ID signal low. The USB_ID signals tell the AM335x which type of interface each USB port is operating as. The ID pin is connected to ground inside the mini-A plug and left floating in the mini-B plug. The OTG device receiving the grounded ID pin is the default A-Device (host); the device with the floating, pulled-up ID signal is the default B-Device (peripheral).

USB HOST (X48)

The USB-A connector for USB1 (Host) is at X48. The phyCORE-AM335x SOM comes with integrated USB 2.0 interfaces. These support high-speed, full-speed, and low-speed transactions.The Open board-AM335x uses USB1 as a dedicated host.

JTAG (X21)

The Open Board's pin header at X21, connects to the AM335x's JTAG interface. This can be used for software debug. These JTAG signals are also accessible on the SOM at connector X2. Table has the JTAG signal pin assignments.

Pin	Signal
5	X_TDI
13	X_TDO
7	X_TMS
9	X_TCK
3	X_TRSTn
11	RTCK
15	SRST
1, 2	VCC_3V3
4, 6, 8, 10, 12, 14. 16. 18, 20	GND

Table 5: Open Board JTAG X21

LCD / Touch (X40,41)

The Open Board-AM335x supports the parallel display interface provided by the phyCORE-AM335x. The parallel display interface signals are converted into LVDS and are available at the PHYTEC Display-Interface(PDI). The parallel display interface is available at connector X40.The Open board-AM335x supports the parallel display interface provided by the phyCORE-AM335x. The various performance classes of the phyCORE family allow to attach a large number of different displays varying in resolution, signal level, type of the backlight, pinout, etc. In order not to limit the range of displays connectable to the phyCORE, the Open board-AM335x has no special display connector suitable only for a small number of displays. The new concept intends the use of an adapter board (e.g. PHYTECs LCD display adapters LCD-014 and LCD-017) to attach a special display, or display family to the phyCORE. A new Phytec Display-Interface (PDI) was defined to connect the adapter board to the phyCORE-OMAP44xx Carrier Board. It consists of two universal connectors which provide the connectivity for the display adapter. They allow easy adaption also to any customer display adapter. PDI data connector X40, X41 provides display data from the parallel display interface of the AM335x after the signals have been converted to LVDS.

PIN	SIGNAL
1	VCC_3V3
2	VCC_5V0
3	VCC_3V3
4	VCC_5V0
5	VCC_3V3
6	VCC_5V0

7	GND
8	VCC_5V0
9	SPI0_SCLK
10	SPI0_D1
11	SPI0_D0
12	SPI0_CS0
13	GND
14	GND
15	TOUCH_X+
16	GPIO3_4
17	TOUCH_X-
18	INTR1
19	TOUCH_Y+
20	I2C0_SCL
21	TOUCH_Y-
22	I2C0_SDA
23	GND
24	GND
25	ECAP0_IN_PWM0_OUT
26	RESET_OUTn
27	LCD_D3
28	LCD_D10
29	LCD_D2
30	LCD_D17
31	LCD_D1
32	LCD_D23

Table 6: Pin description of Open board X41Connector

PIN	SIGNAL
1	GND
2	GND
3	LCD_D0
4	LCD_D20
5	GND
6	GND
7	LCD_D16
8	LCD_D11
9	LCD_D18
10	LCD_D12
11	LCD_4
12	LCD_13
13	LCD_5
14	LCD_14
15	GND
16	GND
17	LCD_6
18	LCD_15
19	LCD_D7
20	LCD_HSYNC
21	LCD_D22
22	LCD_VSYNC

23	LCD_19
24	LCD_AC_BIAS_EN
25	GND
26	GND
27	LCD_D8
28	LCD_D21
29	LCD_D9
30	LCD_PCLK
31	GND
32	GND

Table 7: Pin description of Open board X40 Connector

MMC/SD (X20)

The AM335x MMC0 interface routes directly to MMC/SD connector X20. The AM335x processor can be configured to boot from the MMC0 interface by configuring the boot pins appropriately either with the resistors on the SOM or with jumper JP3 on the Open Board.

WiFi/BT (X27)

A WiFi/Bluetooth module, such as the PHYTEC PCM-958, can connect to the Open Board's pin header at X27. WiFi shares some signals with the Profibus interface. When the WiFi module is installed, the Profibus transceiver is automatically disabled to prevent it from interfering with the WiFi module.

Pin	Signal
1	X_MCASP1_FSX, SPI1_D1, GPIO3_2
2	VCC_3V3
3	X_MCASP1_AXR0
4	VDIG1_1P8V
5	X_MCASP1_ACLKX, SPI1_D0, GPIO3_1
6	VDIG1_1P8V
7	GND
8	GND
9	X_UART1_TXD, P_UART0_TXD
10	VCC_3V3
11	X_SPI1_CS1, UART1_RTS
12	VCC_3V3
13	X_GPIO3_19
14	VCC_3V3
15	GND
16	VCC_3V3
17	X_PORZ
18	GND
19	X_PORZ
20	X_MCASP1_AXR2, SPI1_SCK, GPIO3_0
21	X_MMC1_D3, UART3_TX
22	X_UART1_RXD, P_UART0_RXD
23	GND
24	X_SPI1_CS0, UART1_CTS
25	X_MMC1_D2, UART3_RX

26	GND
27	X_MMC1_D1, UART2_TX
28	
29	X_MMX1_D0, UART2_RX
30	X_MMC1_CMD, GPIO0_21
31	GND
32	X_MMC1_CLK, GPIO0_28

Table 8: Pin description of Open board X27 Connector

CAN PROFIBUS (X54)

The CAN PROFIBUS Connectors at X54 on the Open Board provide dedicated interface for CAN .

Pin	Signal
1	X_UART1_RXD, P_UART0_RXD
2	VCC_3V3
3	X_UART1_TXD, P_UART0_TXD
4	GND

Table 9: Pin description of Open board X54 Connector

GPIO Expansion Connector (X49)

The GPIO Expansion Connectors at X49 on the Open Board provide dedicated interface for GPIO .

PIN	GPIO	Muxxing
1	GND	
2	VCC_3V3	
3	GPIO0_18	X_USB1_DRVVBUS, GPIO0_18
4	GPIO2_1	X_GPIO2_1
5	GPIO3_13	X_USB0_DRVVBUS, GPIO3_13
6	GPIO2_0	X_GPIO2_0
7	GPIO0_31	X_GPIO0_31
8	GPIO0_29	X_GPIO0_29
9	GPIO0_19	X_GPIO0_19
10	GPIO3_4	X_GPIO3_4
11	GND	
12	VCC_3V3	

Table 10: Pin description of Open board X49 Connector

I2C Expansion (X53)

The I2C Expansion Connectors at X53 on the Open Board provide dedicated interface for I2C1 .

PIN	I2C	Muxxing
1	X_I2C1_SDA	X_I2C1_SDA, GPIO1_8
2	VCC_3V3	
3	X_I2C1_SCL	X_I2C1_SCL, GPIO1_9

4	GND	

Table 11: Pin description of Open board X53 Connector

SPI Expansion (X56)

The SPI interface SPI1 is accessible on the Expansion Board. On the PHYTEC Open Board, the SPI0 interface connects to the LCD connector. The LCD connector is also on the SPI0_CS0 signal. If the LCD on the Carrier Board requires SPI, then the SPI Flash on the SOM should be disabled using SOM jumper J22. This is because the SPI Flash on the SOM and the LCD connector are both connected as the SPI0 CS0 device. The LCD which comes with the phyCORE kit does not use the SPI interface, so disabling SPI Flash on the SOM is not required.

PIN	SPI	Muxxing
1	SPI1_D0	X_MCASP1_ACLKX, SPI1_D0, GPIO3_1
2	VCC_3V3	
3	SPI1_D1	X_MCASP1_FSX, SPI1_D1, GPIO3_2
4	VCC_3V3	
5	SPI1_CS0	X_SPI1_CS0, UART1_CTS
6	SPI1_SCK	X_MCASP1_AXR2, SPI1_SCK, GPIO3_0
7	SPI1_CS1	X_SPI1_CS1, UART1_RTS
8	GND	

Table 12: Pin description of Open board X56 Connector

UART Expansion (X51)

The UART Expansion Connectors at X51 on the Open Board provide dedicated interface for UART 2, 3, 4.

PIN	UART	Muxxing
1	UART2_TX	X_MMC1_D1, UART2_TX
2	VCC_3V3	
3	UART2_RX	X_MMX1_D0, UART2_RX
4	GND	
5	UART3_TX	X_MMC1_D3, UART3_TX
6	VCC_3V3	
7	UART3_RX	X_MMC1_D2, UART3_RX
8	GND	
9	UART4_TX	X_UART4_TX
10	VCC_3V3	
11	UART4_RX	X_UART4_RX
12	GND	

Table 13: Pin description of Open board X51 Connector

ADC-IN Expansion (X50)

The ADC-IN Expansion Connectors at X50 on the Open Board provide dedicated interface for ADC .

PIN	ADC
1	GND
2	VCC_3V3
3	AIN4
4	AIN0
5	AIN5
6	AIN1
7	AIN6
8	AIN2
9	AIN7
10	AIN3
11	GND
12	VCC_3V3

Table 14: Pin description of Open board X50 Connector

McASP (X14, X15, X16, X17)

The AM335x McASP0 interface routes to an audio codec at U20. This codec can be configured through the I2C0 bus at address 0x1A. There are also some jumpers for hardware configuration. The jumpers are described in Table 4.

Connector	Audio Feature
X14	microphone in
X15	headphones out
X16	mono out
X17	speakers out

Table 15: Pin description of Open board X50 Connector

Note : See jumper number JP5 JP13 in table number 4 for more details

Multiple connection of the device on the open board

UART0		UART1		UART2		UART3		UART4		SPI0		SPI1		I2C0		I2C1		GPIO
X27	9	X27	9	X.27	27	X.27	21	X51	9	X41	9	X.27	1	X41	20	X53	1	X27
X27	22	X27	11	X.27	29	X.27	25	X51	11	X41	10	X.27	5	X41	22	X53	3	X49
X54	1	X27	22	X51	1	X51	5			X41	11	X.27	11					X53
X54	3	X27	24	X51	3	X51	7			X41	12	X.27	20					X56
		X54	1									X.27	24					
		X54	3									X56	1					
		X56	5									X56	3					
		X56	7									X56	5					
												X56	6					
												X56	7					

Table 16: Multiple connection of the device on the open board
connector name in blue

Part II: PCM-051/phyCORE-AM335x System on Module

Part 2 of this two part manual provides detailed information on the phyCORE-AM335x System on Module (SOM) designed for custom integration into customer applications. The information in the following chapters is applicable to the 1358.2 PCB revision of the phyCORE-AM335x SOM.

Introduction

The phyCORE-AM335x is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and evaluation platform.
2. As insert-ready, fully functional phyCORE OEM modules, which can be

embedded directly into the user's peripheral hardware design.
Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware further reduce development time and expenses. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial designs issues and risks. For more information go to:
http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html
or
http://www.phytec.eu/europe/oem-integration/evaluation-start-up.html

The phyCORE-AM335x offers the following features

- Insert-ready, sub-miniature (44 x 50 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Texas Instruments AM335x microcontroller (ZCZ 324-pin PBGA package)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to two high-density (0.5 mm) Samtec connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- Max. 720 MHz core clock frequency
- Boot from NAND Flash, SPI Flash, or SD Card
- 512 MByte on-board NAND Flash1
- 512 MByte DDR3 SDRAM
- 2x High-Speed USB OTG ports
- 1x 10/100 MBit Ethernet interface
- 1x 10/100/1000 RGMII Ethernet interface
- Single supply voltage of 5V (max. 600mA) with on-board power management
- All controller required supplies generated on board
- Parallel LCD-Interface with an integrated touch interface and up to 24 data bits
- Support of standard 20 pin debug interface through JTAG connector

- 3x I²C interfaces
- 2x SPI interfaces
- 3x SD/MMC card interfaces
- Real-Time Clock
- 2x Multi-channel audio serial interfaces (McASP)

Block Diagram

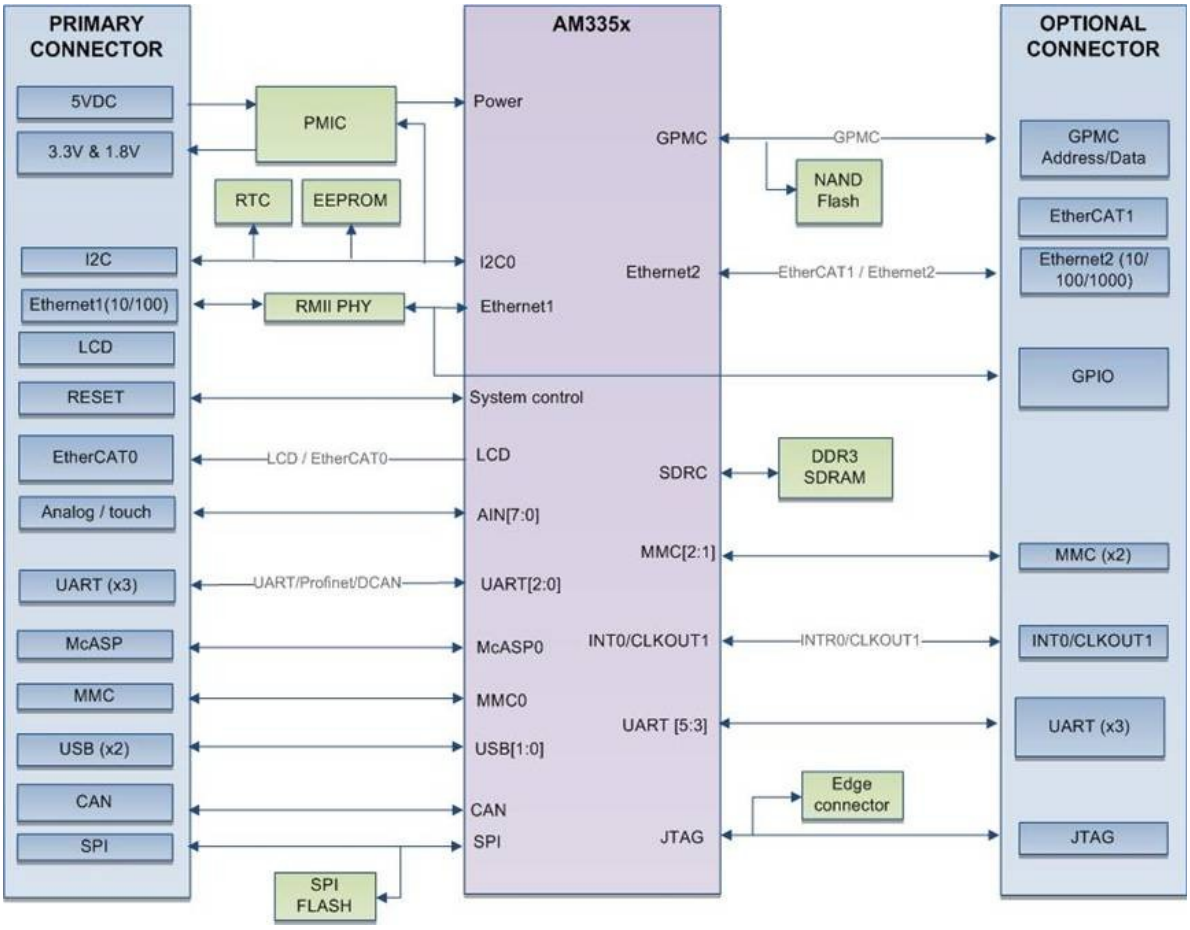


Figure 4: Block Diagram of the phyCORE-AM335x

View of the phyCORE-AM335x

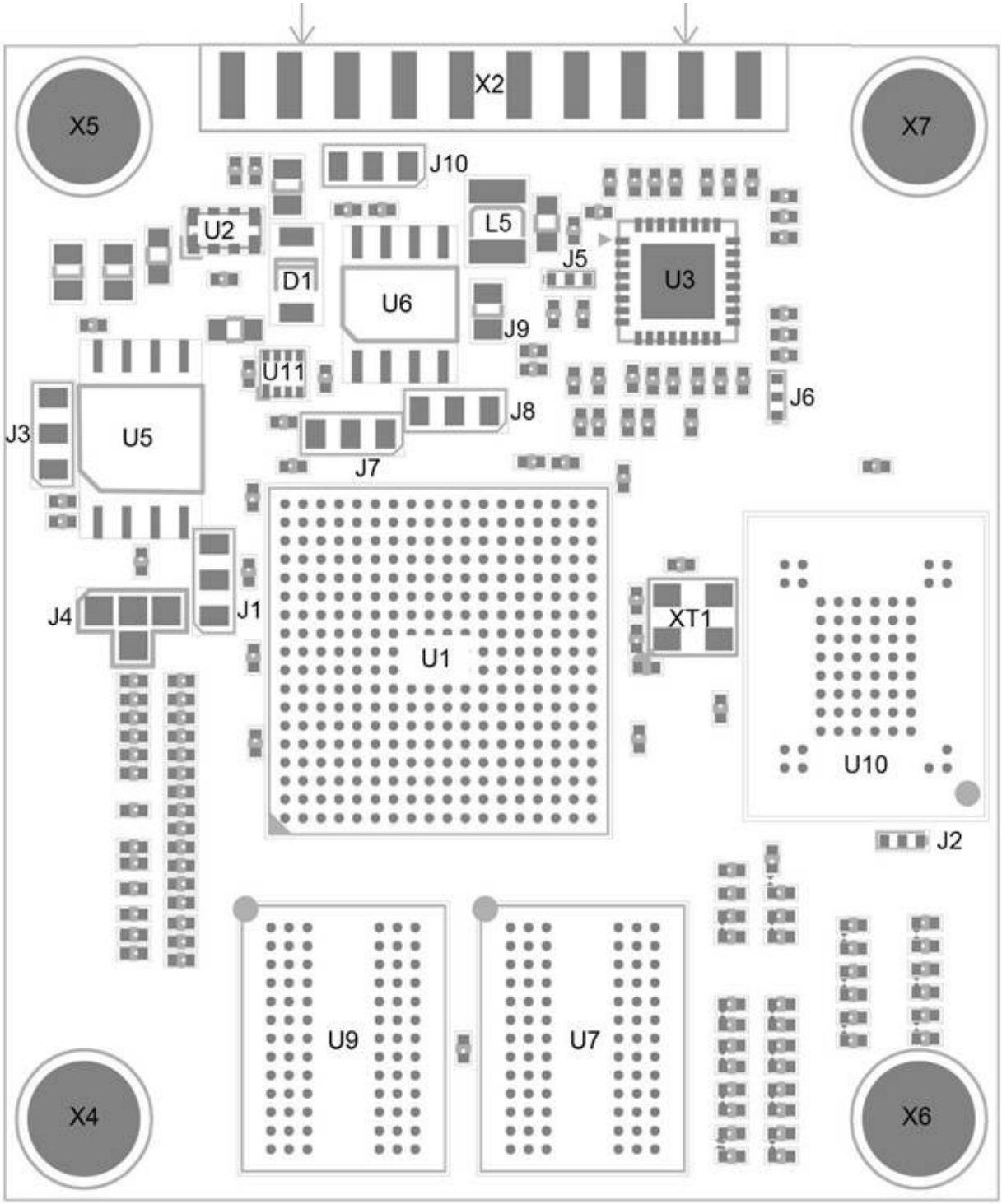


Figure 5: Top View of the phyCORE-AM335x (controller side)

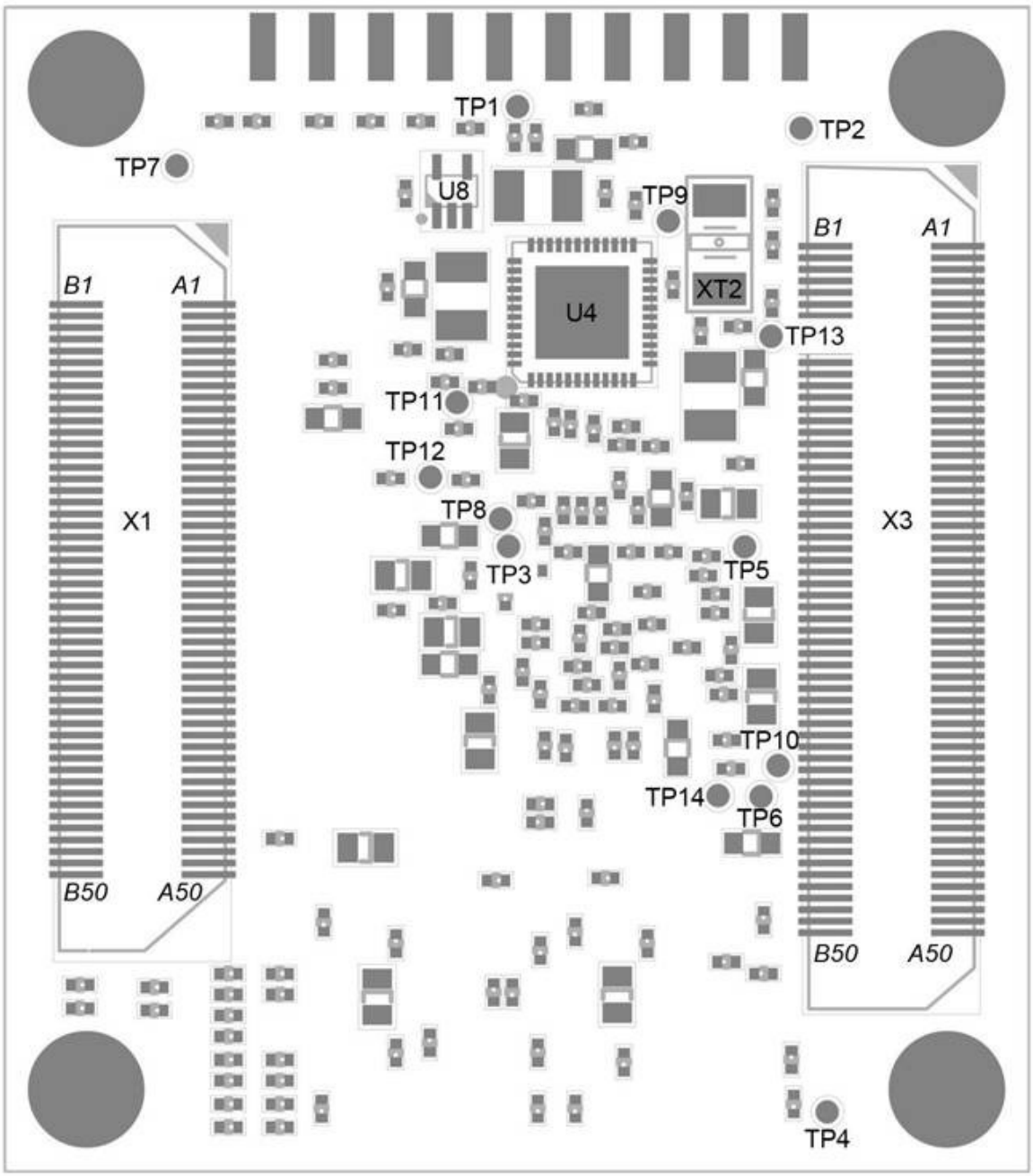


Figure 6: Bottom View of the phyCORE-AM335x (connector side)

Minimum Requirements to Operate the phyCORE-AM335x

Basic operation of the phyCORE-AM335x only requires supply of a +5.0 V input voltage with 1.0 Amp load and the corresponding GND connections. These supply pins are located at the phyCORE-Connector X3:

VCC_5V0 : Connector : X3 Pins : 1B, 2B, 3B, 5B

Connect all +5.0V VCC input pins to your power supply and at least the matching number of GND pins.
Corresponding GND : Connector : X3 Pins : 1A, 4A, 8A, 4B, 7B

Please refer to phyCORE Connectors and Pins for information on additional GND Pins located at the phyCORE-Connector X3.

phyCORE Connectors and Pins

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.
All controller signals extend to surface mount technology (SMT) connectors (0.5 mm) lining two sides of the module (referred to as the phyCORE-Connector). This allows the phyCORE-AM335x to be plugged into any target application like a big chip.
The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin A1, for example, is located in the upper left hand corner of the matrix looking down through the top of the SOM. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right for each connector (refer to Figure-4).

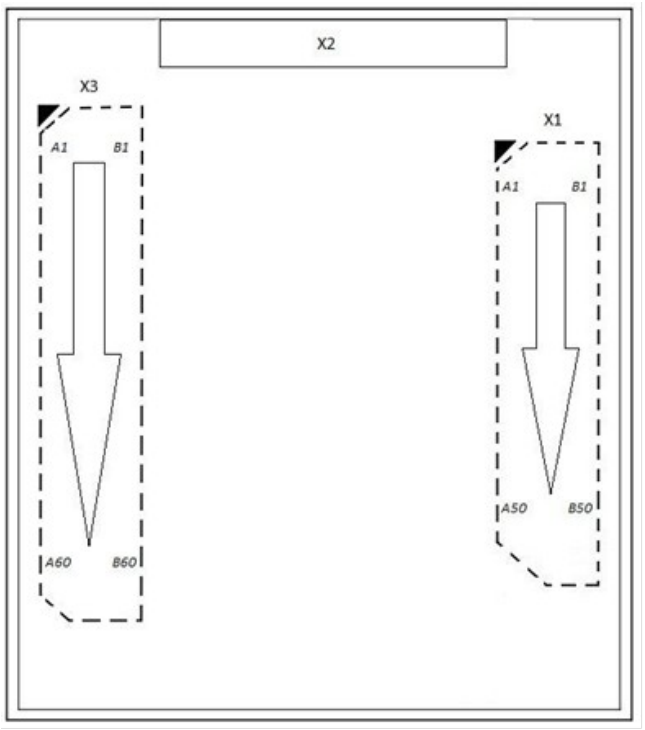


Figure 7: phyCORE Pinout Viewed Through the Top of the SOM

The tables Table 1, Table 2, Table 3 and Table 4 provide an overview of the pinout of the phyCORE-Connector with signal names and descriptions specific to the phyCORE-AM335x. It also lists the signal level interface voltages in the SL (Signal Level) column and the signal direction in the Type column.
Since most of the controller pins are multiplexed with multiple functions, the table relates only to the pin functions as they are used with PHYTEC's carrier board. This means that you can use any of the other pin multiplexed functions in your design (e.g. pin X1.A2, named X_RMII1_RXER_/MCASP1_FSX in the schematics, could alternately be used as SPI1_D1 or GPIO3_2 by making software changes).
The Texas Instruments AM335x is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the Texas Instruments AM335x Technical Reference Manual for details on its functions and features.

Pin Row X1A				
Pin #	**Signal**	**Type**	**SL**	**Description**
X1.1A	RMII_RXER / MCASP1_FSX	IO	VMMC_3P3V	Ethernet1 RMII Rx error or Multi-channel Audio Serial Port1 Tx frame sync
X1.2A	GND	-	-	Ground
X1.3A	RMII1_RXD0 / GPIO_2_21	IO	VMMC_3P3V	Ethernet1 RMII Rx data 0 or AM335x GPIO_2_21
X1.4A	RMII1_RXD1 / GPIO_2_20	IO		
X1.5A	-	-	-	Reserved, no-connect
X1.6A	-	-	-	Reserved, no-connect
X1.7A	GND	-	-	Ground
X1.8A	UART3_RX	IN	VMMC_3P3V	UART3 Rx data
X1.9A	UART3_TX	OUT	VMMC_3P3V	UART3 Tx data
X1.10A	RMII1_TXEN / MCASP1_AXR0	IO	VMMC_3P3V	Ethernet1 RMII Tx enable or Multi-channel Audio Serial Port 1 data 0
X1.11A	RMII1_TXD0 / GPIO_0_28	IO	VMMC_3P3V	Ethernet1 RMII Tx data 0 or AM335x GPIO_0_28
X1.12A	GND	-	-	Ground
X1.13A	RMII1_TXD1 / GPIO_0_21	IO	VMMC_3P3V	Ethernet1 RMII Tx data 1 or AM335x GPIO_0_28
X1.14A	MII1_COL MCASP1_AXR2	IO	VMMC_3P3V	Ethernet1 MII collision detect or Multi-channel Audio Serial Port 1 data 2
X1.15A	RMII1_CRS / MCASP1_ACLKX IO		VMMC_3P3V	Ethernet1 RMII carrier sense or Multi-channel Audio Serial Port 1 Tx bit clock
X1.16A	GPMC_AD1	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.17A	GND	-	-	Ground
X1.18A	RMII1_REFCLK / GPIO_0_29	IO	VMMC_3P3V	Ethernet1 RMII reference clock
X1.19A	-	-	-	Reserved, no-connect
X1.20A	-	-	-	Reserved, no-connect
X1.21A	-	-	-	Reserved, no-connect
X1.22A	GND	-	-	Ground

Pin Row X1A				
Pin #	**Signal**	**Type**	**SL**	**Description**
X1.23A	GPMC_AD0	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.24A	GPMC_AD2	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.25A	GPMC_AD4	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.26A	GPMC_AD5	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.27A	GND	-	-	Ground
X1.28A	GPMC_AD3	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.29A	GPMC_AD6	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.30A	GPMC_AD7	IO	VMMC_3P3V	GeneralPurposeMemoryControllerinterface Address/Data
X1.31A	-	-	-	Reserved, no-connect
X1.32A	GND-	-	-	Ground
X1.33A	GPMC_ADVn_ALE	OUT	VMMC_3P3V	GeneralPurposeMemoryControllerinterface address valid / address latch enable
X1.34A	GPMC_BE0n_CLE	OUT	VMMC_3P3V	General Purpose Memory Controller interface byte enable 0 / command latch enable
X1.35A	RGMII2_RCTL / MMC2_DAT0 / P_MII1_TXD3	IO	VAUX2_3P3V	Ethernet 2 RGMII Rx control or MMC/SDIO 2 data 2 or PRU Ethernet1 Tx data 3
X1.36A	RGMII2_TD3 / MMC2_DAT1 / P_MII1_TXD2	IO	VAUX2_3P3V	Ethernet 2 RGMII Tx data 3 or MMC/SDIO 2 data 1 or PRU Ethernet1 Tx data 2
X1.37A	GND	-	-	Ground
X1.38A				
X1.39A	RGMII2_TD2 / MMC2_DAT2 / P_MII1_TXD1	IO	VAUX2_3P3V	Ethernet 2 RGMII Tx data 2 or MMC/SDIO 2 data 2 or PRU Ethernet1 Tx data 1
X1.40A	RGMII2_TD0 / P_MII1_RXD3	IO	VAUX2_3P3V	Ethernet 2 RGMII Tx data 0 or PRUEthernet1 Rx data 3

Pin Row X1A				
Pin #	**Signal**	**Type**	**SL**	**Description**
X1.41A	RGMII2_TCLK / MMC2_DAT4 / P_MII1_RXD2	IO	VAUX2_3P3V	Ethernet 2 RGMII Tx data 2 or MMC/SDIO 2 data 2 or PRU Ethernet1 Tx data 1
X1.42A	GND	-	-	Ground
X1.43A	RGMII2_RCLK / MMC2_DAT5/ P_MII1_RXD1	IO	VAUX2_3P3V	Ethernet 2 RGMII Rx data 2 or MMC/SDIO 2 data 7 or PRU Ethernet1 Rx clock
X1.44A	RGMII2_RD2 / MMC2_DAT7 / P_MII1_MR1_CLK	IO	VAUX2_3P3V	Ethernet 2 RGMII Rx data 1 or PRU Ethernet1 Rx data valid
X1.45A	RGMII2_RD1 / P_MII1_RXDV	IO	VAUX2_3P3V	Ethernet 2 RGMII Rx data 1 or PRU Ethernet1 Rx data valid
X1.46A	RGMII2_RD0 / P_MII1_RXER	IO	VAUX2_3P3V	Ethernet 2 RGMII Rx data 0 or PRU Ethernet1 Rx error
X1.47A	GND	-	-	Ground
X1.48A	MMC2_CLK / P_MDIO_MDCLK	IO	VAUX2_3P3V	MMC/SDIO 2 clock or PRU Ethernet1 MDIO Clock
X1.49A	-	-	-	Reserved, no-connect
X1.50A	-	-	-	Reserved, no-connect

Table 17: Pinout of the phyCORE-Connector X1, Row A

Pin Row X1B				
Pin #	**Signal**	**Type**	**SL**	**Description**
X1.1B	X_SPI_WRn	PU	VMMC_3P3V	SPI FLASH write-protect (low-true)
X1.2B	MDIO_DATA	IO	VMMC_3P3V	Ethernet MDIO interface data
X1.3B	MDIO_CLK	OUT	VMMC_3P3V	Ethernet MDIO interface clock
X1.4B	GND	-	-	Ground
X1.5B	GPIO_3_18	IO	VMMC_3P3V	AM335x GPIO_3_18
X1.6B	MII1_RCTL / GPIO_3_4	IO	VMMC_3P3V	Ethernet MII1 Rx control or AM335x GPIO_3_4
X1.7B	TDI	IN	VMMC_3P3V	JTAG data in
X1.8B	TCK	IN	VMMC_3P3V	JTAG clock
X1.9B	GND	-	-	Ground

X1.10B	TDO	OUT	VMMC_3P3V	JTAG data out
X1.11B	TRSTn	IN	VMMC_3P3V	JTAG reset (low-true)
X1.12B	TMS	IN	VMMC_3P3V	JTAG mode select
X1.13B	-	-	-	Reserved, no-connect
X1.14B	GND	-	-	Ground
X1.15B	INTR1	IPU	VMMC_3P3V	AM335x Interrupt 1
X1.16B	X_INT_RTCn	OUT	VBAT_4I2C_RTC (3 V)	External RTC interrupt (low-true)
X1.17B	GPMC_WEn	OUT	VMMC_3P3V	General Purpose Memory Controller write enable
X1.18B	GPIO_3_8	IO	VMMC_3P3V	AM335x GPIO_3_8
X1.19B	GND	-	-	Ground
X1.20B	GPIO_3_7	IO	VMMC_3P3V	AM335x GPIO_3_7
X1.21B	GPMC_CS0n	OUT	VMMC_3P3V	General Purpose Memory Controller write enable
X1.22B	GPMC_OEN_REn	OUT	VMMC_3P3V	General Purpose Memory Controller output enable / read enable
X1.23B	GPMC_WAIT/P_MII0_COL	IO	VAUX2_3P3V	General Purpose Memory Controller WAIT / PRU Ethernet0 collision
X1.24B	GND	-	-	Ground
X1.25B	X_PMIC_POWER_EN	IN	5V PD	PMIC power enable
X1.26B	LCD_D21	OUT	VAUX2_3P3V	LCD data
X1.27B	LCD_D23	OUT	VAUX2_3P3V	LCD data
X1.28B	LCD_D22 / P_MII0_COL	IO	VAUX2_3P3V	LCD data / PRU Ethernet0 collision Detect
X1.29B	GND	-	-	Ground
X1.30B	LCD_D20	OUT	VAUX2_3P3V	LCD data
X1.31B	LCD_D19	OUT	VAUX2_3P3V	LCD data
X1.32B	LCD_D18	OUT	VAUX2_3P3V	LCD data
X1.33B	P_MII1_TXEN	OUT	VAUX2_3P3V	PRU Ethernet 1 MII Tx enable
X1.34B	GND	-	-	Ground
X1.35B	X_GPIO_CKSYNC	IO	VMMC_3P3V	PMIC clock-sync input or PMIC General-Purpose-Input-Output
X1.36B	LCD_D16	OUT	VAUX2_3P3V	LCD data

X1.37B	RGMII2_INT / MMC2_DAT3 / P_MII1_RXLINK	IO	VAUX2_3P3V	Ethernet 2 Rx data 3 or MMC/SDIO 2 data 6 or PRU Ethernet 1 Rx data 0
X1.38B	LCD_D17	OUT	VAUX2_3P3V	LCD data
X1.39B	GND	-	-	Ground
X1.40B	RGMII2_RD3 / MMC2_DAT6 / P_MII1_RXD0	IO	VAUX2_3P3V	Ethernet2 Rx data 3 or MMC/SDIO2 data 6 or PRU Ethernet1 Rx data 0
X1.41B	RGMII2_TD1 / P_MMI1_TXD0	IO	VAUX2_3P3V	Ethernet2 Tx data 1 or PRU Ethernet1 Tx data 0
X1.42B	RGMII2_TCTL / P_MII1_MT_CLK	IO	VAUX2_3P3V	Ethernet2 Tx control or PRU Ethernet1 Tx clock
X1.43B	-	-	-	Reserved, no-connect
X1.44B	GND	-	-	Ground
X1.45B	CLKOUT1	OUT	VMMC_3P3V	AM335x CLKOUT1, 25 MHz
X1.46B	MMC2_CMD / P_MDIO_DATA	IO	VAUX2_3P3V	MMC/SDIO2 command or PRU MDIO Data
X1.47B	GPIO_1_30	IO	VMMC_3P3V	AM335x GPIO_1_30
X1.48B	GPIO_1_31	IO	VMMC_3P3V	AM335x GPIO_1_31
X1.49B	GND	-	-	Ground
X1.50B	-		-	Reserved, no-connect

Table 18: Pinout of the phyCORE-Connector X1, Row B

Pin Row X3A				
Pin #	**Signal**	**Type**	**SL**	**Description**
X3.A1	GND	**-**	**-**	Ground 0 V
X3.A2	VBAT_IN_4RTC	PWR	3 V - 5 V	Optional always-on power for the Real-Time Clock (RTC). If a backup batter is not used, connect this pin to the primary 5V supply
X3.A3	VDIG1_1P8V	REF	VDIG1_1P8V	1.8 V reference voltage out
X3.A4	GND	-	-	Ground
X3.A5	AM335_NMIn	IPU	VMMC_3P3V	Non-maskable interrupt to the AM335x Processor

X3.A6	ETH1_RXn	IO	VDD_3PV_ETH	Ethernet PHY data minus
X3.A7	ETH1_RXp	IO	VDD_3PV_ETH	Ethernet PHY data plus
X3.A8	GND	-	-	Ground
X3.A9	ETH1_TXn	IO	VDD_3PV_ETH	Ethernet PHY data minus
X3.A10	ETH1_TXp	IO	VDD_3PV_ETH	Ethernet PHY data plus
X3.A11	PB_RESETn	IN	VMMC_3P3V	Push-button reset
X3.A12	GND	-	-	Ground
X3.A13	ETH_LED2 / INTSELn	IO	VMMC_3P3V	Ethernet configuration input and speed LED control output
X3.A14	ETH_LED1 / REGOFF	IO	VMMC_3P3V	Ethernet configuration input and activity LED control output
X3.A15	SPI0_SCLK	OUT	VMMC_3P3V	Serial Peripheral Interface 0 clock
X3.A16	GND	-	-	Ground
X3.A17	SPI0_CS0	OUT	VMMC_3P3V	Serial Peripheral Interface 0 chip select 0. CS0 is not externally available in the default SOM configuration with SPI Flash installed
X3.A18	SPI0_CS1 / MMC0_SDCD	IO	VMMC_3P3V	Serial Peripheral Interface 0 chip select 1 or MMC/SD0 Card Detect
X3.A19	I2C0_SCL	IO	VMMC_3P3V	I²C bus 0 clock. Some I2C0 address are reserved. See Section 1.9.6
X3.A20	I2C0_SDA	IO	VMMC_3P3V	I²C bus 0 data.
X3.A21	GND	-	-	Ground
X3.A22	MCASP0_AXR0	IO	VMMC_3P3V	Multi-channel Audio Serial Port 0 data 0
X3.A23	GPIO_3_17	IO	VMMC_3P3V	AM335x GPIO3_17
X3.A24	DCAN0_RX	IN	VMMC_3P3V	CAN0 Rx data
X3.A25	DCAN0_TX	OUT	VMMC_3P3V	CAN0 Tx data
X3.A26	GND	-	-	-
X3.A27	MCASP0_AHCLKX	IO	VMMC_3P3V	Multi-channel Audio Serial Port 0 Tx bit clock
X3.A28	MCASP0_AXR1	IO	VMMC_3P3V	Multi-channel Audio Serial Port 0 data 1

X3.A29	MCASP0_FSX	IO	VMMC_3P3V	Multi-channel Audio Serial Port 0 Tx frame sync
X3.A30	PORZ	OUT	VMMC_3P3V	Power-on reset (low-true)
X3.A31	GND	IO	-	Ground
X3.A32	UART0_TXD	OUT	VMMC_3P3V	UART0 Tx data from AM335x
X3.A33	UART0_RXD	IN	VMMC_3P3V	UART0 Rx data to AM335x
X3.A34	SPI0_D0	IN	VMMC_3P3V	Serial Peripheral Interface 0 Master-In-Slave-Out (MISO) data
X3.A35	SPI0_D1	OUT	VMMC_3P3V	Serial Peripheral Interface 0 Master-Out-Slave-In (MOSI) data
X3.A36	GND	-	-	Ground
X3.A37	LCD_D3 / P_MII0_TXD2	IO	VMMC_3P3V	LCD data 3 or PRU Ethernet 0 Tx data 2
X3.A38	LCD_D2 / P_MII0_TXD3	IO	VMMC_3P3V	LCD data 2 or PRU Ethernet 0 Tx data 3
X3.A39	LCD_D4 / P_MII0_TXD1	IO	VAUX2_3P3V	LCD data 4 or PRU Ethernet 0 Tx data 1
X3.A40	LCD_D5 / P_MII0_TXD0	IO	VAUX2_3P3V	LCD data 5 or PRU Ethernet 0 Tx data 0
X3.A41	GND	-	-	Ground
X3.A42	LCD_D0 / P_MII0_MT_CLK	IO	VAUX2_3P3V	LCD data 0 or PRU Ethernet 0 Tx clock
X3.A43	LCD_D1 / P_MII0_TXEN	OUT	VAUX2_3P3V	LCD data 1 or PRU Ethernet 0 Tx enable
X3.A44	LCD_D13 / P_MII0_RXER	IO	VAUX2_3P3V	LCD data 13 or PRU Ethernet 0 Rx error
X3.A45	LCD_HSYNC	OUT	VAUX2_3P3V	LCD horizontal sync
X3.A46	GND	-	-	Ground
X3.A47	USB0_DM	DIFF100	VAUX33_3P3V	USB 0 data minus
X3.A48	USB0_DP	DIFF100	VAUX33_3P3V	USB 0 data plus
X3.A49	LCD_D12 / P_MII0_RXLINK	IO	VMMC_3P3V	LCD data 12 or PRU Ethernet 0 Rx link
X3.A50	LCD_BIAS_EN / P_MII1_CRS	IO	VMMC_3P3V	LCD AC bias enable or PRU Ethernet 1 carrier sense
X3.A51	GND	-	-	Ground
X3.A52	LCD_D8 / P_MII0_RXD3	IO	VMMC_3P3V	LCD data 8 or PRU Ethernet 0 Rx data 3
X3.A53	LCD_D14 / P_MII0_MR_CLK	IO	VMMC_3P3V	LCD data 14 or PRU Ethernet 0 Rx clock
X3.A54	LCD_D15 / P_MII0_RXDV	IO	VMMC_3P3V	LCD data 15 or PRU Ethernet Rx data

				Valid
X3.A55	LCD_D6	OUT	VMMC_3P3V	LCD data 6
X3.A56	GND	-	-	Ground
X3.A57	LCD_D7	OUT	VMMC_3P3V	LCD data 7
X3.A58	LCD_D9 / P_MII0_RXD2	IO	VMMC_3P3V	LCD data 9 or PRU Ethernet 0 Rx data 2
X3.A59	LCD_D10 / P_MII0_RXD1	IO	VMMC_3P3V	LCD data 10 or PRU Ethernet 0 Rx data 1
X3.A60	UART2_RX	IN	VAUX2_3P3V	UART 2 Rx data to AM335x

Table 19: Pinout of the phyCORE-Connector X3, Row A

Pin Row X3B				
Pin #	**Signal**	**Type**	**SL**	**Description**
X3.B1	VDD_5V_IN	PWR	VDD_5V_IN	3.6 V - 5 Volt power input
X3.B2	VDD_5V_IN	PWR	VDD_5V_IN	3.6 V - 5 Volt power input
X3.B3	GND	-	-	Ground
X3.B4	VDD_5V_IN	PWR	VDD_5V_IN	3.6 V - 5 Volt power input
X3.B5	VDD_5V_IN	PWR	VDD_5V_IN	3.6 V - 5 Volt power input
X3.B6	VAUX2_3P3V	REF	VAUX2_3P3V	3.3 V reference Voltage
X3.B7	GND	-	-	Ground
X3.B8	UART1_CTS	IN	VMMC_3P3V	UART1 clear to send
X3.B9	UART1_RTS	OUT	VMMC_3P3V	UART1 ready to send
X3.B10	UART1_TX / P_UART0_TX	OUT	VMMC_3P3V	UART 1 Tx data or PRU UART0 Tx data
X3.B11	UART1_RX / P_UART0_RX	IN	VMMC_3P3V	UART 1 Rx data or PRU UART0 Rx data
X3.B12	GND	-	-	Ground
X3.B13	RESET_OUTn	OUT	VMMC_3P3V	Warm reset output
X3.B14	PB_POWER	IN	VDD_5V_IN	Push-button power control
X3.B15	GPIO_3_19	IO	VMMC_3P3V	AM335x GPIO_3_19
X3.B16	MCASP0_ACLKX	IO	VMMC_3P3V	Multi-channel Audio Serial Port 0 Tx bit clock
X3.B17	GND	-	-	Ground
X3.B18	USB1_DP	DIFF100	VAUX33_3P3V	USB 1 data plus
X3.B19	USB1_DM	DIFF100	VAUX33_3P3	USB 1 data minus

			V	
X3.B20	GND	-	-	Ground
X3.B21	USB1_DRVVBUS	OUT	VAUX33_3P3V	USB 1 VBUS control output
X3.B22	USB1_VBUS	USB	5V_PD	USB 1 bus voltage
X3.B23	USB1_ID	IN	VAUX1_1P8V	USB 1 port identification
X3.B24	USB1_CE	OUT	VAUX33_3P3V	USB 1 port charger enable
X3.B25	GND	-	-	Ground
X3.B26	ECAP0_IN_PWM0_OUT	IO	VMMC_3P3V	Enhanced Capture 0 input or Auxiliary Pulse-Width Modulated 0 output
X3.B27	GNDA_ADC	-	-	Analog ground
X3.B28	AIN7	analog	VPLL_1P8V	AM335x analog input/output 7
X3.B29	AIN6	analog	VPLL_1P8V	AM335x analog input/output 6
X3.B30	GNDA_ADC	-	-	Analog ground
X3.B31	AIN5	analog	VPLL_1P8V	AM335x analog input/output 5
X3.B32	AIN4	analog	VPLL_1P8V	AM335x analog input/output 4
X3.B33	GNDA_ADC	-	-	Analog ground
X3.B34	AIN2	analog	VPLL_1P8V	AM335x analog input/output 2
X3.B35	AIN3	analog	VPLL_1P8V	AM335x analog input/output 3
X3.B36	GNDA_ADC	-	-	Analog ground
X3.B37	AIN1	analog	VPLL_1P8V	AM335x analog input/output 1
X3.B38	AIN0	analog	VPLL_1P8V	AM335x analog input/output 0
X3.B39	AM335_EXT_WAKEUP	IN	VDIG2_1P8V	AM335x processor external wakeup
X3.B40	GND	-	-	Ground
X3.B41	USB0_VBUS	IN	5V_PD	USB 0 bus Voltage
X3.B42	USB0_DRVVBUS	OUT	VAUX33_3P3V	USB 0 VBUS control output
X3.B43	USB0_ID	IN	VAUX1_1P8V	USB 0 port identification
X3.B44	USB0_CE	OUT	VAUX33_3P3V	USB 0 charger enable
X3.B45	GND	-	-	Ground
X3.B46	LCD_PCLK / P_MII0_CRS	IN	VMMC_3P3V	LCD pixel clock or PRU Ethernet 0 carrier

				sense
X3.B47	LCD_VSYNC	OUT	VMMC_3P3V	LCD vertical sync
X3.B48	GND	-	-	Ground
X3.B49	LCD_D11 / P_MII0_RXD0	IO	VMMC_3P3V	LCD data 11 or PRU Ethernet 0 Rx data
X3.B50	GPIO_1_9	IO	VMMC_3P3V	AM335x GPIO_1_9
X3.B51	GPIO_1_8	IO	VMMC_3P3V	AM335x GPIO_1_8
X3.B52	GND	-	-	Ground
X3.B53	MMC0_CLK	IO	VAUX2_3P3V	MMC / SDIO 0 clock
X3.B54	MMC0_CMD	IO	VAUX2_3P3V	MMC / SDIO 0 command
X3.B55	MMC0_D0	IO	VAUX2_3P3V	MMC / SDIO 0 data 0
X3.B56	MMC0_D1	IO	VAUX2_3P3V	MMC / SDIO 0 data 1
X3.B57	GND	-	-	Ground
X3.B58	MMC0_D2	IO	VAUX2_3P3V	MMC / SDIO 0 data 2
X3.B59	MMC0_D3	IO	VAUX2_3P3V	MMC / SDIO 0 data 3
X3.B60	UART2_TX	OUT	VAUX2_3P3V	UART 2 Tx data to Carrier Board

Table 20: Pinout of the phyCORE-Connector X3, Row B

Jumpers

For configuration purposes, the phyCORE-AM335x has ten solder jumpers, all of which have been installed prior to delivery. Figure 5 indicates the location of the solder jumpers on the board. The ten solder jumpers are located on the top side of the module (opposite side from connectors). No solder jumpers are located on the bottom side of the module (the connector side). Table 5 below provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-AM335x to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.
Please pay special attention to the "TYPE" column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc…). The jumpers are either 0805 package or 0402 package with a 1/8W or larger power rating.

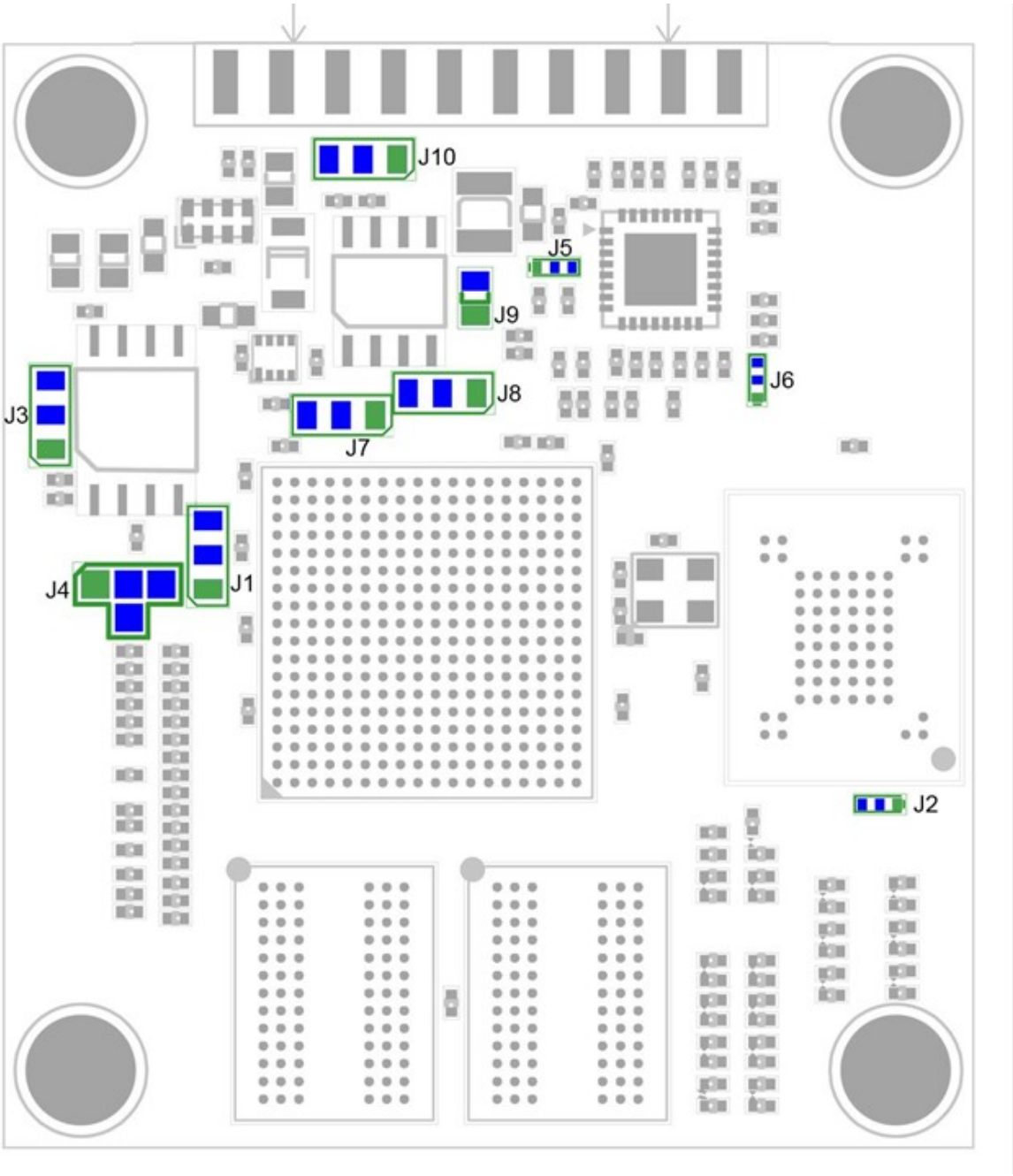


Figure 8: Jumper Locations (Top View)

The jumpers on the AM335x SOM have the following functions:

Jumper	Description	Type
J1	J1 routes CLKOUT1 to either the phyCORE or to the ETH1 PHY.	0R (0805)
1+2	CLKOUT1 normally connects to the phyCORE for use on the Carrier Board	
2+3	CLKOUT1 can connect to the ETH1 PHY for MII mode. This is one of many hardware changes needed to run the PHY in MII mode instead of RMII mode.	
J2	J2 connects the low-true write-protect input of the NAND-Flash (U10) to either PORZ or to GND.	0R (0402)
1+2	NAND_WPn connects to GND. This will prevent data corruption during power-up. FLASH is writable.	
2+3	**NAND-WPn connects to PORz. FLASH is not writable.**	
J3	J3 connects the HOLDn input of the SPI Flash (U5) to 3.3 V or GND.	0R (0805)
1+2	HOLDn is low. SPI Flash is disabled.	
2+3	**HOLDn is high. SPI Flash works normally.**	
J4	J4 connects the low-true write-protect input of the SPI-Flash (U5) to PORZ, GND, or X_SPI_WPn.	0R (0805)
1+2	SPI_WPn is controlled externally with the X_SPI_WPn signal	
2+3	SPI_WPn is low. SPI is not writable.	
2+4	**SPI_WPn connects to PORZ. This prevents data corruption during power-up. SPI Flash is writable.**	
J5	Route RMII1_REFCLK signal	0R (0402)
1+2	**Routes RMII1_REFCLK/GPIO0_29 to the phyCORE connector as a GPIO signal**	

2+3	Routes RMII1_REFCLK to the ETH1 PHY refclk input. Do not use.	
J6	Selects the COL/CRS PHY signal for ETH1	0R (0402)
1+2	**Selects the COL/CRS PHY signal for ETH1 in RMII mode**	
2+3	Selects the COL/CRS PHY signal for ETH1 in MII mode.	
J7	J7 sets the I²C EEPROM (U6) address bit A1 high or low.	0R (0805)
1+2	**I²C EEPROM A1 is high**	
2+3	I²C EEPROM A1 is low	
J8	J8 sets the I²C EEPROM (U6) address bit A2 high or low.	0R (0805)
1+2	I²C EEPROM A2 is high	
2+3	**I²C EEPROM A2 is low**	
J9	J9 sets the write-protection for the I²C EEPROM (U6)	0R (0805)
closed	**I²C EERPROM is writable**	
open	I²C EEPROM is write-protected	
J10	Selects the PMICs VBACKUP input source	0R (0805)
1+2	VBACKUP connects to the main system power. The RTC does not run when the system is off	
2+3	VBACKUP connects to the VBAT_IN_4RTC backup battery supply from the carrier board. The RTC runs when the system is off	

Table 21: SOM Jumper Settings
Defaults are in bold blue text

Power

phyCORE-AM335x The phyCORE-AM335x operates off of a single 5.0V system power supply. The phyCORE-AM335x includes the option to provide a 3.0V backup supply to power the Real-Time Clock (RTC) on the phyCORE-AM335x when the system power supply is off. The following sections of this chapter describe the power design of the phyCORE-AM335x.

Primary System Power (VDD_5V_IN)

The phyCORE-AM335x operates off of a primary voltage supply with a nominal value of +5.0.V. On-board switch-ing regulators generate the 1.1V, 1.5V, 1.8V and 3.3 V voltage supplies required by the AM335x processor and on-board components from the primary 5.0V supplied to the SOM.

For proper operation the phyCORE-AM335x must be supplied with a voltage source of 5.0V ±5 % with at least 1.0 Amp capacity at the VCC pins on the phyCORE-Connector X3.

VDD_5V_IN: X3 1B, 2B, 3B, 5B

Connect all +5V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X3 1A, 4A, 8A, 4B, 7B.

Optional Backup Power (VBAT_IN_4RTC)

The phyCORE-AM335x Carrier Board includes a battery to power the SOM's Real-Time Clock (RTC) when the main power is off. The battery may be replaced when the system is running on main power without disturbing the RTC.There are two RTCs on the AM335x-SOM.

The RTC in the TPS65910A3 PMIC includes alarm and timekeeping functions. This RTC is supplied by the backup battery voltage VBAT_IN_4RTC, when present, if the main power supply is off.

The SOM also provides an ordering option to populate an additional, external RTC at U2. This external RTC uses less power than the RTC integrated in the PMIC, and it could be used where very-low battery power is important. The external RTC typically uses 350 nA. The PMIC RTC typically uses 6 uA. To optimize the power-saving when using the external RTC, a low-power supervisory device must also be added. This supplies the power to the external RTC from the system, when it is on, or from the backup battery, when the system is off, using very low supply current.

The AM335x processor also includes an integrated RTC. However, the RTC integrated in the AM335x uses signif-icantly more power than the RTC in the PMIC. Because of this power disadvantage, the SOM has not been designed to support the AM335x RTC when the primary system power is off. Carrier Boards for applications not requiring a backup mode should connect the VBAT pin to the VDD_5V_IN primary system power supply.

Power Management IC (U4)

The phyCORE-AM335x provides a Texas Instruments TPS65910A3 Power Management IC (PMIC) at U4. The PMIC sources the different voltages required by the processor and on-board components. Figure 6 presents a graph-ical depiction of the SOM powering scheme.
The TPS65910A3 supports many functions including an integrated RTC and different power management func-tions. It is connected to the AM335x via the I2C0 interface. The I2C0 addresses of the TPS65910A3 PMIC are 0x2D and 0x412 (hexadecimal). Refer to the Texas Instruments TPS65910 datasheet for details about the PMIC's registers and operation.

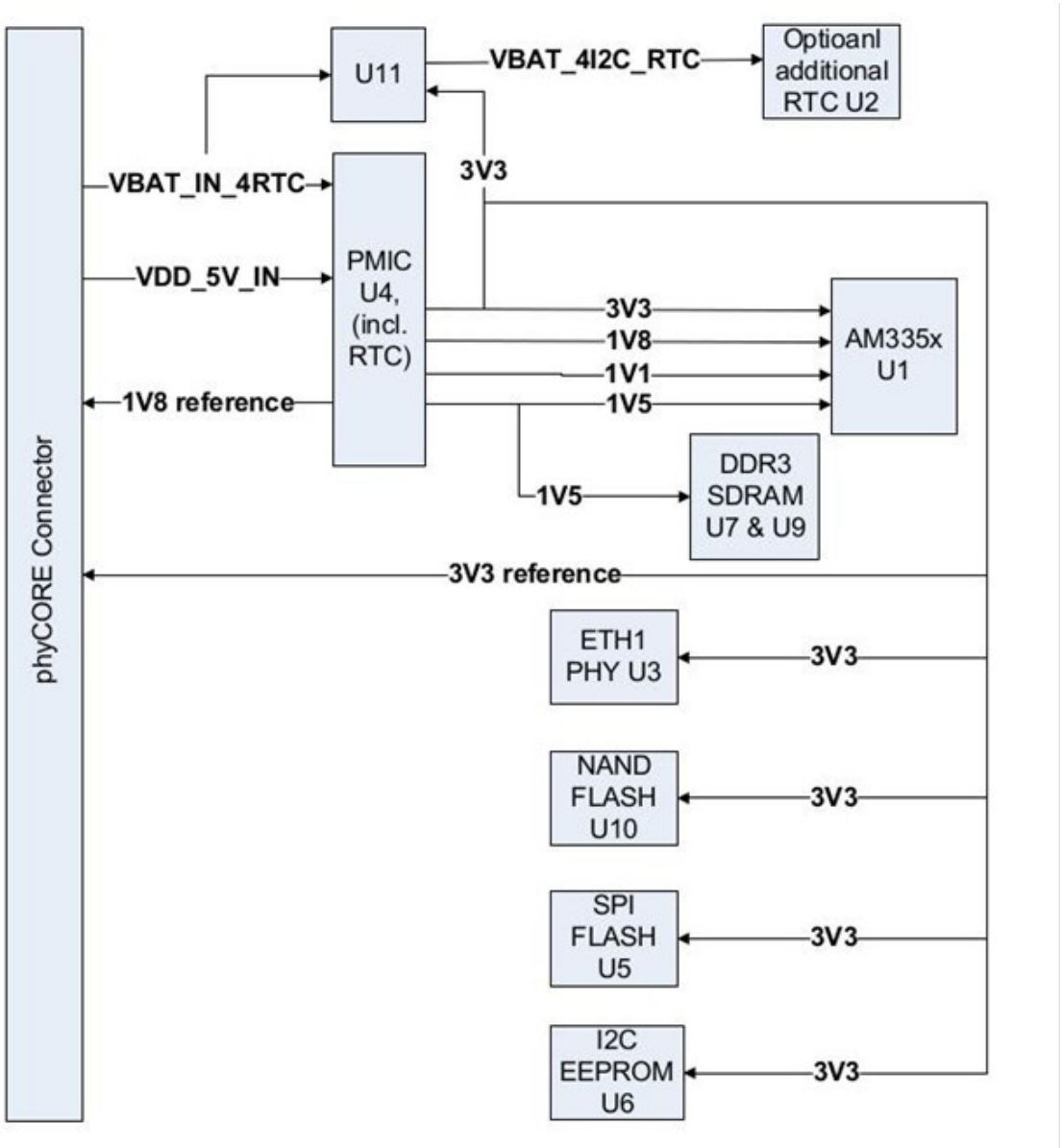


Figure 9: AM335x SOM Power Scheme

Backup Battery Management

When jumper J10 on the SOM is set to its default position, the RTC in the PMIC is powered off when the system is powered off. But when jumper J10 is moved to (2+3) the rTC in the PMIC is powered by the VBAT_IN_4RTC supply. TPS65910A3 PMIC includes a backup battery switch connecting its VRTC regulator input to the main power supply (VDD_5V_IN) or to a backup battery supply (VBAT_IN_4RTC) depending on which of these input supplies has the higher voltage level.

The VRTC supply is maintained during a backup state as long as the VBAT_IN_4RTC voltage is above 2.1V. The VRTC backup domain functions include the 32-kHz oscillator and the backup registers.When the system's main power is on, the backup battery on the Carrier Board can be charged from the primary supply, VDD_5V_IN, through a charger integrated in the TPS65910A3. The backup battery charge voltage and enable are controlled through the BBCH_REG register. The contents of this register are maintained during the device backup state.

Real-Time Clock (RTC)

There are three RTCs on the AM335x-SOM. The default RTC is the one integrated in the TPS65910A3 PMIC. This RTC includes alarm and timekeeping func-tions. The RTC is supplied by the main system power when it is on, and by the backup battery voltage VBAT_IN_4RTC, when present, if the main power supply is off and the jumper J2 has been moved from its default position of (1+2) to position (2+3).

The SOM also provides an ordering option to populate an additional, external RTC at U2. This external RTC uses less power than the RTC integrated in the PMIC, and it could be used where very-low battery power is important. The external RTC typically uses 350 nA. The PMIC RTC typically uses 6 uA. To optimize the power-saving when using the external RTC, a low-power supervisory device (U11) must also be populated. The supervisor supplies the power to the external RTC from the system, when it is on, or from the VBAT_IN_4RTC backup battery supply, when the system is off, using very low operating current.

The AM335x processor also includes an integrated RTC. However, the RTC integrated in the AM335x uses signif-icantly more power than the RTC in the PMIC. Because of this power disadvantage, the SOM has not been designed to support the AM335x RTC when the primary system power is off.

The open-collector output signals X_INT_RTCn from the external RTC and X_MII1_RCTL/_GPIO3_4 from the PMIC are provided to drive an external power wake circuit not provided on the SOM allowing the system to wake from sleep at a specified time.

System Configuration and Booting

The phyCORE-AM335x boots from an internal ROM which implements a boot sequence as described in the Initialization chapter of the AM335x Technical Reference Manual from Texas Instruments. Briefly, the AM335x latches the SYSBOOT[4:0] signals on the rising edge of the power-on reset signal to determine the boot order.

The following Table 6 shows the different boot orders which can be selected by configuring the SYSBOOT[4:0] signals. Please note that only configurations allowed by Texas Instruments are listed in the table. The value is set with resistors on the SOM, which can be changed as BOM stuffing options. The default boot order can also be over-ridden with JP3 (SD_Boot) jumper.The AM335x implements the boot order by accessing each peripheral in its list and searching it for a valid image. It boots from the first peripheral which contains a valid boot image. If it does not find a valid image, it proceeds to the next peripheral in its list. Boot speed can be increased by ensuring that the normal boot device of a production system is configured to be the first device in the boot sequence.

The default phyCORE-AM335x module comes with the boot configuration set to '**10011**', so the system tries to boot from NAND-Flash, NAND-I2C, MMC0 and UART0 in this order.

Boot Mode Selection X_LCD_D[4:0]	**Booting Device Order**			
	1st	**2nd**	**3rd**	**4th**
00010	UART0	SPI0	NAND	NANDI2C
00110	EMAC1	SPI0	NAND	NANDI2C
01011	USB0	NAND	SPI0	MMC0
10010	NAND	NANDI2C	USB0	UART0
10011	**NAND**	**NANDI2C**	**MMC0**	**UART0**
10100	NAND	NANDI2C	SPI0	EMAC1
10110	SPI0	MMC0	UART0	EMAC1
10111	MMC0	SPI0	UART0	USB0
11000	SPI0	MMC0	USB0	UART0
11001	SPI0	MMC0	EMAC1	UART0
11100	MMC1	MMC0	UART0	USB0

Table 22: Boot Device Order of AM335x Module
Defaults are in **bold blue** text

System Memory

The phyCORE-AM335x provides four types of on-board memory:

- DDR3 SDRAM: 512 MByte
- NAND Flash: 512 MByte

These are described in the following sections

DDR3-SDRAM (U7, U9)

The RAM memory of the phyCORE-AM335x is comprised of two 8-bit wide DDR3-SDRAM chips at U7 and U9.The effective bus is 16-bits wide. The chips are connected to the dedicated DDR interface called the Extended Memory Interface (EMIF) of the AM335x processor.

Typically the DDR3-SDRAM initialization is performed by a boot loader or operating

system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized through the appropriate SDRAM configuration registers on the AM335x controller. Refer to the AM335x Technical Reference Manual about accessing and configuring these registers.
The SDRAM memory addresses begin at address 0x80000000.

NAND Flash Memory (U10)

The use of NAND flash as non-volatile memory on the phyCORE-AM335x provides an easily reprogrammable means of code storage.

The NAND Flash memory is connected to the AM335x GPMC interface with a bus-width of 8-bits.

SPI Flash Memory (U5)

The phyCORE-AM335x can be populated with a SPI Flash memory device as an ordering option. This would be suitable for applications which require a small code footprint or small RTOSes.

Using a SPI Flash can eliminate the need to install NAND Flash memory on the SOM. This could reduce BOM costs, free up the NAND signals for other devices on the AM335x GPMC interface, and remove the need for doing the bad block management that is required when using NAND Flash

I²C EEPROM (U6)

The phyCORE-AM335x can be populated with a non-volatile 4 KB EEPROM with an I²C interface as an ordering option. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 0 on the AM335x. Two solder jumpers are provided to set two of the lower address bits: J7 and J8. Write protection to the device is accomplished with jumper J9.

Setting the EEPROM Lower Address Bits (J7, J8)

The 4 KB I²C EEPROM populating U2 on the phyCORE-AM335x SOM allows the user to configure the lower address bits A0, A1, and A2. The four upper address bits of the 7-bit address are fixed at ‘1010’. On the SOM, A0 is tied to GND. J7 sets address bit A1. And J8 sets address bit A2.
Table 7 below shows the resulting seven bit I²C device address for the four possible jumper configurations.

U6 I²C Device Address	J7	J8
1010 000	2 + 3	2 + 3
1010 010	2 + 3	1 + 2
1010 100	**1 + 2**	**2 + 3**
1010 110	1+2	1+2

Table 23: U6 EEPROM I²C Address via J7 and J8 Defaults are in **bold blue** text

EEPROM Write Protection Control (J9)

Jumper J9 controls write access to the EEPROM (U6) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J9
Write access allowed	**closed**
Write protected	**open**

Table 24: EEPROM Write Protection States Via J9
Defaults are in **bold blue** text

Memory Model

There is no special address decoding device on the phyCORE-AM335x, which means that the memory model is given according to the memory mapping of the AM335x. Please refer to the AM335x Technical Reference Manual

SD / MMC Card Interfaces

The phyCORE-AM335x includes three SD / MMC Card interfaces: MMC0, MMC1 and MMC2. The MMC0 interface signals including four of its data signals are identified on the phyCORE connector. The other four MMC0 data signals and all of the MMC1 and MMC2 signals are multiplexed on other signals. See the AM335x datasheet for all signal multiplexing options. Table 9 shows the location of the MMC0 interface signals on the phyCORE-Con-nector.

Pin #	Signal	IO	SL	Description
X3.B54	X_MMC0_CMD	IO	3.3V	SD/MMC0 command
X3.B53	X_MMC0_CLK	OUT	3.3V	SD/MMC0 clock
X3.B55	X_MMC0_DAT0	IO	3.3V	SD/MMC0 data bit 0
X3.B56	X_MMC0_DAT1	IO	3.3V	SD/MMC0 data bit 1
X3.B58	X_MMC0_DAT2	IO	3.3V	SD/MMC0 data bit 2
X3.B59	X_MMC0_DAT3	IO	3.3V	SD/MMC0 data bit 3
X3.B18	X_MMC0_SDCD	IN	3.3V	SD/MMC0 card detect

Table 25: Locations of Named SD/MMC0 Card Interface Signals on phyCORE Connector X3

Serial Interfaces

The phyCORE-AM335x provides many different serial interfaces, some of which are equipped with a transceiver to allow direct connection to external devices:

- Six high speed UART interfaces with up to 3.6Mbps. One of these, UART1, provides hardware flow control (RTS and CTS signals).
- Two high speed USB 2.0 OTG interfaces with integrated transceivers
- One two-port 10/100/1000 EMAC supporting MII, RMII and RGMII. The phyCORE-AM335x includes a 10/100 RMII Ethernet transceiver on one of these two Ethernet ports.
- One two-port 10/100 EMAC in the PRU which supports EtherCAT.
- One Profibus interface
- Three I²C interfaces
- Two Serial Peripheral Interface (SPI) interfaces
- Two CAN interfaces
- Two Multichannel Audio Serial Port (McASP) interfaces

The following sections of this section detail each of these serial interfaces

Universal Asynchronous Receiver/Transmitter Interfaces (UARTs)

The phyCORE-AM335x provides six high speed universal asynchronous interface with up to 3.6 Mbps. These are part of the AM335x MPU. All of these UARTs support hardware flow control with RTS and CTS signals. One of them, UART1, supports full modem control.

Three of the UARTs, (UART0, UART1 and UART3), have pins identified on the phyCORE connectors. For all of the signal multiplexing options, see the phyCORE-AM335x datasheet. The following table shows the location of the UART signals which are identified by name on the phyCORE connectors.

Pin#	Signal	I/O	SL	Description
X3.A32	X_UART0_TXD	OUT	3.3V	UART 0 transmit data
X3.A33	X_UART0_RXD	IN	3.3V	UART 0 receive data
X3.B10	X_UART1_TXD	OUT	3.3V	UART 1 transmit data
X3.B11	X_UART1_RXD	IN	3.3V	UART 1 receive data
X3.B8	X_UART1_CTS	IN	3.3V	UART 1 clear to send
X3.B9	X_UART1_RTS	OUT	3.3V	UART 1 request to send
X3.B60	X_UART2_TX	OUT	3.3V	UART 2 transmit data
X3.A60	X_UART2_RX	IN	3.3V	UART 2 receive data
X1.A9	X_UART3_TX	OUT	3.3V	UART 3 transmit data
X1.A8	X_UART3_RX	IN	3.3V	UART 3 receive data

Table 26: Locations of the UART Signals

USB-OTG interfaces

The phyCORE-AM335x provides two high speed USB-OTG interfaces. These use the AM335x embedded HS USB-OTG PHYs. The AM335x USB signals all route directly to the phyCORE connectors. The signal assignments on the phyCORE-Connector is shown in

Pin #	Signal	IO	SL	Description
X3.A48	X_USB0_DP	IO	3.3V	USB0 data plus
X3.A47	X_USB0_DM	IO	3.3V	USB0 data minus
X3.B43	X_USB0_ID	IN	1.8V	USB0 connector identification signal
X3.B41	X_USB0_VBUS	IN	5V	USB0 VBUS detection input
X3.B42	X_USB0_DRVVBUS	OUT	3.3V	USB0 VBUS control output
X3.B44	X_USB0_CE	OUT	3.3V	USB0 charger enable
X3.B18	X_USB1_DP	IO	3.3V	USB1 data plus
X3.B19	X_USB1_DM	IO	3.3V	USB1 data minus
X3.B23	X_USB1_ID	IN	1.8V	USB1 connector identification signal
X3.B22	X_USB1_VBUS	IN	5V	USB1 VBUS detection input
X3.B21	X_USB1_DRVVBUS	OUT	3.3V	USB1 VBUS control output
X3.B24	X_USB1_CE	OUT	3.3V	USB1 charger enable

Table 27: Location of the USB-OTG signals on the phyCORE connectors

Ethernet1 with PHY (U3)

Connection of the phyCORE-AM335x to the world wide web or a local area network (LAN) is possible using the on module FEC (Fast Ethernet Controller) SMSC LAN8710AI (U3) of the phyCORE-AM335x. The FEC operates with a data transmission speed of 10 or 100 Mbit/s.
The phyCORE-AM335x has been designed for use in 10Base-T and 100Base-T networks with an ethernet PHY included on the SOM.

Pin #	Signal	I/O	SL	Description
X3.A10	X_ETH_TX+	DIFF100	3.3 V	Ethernet transmit positive output
X3.A9	X_ETH_TX-	DIFF100	3.3 V	Ethernet transmit negative output
X3.A13	X_ ETH_LED2	OUT	3.3 V	Ethernet Speed Indicator (open drain)
X3.A7	X_ETH_RX+	DIFF100	3.3 V	Ethernet receive positive input
X3.A6	X_ETH_RX-	DIFF100	3.3 V	Ethernet receive negative input
X3.A14	X_ETH_LED1	OUT	3.3 V	Ethernet link indicator (open drain)

Table 28: Ethernet1 Signals

The embedded MAC of the Ethernet controller supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet controller provides wake on LAN and other power management modes. The interrupt signal of the LAN8710AI is connected to the interrupt 1 (INTR1) signal which routes to the phyCORE connector X1.

In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module. Connection to an external Ethernet magnetics should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

The two LED control signals for the Ethernet1 interface are also configuration inputs for the Ethernet PHY on the SOM. To make sure the PHY powers up into the planned configuration, with its internal voltage regulator and interrupt signal enabled, the X_ETH_LED2/_INTSELn signal should be on the GND side of its LED, and the X_ETH_LED1/_REGOFF signal should be on the power side of its LED. See the phyCORE-AM335x Carrier Board schematics for a reference design for this circuit. The AM335x Ethernet1 signals also route to the phyCORE connectors. This provides customers the option to not populate the Ethernet PHY on the SOM and to use these signals for other purposes.

Ethernet 2

The AM335x Ethernet2 port signals route directly off of the SOM. The PHYTEC Carrier Board connects these to a RGMII PHY. These signals can alternately connect to any industry-standard Ethernet PHY or be used for other purposes. The AM335x processor supports MII, RMII and RGMII modes on this interface. It does not support GMII mode.

It is strongly recommended to place the Ethernet PHY on the Carrier Board so that the signals between the phyCORE connectors and the Ethernet PHY are 4 inches or shorter.

Pin #	Signal	I/O	SL	Description
X1.B43	X_RGMII2_TCTL	OUT	3.3 V	RGMII transmit control
X1.A42	X_RGMII2_TCLK	OUT	3.3 V	RGMII transmit clock
X1.A37	X_RGMII2_TD3	OUT	3.3 V	RGMII transmit data bit 3
X1.A39	X_RGMII2_TD2	OUT	3.3 V	RGMII transmit data bit 2
X1.B42	X_RGMII2_TD1	OUT	3.3 V	RGMII transmit data bit 1
X1.A40	X_RGMII2_TD0	OUT	3.3 V	RGMII transmit data bit 0
X1.A36	X_RGMII2_RCTL	IN	3.3 V	RGMII receive control
X1.A43	X_RGMII2_RCLK	IN	3.3 V	RGMII receive clock
X1.B40	X_RGMII2_RD3	IN	3.3 V	RGMII receive data bit 3
X1.A45	X_RGMII2_RD2	IN	3.3 V	RGMII receive data bit 2
X1.A46	X_RGMII2_RD1	IN	3.3 V	RGMII receive data bit 1
X1.A48	X_RGMII2_RD0	IN	3.3 V	RGMII receive data bit 0

Table 29: Location of the Ethernet 2 signals

Profibus

The Profibus interface is available on the AM335x PRU UART0. This UART is in addition to the 6 high-speed UART mentioned above, which are part of the AM335x MPU. The PRU UART0 signals are available on either the UART1 or the SPI1 pins as signal multiplexing options. These signals are all available on the phyCORE connectors.

I²C Interface

The Inter-Integrated Circuit (I²C) interface is a two-wire, bi-directional serial bus that provides a simple and efficient method for data exchange among devices. The AM335x contains three I²C interfaces. These are available on the phyCORE connector. The I²C0 interface connects also to several devices on the SOM: the I²C EEPROM, the optional external RTC, and to the PMIC TPS65910A3. So do not use the I²C0 interface if another one is available to avoid bandwidth issues and potential address collisions. The I²C EEPROM is used to store the SOM's MAC address. The MAC address of the phyCORE-AM335x is also located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

I²C0 write/read addresses 0x2D/0x2E, 0x12,0x13, 0xD0/0xD1, and 0xA8/0xA9 are reserved for devices on the SOM. The 0xA8/0xA9 address is the default address for the I2C EEPROM. In case of an address conflict, its address can be modified with jumpers. This is described in section *I²C EEPROM (U6)* The I²C interfaces are available on many signals, depending on how the AM335x pin multiplexing is configured. See the Texas Instruments AM335x Datasheet for all of the pin multiplexing options. The following Table 14 lists the I²C signals named on the phyCORE-Connector:

Pin #	Signal	I/O	SL	Description
X3.A19	X_I2C0_SCL	OUT	3.3 V	I2C0 clock (open drain with pull-up resistor on the SOM)
X3.A20	X_I2C0_SDA	IO	3.3 V	I2C0 data (open drain with pull-up resistor on the SOM)

Table 30: I²C Interface Signal Locations

SPI Interfaces

The Serial Peripheral Interface (SPI) interface is a four-wire, bi-directional serial bus that provides a simple and efficient method for data exchange among devices. The AM335x contains two SPI modules. The interface signals of the first module (SPI0) are identified on the phyCORE-Connector. If there is a SPI Flash installed on the SOM, it connects to SPI1_CS0. The signals for the SPI1 interface are also available on the phyCORE connector, multiplexed with other signals. See the Texas Instruments AM335x datasheet for all pin-multiplexing options. The SPI module is Master/Slave configurable.The following Table 15 lists the SPI signals identified on the phyCORE-Connector:

Pin #	Signal	I/O	SL	Description
X3.A17	X_SPI0_CS0	OUT	3.3 V	SPI0 chip select 0 (used by SPI Flash, if installed)
X3.A18	X_MMC0_SDCD 9SPI0_CS1)	OUT	3.3 V	SPI0 chip select 1
X3.A31	X_SPI0_D1 (MOSI)	OUT	3.3 V	SPI0 master output / slave input
X3.A33	X_SPI0_D0 (MISO)	IN	3.3 V	SPI0 master input / slave output
X3.A15	X_SPI0_CLK	OUT	3.3 V	SPI0 clock

Table 31: SPI Interface Signal Locations

Controller Area Network (CAN) Interfaces

The two AM335x CAN ports support CAN Version 2 parts A and B. These ports are each available on three different pin multiplexing options.

Multichannel Audio Serial Ports (McASP)

The multichannel audio serial port (McASP) interfaces of the phyCORE-AM335x are general audio serial ports optimized for the requirements of various audio applications. The MCASP interfaces support many audio formats including SPDIF, IEC60958-1, AES-3, TDM, I2S and similar formats. The McASP signals which are used on the Phytec Carrier Board are listed in the following Table 16. See Texas Instrument's AM335x Data Sheet for all of the pin-multiplexing options for the two McASP interfaces.

Pin #	Signal	I/O	SL	Description
X3.A22	X_McASP0_AXR0	IO	3.3 V	serial data
X3.A29	X_McASP0_FSX	IO	3.3 V	frame synchronization transmit
X3.B27	X_McASP0_AHCLK X	IO	3.3 V	high frequency clock
X3.A28	X_McASP0_AXR1	IO	3.3 V	serial data
X3.B16	X_McASP0_ACLKX	IO	3.3 V	transmit bit clock

Table 32: McASP Signal Locations

General Purpose I/Os

The phyCORE-AM335x provides 3 named GPIOs. Beside these 3 dedicated GPIOs, most of the AM335x signals which are connected directly to the module connector can also be configured to act as GPIOs, due to the multiplexing functionality of the most controller pins. The GPIO pins can be used as data input with an optional and configurable debounce cell or data output. Furthermore the pins support an interrupt generation in active mode and wake-up request generation in idle mode upon the detection of external events. With the pad control feature of the AM335x, you can also configure the GPIO to have optional a pull-up/pull-down or to enable the open drain feature. Table 17 shows the location of the dedicated GPIO pins on the phyCORE connector, as well as the corresponding ports of the AM335x.

Pin #	Signal	I/O	SL	Description
X1.B20	X_GPIO_3_7	IO	3.3 V	GPIO_3_7
X1.B18	X_GPIO_3_8	IO	3.3 V	GPIO_3_8
X3.A23	X_GPIO_3_17	IO	3.3 V	GPIO_3_17
X1.B5	X_GPIO_3_18	IO	3.3 V	GPIO_3_18
X3.B15	X_GPIO_3_19	IO	3.3 V	GPIO_3_19

Table 33: Locations of Dedicated GPIO Pins

As can be seen in the Table 17 above the voltage level is 3.3 V. To avoid mismatch of the different voltage levels external devices connected to these pins should be supplied by a 3.3 V supply which powers up and down with the IO reference voltage (VAUX2_3P3V) which is available at the phyCORE connector at pin X3.B6.

JTAG / Debug Interface (X2)

The phyCORE-AM335x is equipped with a JTAG interface for running boundary scans, downloading program code into the external flash, accessing internal controller RAM or for debugging programs which are executing.The JTAG interface connects to a 2.54 mm pitch pin header at X2 on the edge of the module PCB and also to the Samtec phyCORE connector X1. Figure 7 shows the position of the debug interface connector X2 on the phyCORE-AM335x module.
The JTAG connector X2 is installed on the phyCORE-AM335x as an ordering option.

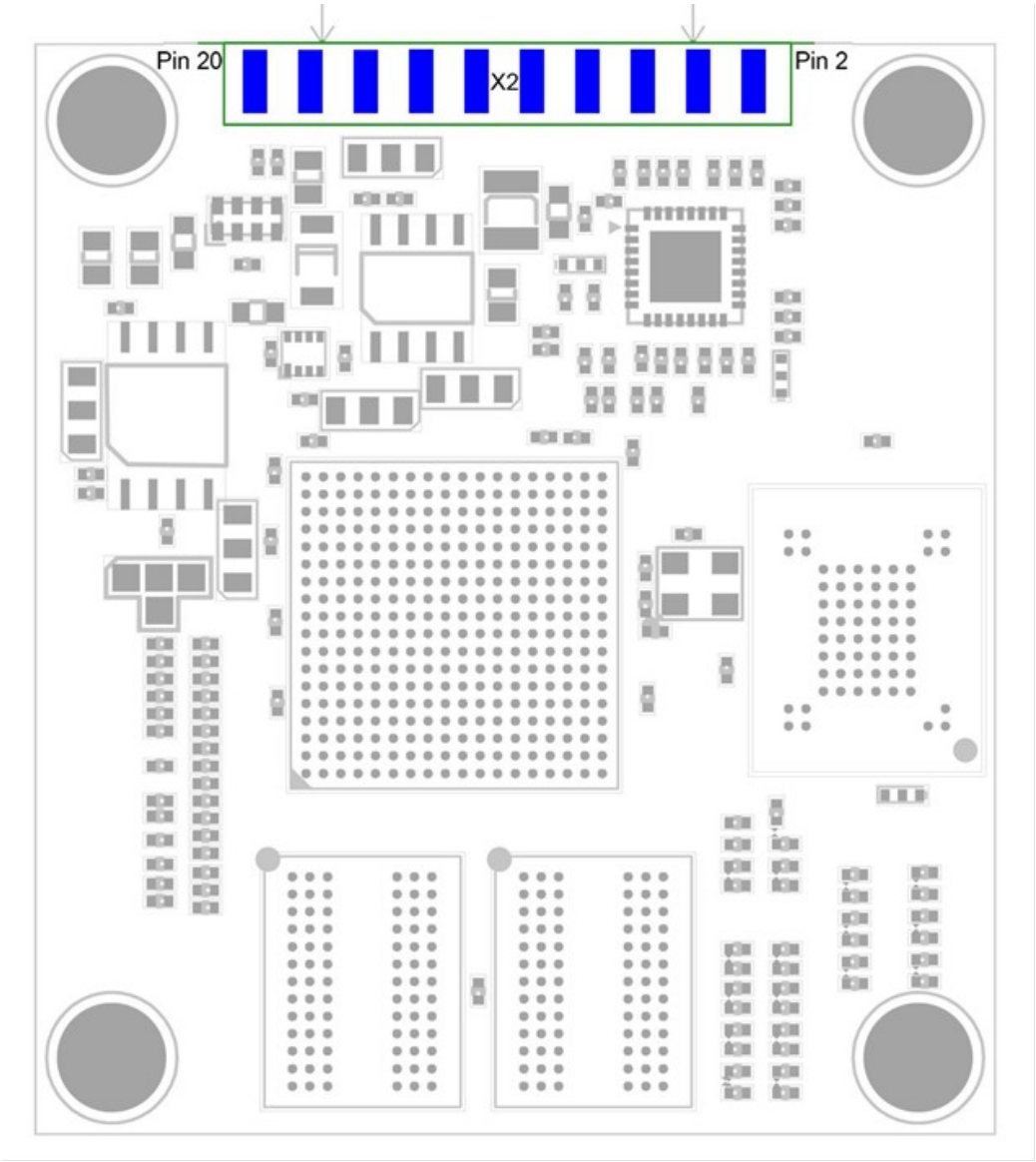


Figure 10: JTAG Interface at X2 (Top View)

Pin 1 of the JTAG connector X2 is on the bottom side of the module. Pin 2 of the JTAG connector is on the top of the module.

The following Table 18 provides on the JTAG signal pin assignment on connector X2.

Signal	**Pin Row***		**Signal**
	A	B	
VMMC_3P3V	2	1	TREF (3.3 V via 100 Ohm)
GND	4	3	X_JTAG_nTRST
GND	6	5	X_JTAG_TDI
GND	8	7	X_JTAG_TMS
GND	10	9	X_JTAG_TCK
GND	12	11	X_JTAG_RTCK
GND	14	13	X_JTAG_TDO
GND	16	15	X_nRESET_WARM

GND	18	17	no-connect
GND	20	19	no-connect

Table 34: JTAG Connector X2 Signal Assignments

*Note: Row A is on the top side of the module and Row B is on the bottom side of the module

The following Table 19 provides on the JTAG signal pin assignment on the module connector X1.

Pin #	Signal	I/O	SL	Description
X1.B10	X_TDO	OUT	3.3 V	JTAG test data output
X1.B12	X_TMS	OUT	3.3 V	JTAG test mode select
X1.B8	X_TCK	OUT	3.3 V	JTAG test clock input
X1.B11	X_nTRST	IN	3.3 V	JTAG test reset
X1.B7	X_TDI	IN	3.3 V	JTAG test data input

Table 35: Location of JTAG Pins on phyCORE Connector X1

Display Interface

The phyCORE-AM335x provides a configurable parallel display interface with up to 24 data bits and touch-screen control.

Parallel Display Interface

The AM335x's 24-bit parallel display interface is directly connected from the AM335x to the module connector.The location of the applicable interface signals can be found in Table 20 below. Signal X_ECAP0_IN_PWM0_OUT can be used as PWM output to control the display brightness.

Pin #	Signal	I/O	SL	Description
X3.B26	X_ECAP0_IN_PWM0_OUT	OUT	3.3 V	PWM output, can be used for display brightness control
X1.B27	X_LCD_DATA23	OUT	3.3 V	LCD data bit 22
X3.B28	X_LCD_DATA22	OUT	3.3 V	LCD data bit 22
X3.B26	X_LCD_DATA21	OUT	3.3 V	LCD data bit 21
X3.B30	X_LCD_DATA20	OUT	3.3 V	LCD data bit 20
X3.B31	X_LCD_DATA19	OUT	3.3 V	LCD data bit 19
X3.B32	X_LCD_DATA18	OUT	3.3 V	LCD data bit 18
X3.B38	X_LCD_DATA17	OUT	3.3 V	LCD data bit 17
X3.B36	LCD data bit 17	OUT	3.3 V	LCD data bit 15
X3.A54	X_LCD_DATA15	OUT	3.3 V	LCD data bit 14
X3.A53	X_LCD_DATA14	OU	3.3	LCD data bit 13

		T	V	
X3.A44	X_LCD_DATA13	OUT	3.3 V	LCD data bit 12
X3.B49	X_LCD_DATA11	OUT	3.3 V	LCD data bit 11
X3.A59	X_LCD_DATA10	OUT	3.3 V	LCD data bit 10
X3.A58	X_LCD_DATA9	OUT	3.3 V	LCD data bit 9
X3.A52	X_LCD_DATA8	OUT	3.3 V	LCD data bit 8
X3.A57	X3.A57	OUT	3.3 V	LCD data bit 7
X3.A55	X_LCD_DATA6	OUT	3.3 V	LCD data bit 6
X3.A40	X_LCD_DATA5	OUT	3.3 V	LCD data bit 5
X3.A39	X_LCD_DATA4	OUT	3.3 V	LCD data bit 4
X3.A37	X_LCD_DATA3	OUT	3.3 V	LCD data bit 3
X3.A38	X_LCD_DATA2	OUT	3.3 V	LCD data bit 2
X3.A35	X_LCD_DATA1	OUT	3.3 V	LCD data bit 1
X3.A34	X_LCD_DATA0	OUT	3.3 V	LCD data bit 0
X3.A45	X_LCD_HSYNC	OUT	3.3 V	LCD horizontal synchronization

Table 36: Parallel Display Interface Signal Locations

Touch Screen Controller

The AM335x processor includes an integrated touch controller. This can connect to a resistive touch panel such as is typically integrated in an LCD panel.
The AM335x's eight analog input signals, AIN[7:0], are routed to the primary phyCORE connector, X3. Some or all of these can be connected to a resistive touch panel on the Carrier Board. The Phytec Carrier Board connects four of these signals to a touch controller for a LCD. These signals are mapped as follows:
AIN0 = TOUCH_X+
AIN1 = TOUCH_X-
AIN2 = TOUCH_Y+
AIN3 = TOUCH_Y-
Care should be taken in carrier board layout to isolate these analog signals from noise such as from power supplies or digital signals.

Technical Specifications

The physical dimensions of the phyCORE-AM335x are represented in Figure 8. The module's profile is max. **5.0 mm** thick, with a maximum component height of **1.5 mm** on the bottom (connector) side of the PCB and approximately **2.0 mm** on the top (microcontroller) side. The board itself is approximately **1.5 mm** thick.

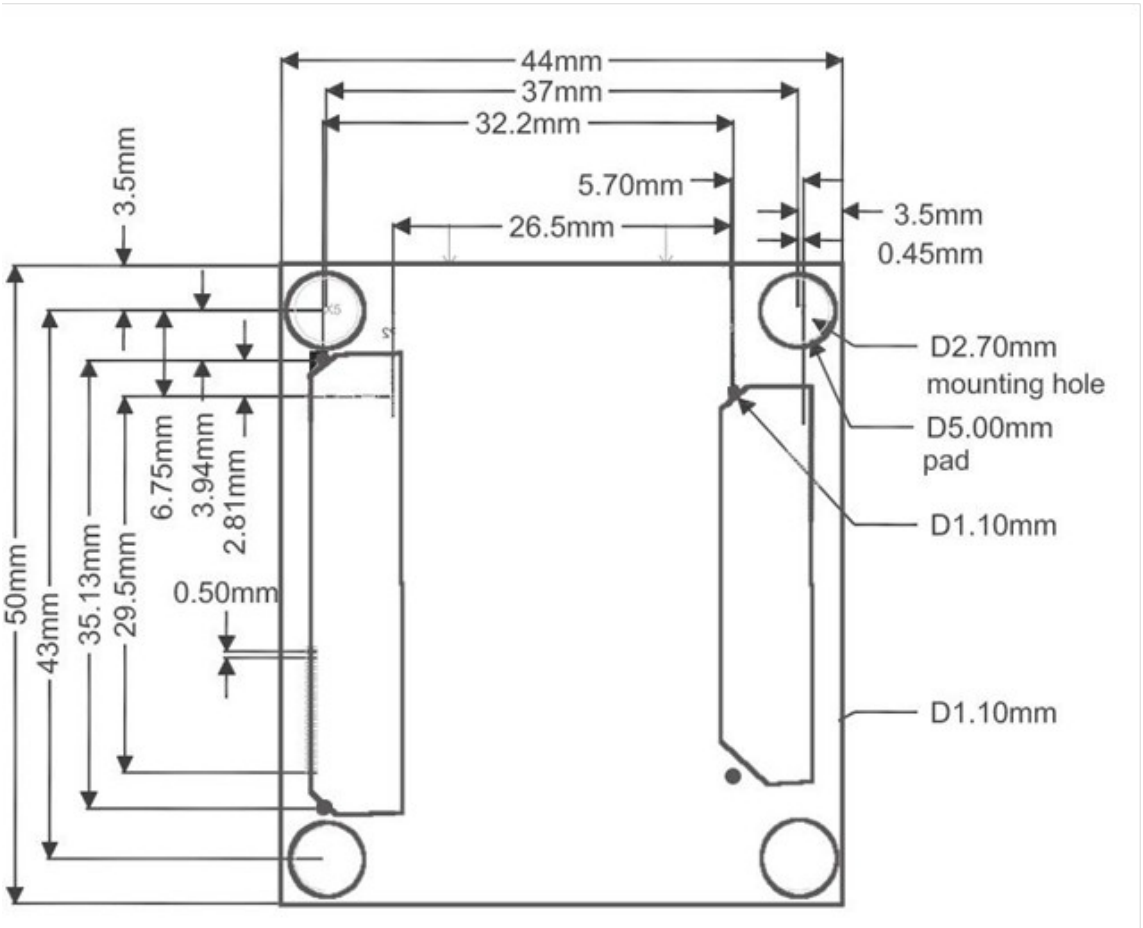


Figure 11: Physical Dimensions

Additional specifications

Dimensions:	44 mm x 50 mm
Weight:	t.b.d.
Storage temperature:	-40 °C to +125 °C
Operating temperature:	0 °C to +70 °C (commercial) -40 °C to +85 °C (industrial)
Humidity:	95 % r.F. not condensed
Operating voltage:	VCC 5.0 V
Power consumption:	VCC 5.0 V / 0.4 A / 2 Watts typical Max. 3 Watts Conditions: **VCC = 5.0 V, VBAT = 3.0 V**,512 MB DDR3-SDRAM, 512 MB NAND Flash, Ethernet, 600 MHz CPU frequency, 20 °C

Table 37: Specification of the SOM

These specifications describe the standard configuration of the phyCORE-AM335x as of the printing of this manual.

Connectors on the phyCORE:

X1 Manufacturer	Samtec
Number of pins per contact Rows	100 (2 Rows of 50 pins each)
Samtec part number (lead free)	BSH-050-01-L-D-A (receptacle)
X3 Manufacturer	Samtec
Number of pins per contact Rows	120 (2 Rows of 60 pins each)
Samtec part number (lead free)	BSH-060-01-L-D-A (receptacle)

Different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-AM335x. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (1.5 mm) on the bottom side of the phyCORE must be subtracted.
Please refer to the corresponding datasheets and mechanical specifications provided by Samtec.

Handling the phyCORE-AM335x

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution

If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

Component Placement Diagram

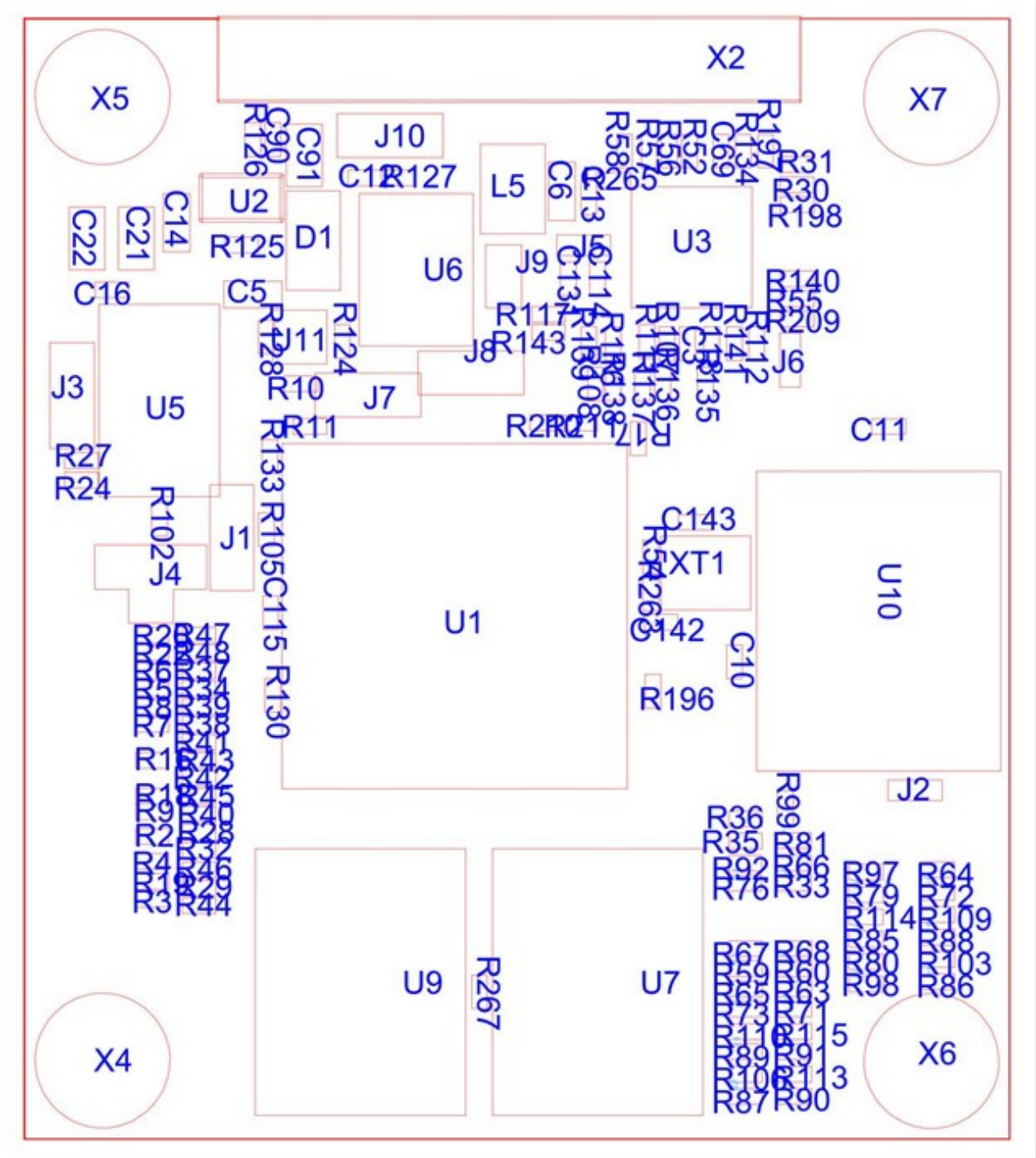


Figure 12: phyCORE-AM335x Component Placement (Top View)

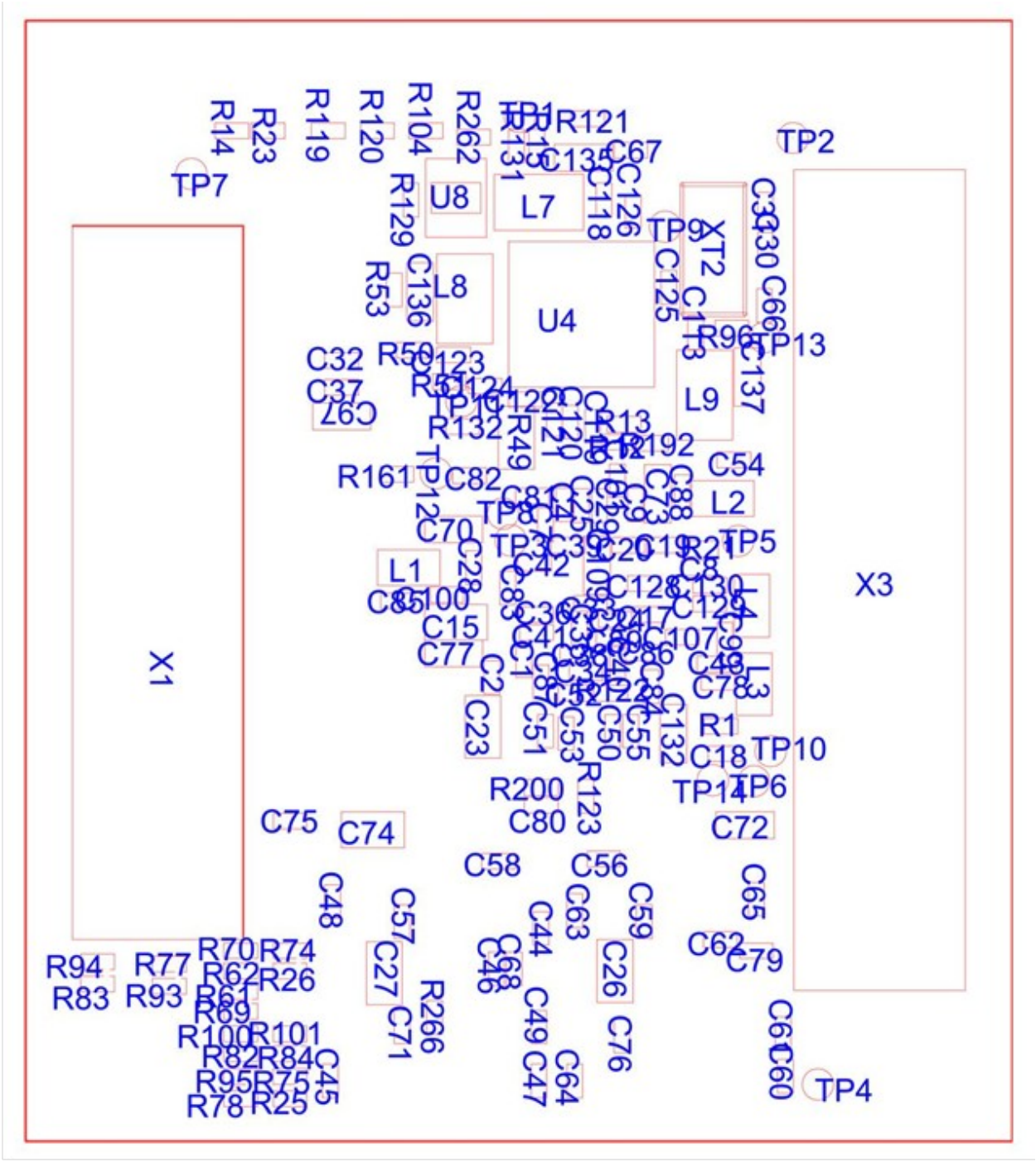


Figure 13: phyCORE-AM335x Component Placement (Bottom View)

Open Board Dimension

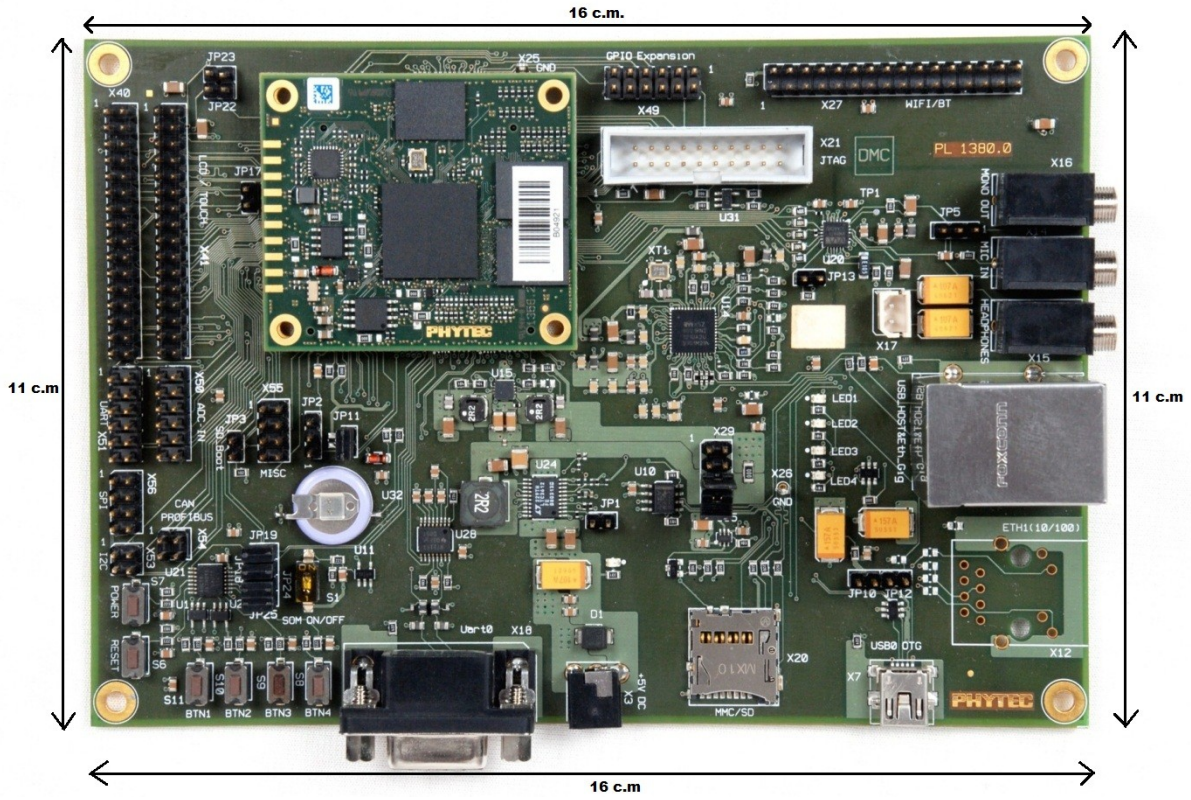


Figure 14: Physical Dimensions of Open Board

PHYTEC

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.....We are looking forward to hearing from you!.....