PHYTEC

Cosmic Board for phyCORE-AM335x System on Module and Carrier Board

Hardware Manual

A product of a **PHYTEC** Technology Holding Company

	INDIA	EUROPE	NORTH AMERICA
Address:	PHYTEC Embedded Pvt. Ltd. #16/9C,3rd Floor,3rd Main,Opp.Police Station Koramangala,8thblock , Bangalore -560095 India	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+91-80-40867046 sales@phytec.in	+49 (800) 0749832 sales@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+91-80-40867047 support@phytec.in	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	-	+49 (6131) 9221-33	1 (206) 780-9135
Website:	http://www.phytec.in	http://www.phytec.eu http://www.phytec.de	http://www.phytec.com

Table of Contents

List of Tables

List of Figures

Conventions, Abbreviations, and Acronyms

Conventions
The conventions used in this manual are as follows:
- Signals that are preceded by a "/" character are designated as active low signals. Their active state is when they are driven low, or are driving low; for example : /RESET.
- Tables show the default setting or jumper position in **bold, teal** text.
- Text in blue indicates a hyperlink, either internal or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connectors on the underside of the Cosmic Board System on Module.

Abbreviations and Acronyms
Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Table i- 1. Abbreviations and Acronyms Used in This Manual

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the PCM-953/Cosmic Board Carrier Board
DFF	D flip-flop
EMB	External memory bus
EMI	Electromagnetic Interference
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
IRAM	Internal RAM; the internal static RAM on the TI AM335x processor
J	Solder jumper; these types of jumpers require solder equipment to remove and place
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools
PCB	Printed circuit board
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards or custom adapters
PEB	PHYTEC Extension Board
PMIC	Power Management Integrated Circuit
PoE	Power over Ethernet
PoP	Package on Package

PoR	Power-on reset
RTC	Real-time clock
SMT	Surface mount technology

Table i-1. Abbreviations and Acronyms Used in This Manual

Abbreviation	Definition
SOM	System on Module; used in reference to the PCM-051/Cosmic Board System on Module
Sx	User button Sx (S1, S2, etc.) used in reference to the available user buttons, or DIP switches on the Carrier Board
TRM	Technical Reference Manual
VBAT	SOM battery supply input

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of a signal.

Table i- 2. Types of Signals

Type of Signal	Description	Abbreviation
Power	Supply voltage	PWR
Ref-Voltage	Reference voltage	REF
USB-Power	USB voltage	USB
Input	Digital input	IN
Output	Digital output	OUT
Input with pull-up	Input with pull-up (jumper or open-collector output)	IPU
Input/output	Bidirectional input/output	IO
5V Input with pull-down	5V tolerant input with pull-down	5V_PD
LVDS	Differential line pairs 100 Ohm LVDS level	LVDS
Differential 90 Ohm	Differential line pairs 90 Ohm	DIFF90
Differential 100 Ohm	Differential line pairs 100 Ohm	DIFF100
Analog	Analog input or output	Analog

Preface

This Cosmic Board Hardware Manual describes the System on Module's design and

functions. Precise specifications for the TI AM335x processor can be found in the processor datasheet and/or user's manual .

In this hardware manual and in the schematics, active low signals are denoted by a "/" preceding the signal name, for example: /RD. A "0" represents a logic-zero or low-level signal, while a "1" represents a logic one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC Cosmic Board

PHYTEC System on Modules (SOMs) are designed for installation in electrical appliances or, combined with the PHYTEC Carrier Board, can be used as dedicated Evaluation Boards (for use as a test and prototype platform for hardware/software development) in laboratory environments.

> **CAUTION:**
> PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

> Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The Cosmic Board is one of a series of PHYTEC System on Modules that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8/16 and 32-bit controllers in two ways:

1. As the basis for Rapid Development Kits which serve as a reference and Evaluation platform.
2. As insert-ready, fully functional phyCORE OEM modules, which can be Embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the

phyCORE module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware further reduce development time and expenses. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. For more information go to:
http://www.phytec.in/services/hardware.html

Product Change Management

In addition to our HW and SW offerings, the buyer will receive a free obsolescence maintenance service for the HW provided when purchasing a PHYTEC SOM.

Our Product Change Management Team of developers is continuously processing all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products. Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are evaluated in order to take the right measures in purchasing or within our HW/SW design.

Our general philosophy here is: We never discontinue a product as long as there is demand for it.

Therefore a set of methods has been established to fulfill our philosophy:

Avoidance strategies
- Avoid changes by evaluating longevity of a part during design-in phase.
- Ensure availability of equivalent second source parts.
- Maintain close contact with part vendors for awareness of roadmap strategies.

Change management in case of functional changes
- Avoid impacts on Product functionality by choosing equivalent replacement parts.
- Avoid impacts on Product functionality by compensating changes through HW redesign or backward compatibility

SW maintenance
- Provide early change notifications concerning functional relevant changes of our Products.

Change management in rare event of an obsolete and non replaceable part
- Ensure long term availability by stocking parts through last time buy management, according to product forecasts.
- Offer long term frame contract to customers.

We refrain from providing detailed, part-specific information within this manual, which is subject to changes, due to ongoing part maintenance for our products.

1 Introduction

X8 RS-232 Console
X6 USB OTG + Board Power
X16 HDMI
X3 USB Host & Ethernet
PCB Edge
S1
S2
S3
S4
S5
User Buttons
Reset Button
JP5 Boot Select
PCL-051/phyCORE- AM335x System on Module
JP1 Power Select
X19 & X20 Expansion Connetors
D5
D4
D10
D11
X2 +5VDC
User LEDs
X18 uSD Card
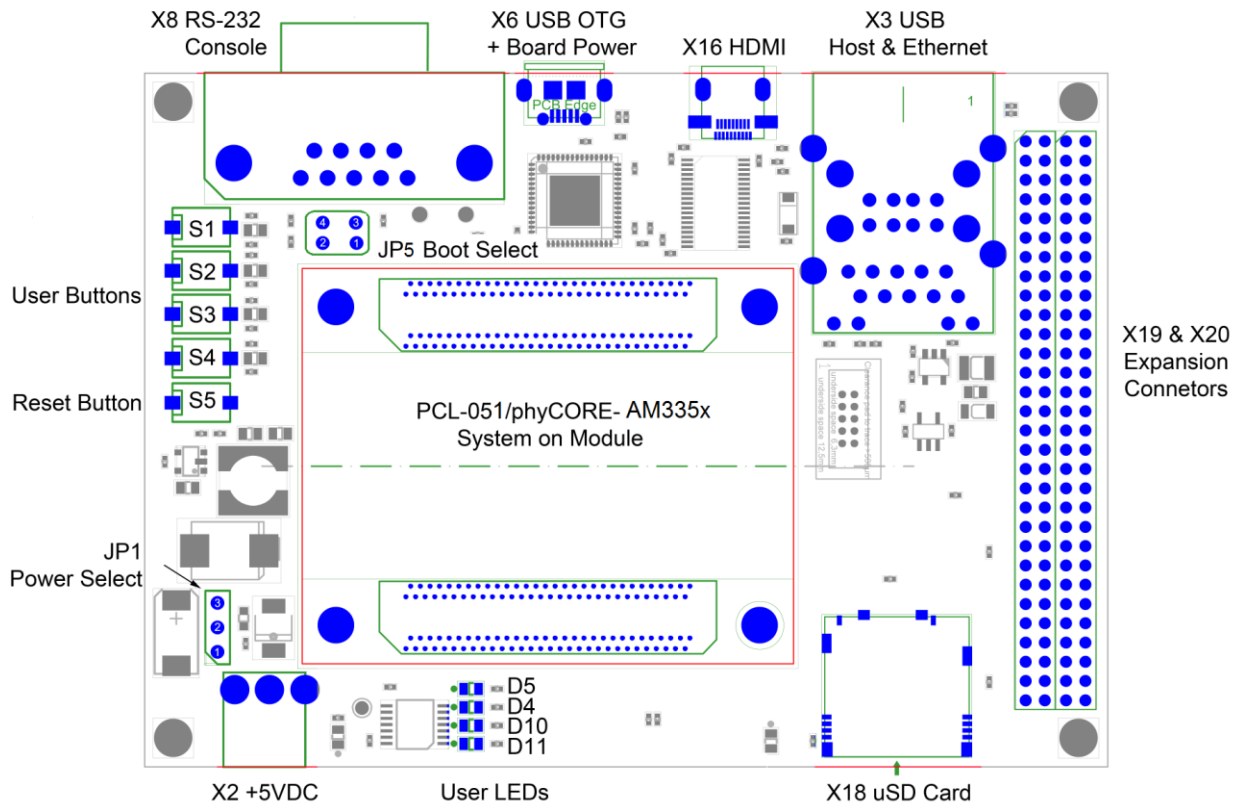
Figure 1- 1. Cosmic Board

The Cosmic Board for phyCORE-AM335x is a low-cost, feature-rich software development platform supporting the TI AM335x processor families. At the core of the Cosmic board is the PCL-051/phyCORE-AM335x System On Module (SOM) in a direct solder form factor, containing the AM335x processor, SDRAM, NAND Flash, power regulation, supervision, transceivers, and other core functions required to support the Cosmic AM335x Board. Surrounding the SOM is the POB-002/Cosmic Carrier Board, adding power input, buttons, connectors, signal breakout, and HDMI connectivity amongst other things.

The PCL-051 System On Module is a connector-less, BGA style variant of the PCM-051/phyCORE-AM335x SOM. Unlike traditional PHYTEC SOM products that support high density connectors, the PCL-051 SOM is directly soldered down to its Carrier Board using PHYTEC's Direct Solder Connect technology. This solution offers an ultra-low cost Single Board Computer for the AM335x processor, while maintaining most of the advantages of the SOM concept.

Adding the phyCORE-AM335x SOM into your own design is as simple as ordering the connectored version (PCM-051) and making use of our Cosmic Carrier Board (POB-002), or RDK Carrier Board (PCM-953) reference schematics. A summary of the Cosmic Board features, along with a block diagram are presented below.

1.1 Cosmic Board Features

- phyCORE-AM335x System On Module
- Board power over:
    - USB OTG Connector
    - Wall Adapter Input
- High Speed USB Host Connector (standard A)
- High Speed USB OTG Connector (micro AB)
- 10/100 Ethernet RJ-45 Jack
- Micro SD Card Slot
- Micro HDMI connector supporting 640x480 @ 24bpp
- RS-232 Console Connectivity via DB-9
- Boot Selection Jumpers (NAND or SD Card or NOR)
- 4x User Buttons
- 4x User LEDs
- 120-pin, 2mm header socket for easy access to AM335x processor signals

1.2 Block Diagram

Figure 1- 2. Cosmic Board Block Diagram

2 PCL-051/phyCORE-AM335x System on Module

This chapter gives a brief introduction to the PCL-051/phyCORE-AM335x System on Module (SOM), highlighting its benefits and features. For more detailed information, please refer to the Hardware Manual for the modular, connectored version of the SOM (PCM-051) by clicking here.

The phyCORE-AM335x belongs to PHYTEC's phyCORE System on Module (SOM) family. The phyCORE SOMs represent the continuous development of PHYTEC SOM technology. Like its mini-, micro-, and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.
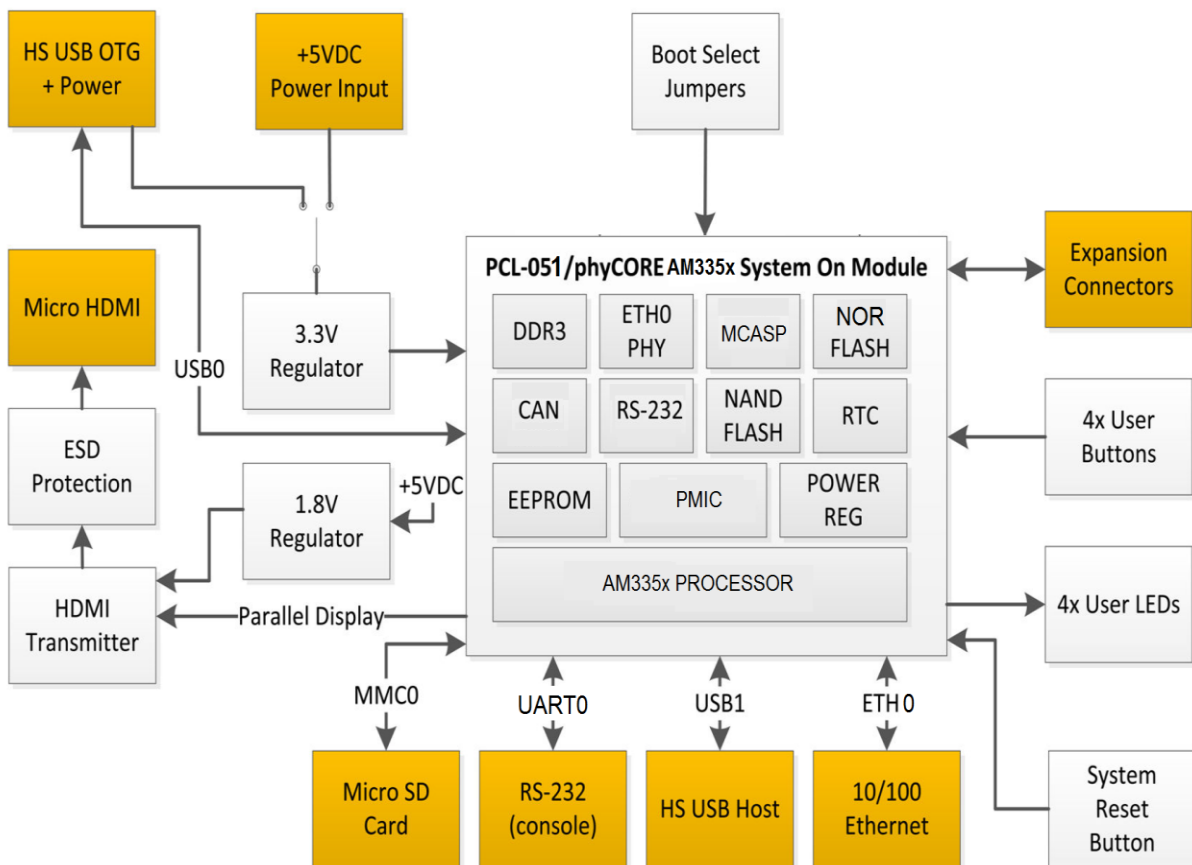
As independent research indicates that approximately 70% of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments, the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20% of all connector pins on the phyCORE boards to ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The PCM-051, connectored version of the phyCORE-AM335x is a sub-miniature (41 x 51 mm) insert-ready SOM populated with AM335x processor. Its universal design enables its insertion into a wide range of embedded applications. All processor signals and ports extend from the processor to high-density pitch (0.5 mm) connectors aligning two sides of the board. This allows the SOM to be plugged like a "big chip" into a target application.

The PCL-051, connectorless version of the phyCORE-AM335x populating the Cosmic Board is identical to the connectored version, with the exception of the connection interface. Instead of two high density connectors aligning the edges of the board, the PCL-051 solders directly down to its Carrier Board with a BGA style footprint.

Precise specifications for the processor populating the board can be found in the applicable processor user's manual and datasheet. The descriptions in this manual are based on the AM335x processor. No description of compatible processor derivative functions is included, as such functions are not relevant for the basic functioning of the Cosmic Board.

2.1 phyCORE-AM335x Features

- Insert-ready, sub-miniature (41 mm x 51 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the TI AM335x (Cortex-A8) processor
- Max. 720 MHz core clock frequency
- Boot from NAND Flash or SPI Flash
- Controller signals and ports extend to two BGA-style connection interfaces aligning two sides of the board, enabling it to be soldered directly into the target application
- Single supply voltage of 3.3 V (max.1 A)
- All controller required supplies generated on board
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- 512 MB (up to 1 GB) on-board NAND Flash
- 512 MB DDR3 SDRAM
- 4 kB (up to 32 kB) I2C EEPROM
- 8 MB SPI Flash
- One RS-232 two-signal (Tx/Rx) serial interfaces, or one RS-232 interface with hardware flow control, configured through software
- Six UARTs
- Dual USB OTG 2.0 High-Speed Controller with PHY
- Two 10/100/1000 MBit Ethernet interfaces with internal L2-Switch and IEEE1588 PTP for Realtime Ethernet (available as RMII TTL signals or 10/100 differential pairs)
- Three I2C interfaces with SMBUS support
- Two Serial Peripheral Interfaces (SPI)
- Two CAN interfaces with transceivers
- Display interface with 24 data bits
- Multichannel Audio Serial Ports
- One 8-channel, analog to digital (ADC) inputs
- JTAG
- 4-bit Secure Digital Host interface (SD/MMC)
- Real-Time Clock
- -40 to 85 degree Celcius operating temperature range

3 Power

Power is supplied to the system using two methods:
        1. USB power via connector X6
        2. Wall power via connector X2

USB power provides an easy, single-cable solution for both power and console connectivity. System functionality is limited when powering the board off of USB. Most features of the board will function under USB power, with the exception of USB host and any add-on boards connected via the Expansion Connectors. Select the power option by configuring jumper JP1 using Table 3-1 below.

3.1 Jumper Settings (JP1)

Table 3- 1. Jumper Settings (JP1)

Jumper Position	Description
1+2	Wall Power
2+3	USB Power

See Figure 1-1 for the location of jumper JP1. Pin 1 is marked on the PCB with a clipped corner on the component outline silk screen.

3.2 USB Power (X6)

USB power can be used if the USB host interface is not required, nor any add-on boards connected to the Expansion Connectors (X19, X20) are required.

Use a standard USB-A to micro-AB, or micro-B connected to a PC to power the board and provide console access. A wall-outlet charger can be used to power the board but will eliminate the use of serial over USB.

Configure the board for USB power by setting JP1 to 2+3. See Figure 1-1 for the location of jumper JP1.

3.3 Wall Power (X2)

Wall power should be used when USB host, or expansion connector add-on boards are used. Both scenarios draw additional power not available through the USB OTG connector at X6.

A suitable +5VDC +- 5% / 1A or greater wall power adapter should be used with a center

positive contact. An appropriate power supply can be ordered with the kit at the time you place your order. Configure the board for wall power by setting JP1 to 1+2. See Figure 1-1 for the location of jumper JP1.

CAUTION:
Do not use a laboratory adapter to supply power to the Carrier Board! Power spikes during power-on could destroy the phyCORE module mounted on the Carrier Board. Do not change jumper settings while the Carrier Board is supplied with power.

---

4 Ethernet (X3)

The 10/100 ETH0 interface, derived from the TI AM335x processor RMII1 signals, is accessible at an RJ-45 connector at X3 (USB Dual Standard A and Ethernet).

LEDs are integrated on the connector for indication of LINK (green) and SPEED (yellow).

The Ethernet PHY on the SOM supports the HP Auto-MDIX function, eliminating the need for considerations of a direct connect LAN cable or cross-over patch cable. The transceivers detect the TX and RX signals of the connected devices and automatically configure their RX and TX pins accordingly.

5 RS-232 Console (X8)

The DB9 connector X8 provides connectivity to the Cosmic (UART) signals at RS-232 level. This interface does not include the Cosmic's UART0_RTS and UART0_CTS signals for flow control. This connection is provided primarily for console access, but could be reconfigured for other purposes if needed.

A standard straight-through serial cable connected to a PC is required to access this console port. This port has the benefit of providing access to U-Boot and to early Linux boot log message, as opposed to the console access provided over the USB port, which provides neither. Use appropriate serial communications software such as minicom for Linux, or putty for Windows. Configure the port for 115200,8,N,1 (8 data bits, no handshake, 1 stop bit).

Figure 5-1 shows the pin numbering for the DB9 connector, while Table 5-1 gives a detailed description of the signals at X8.
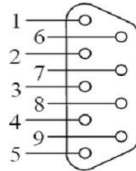
Figure 5- 1. RS-232 Connector X8 Pin Numbering

Table 5- 1. Connector X8 Pin Descriptions

Pin	Signal	I/O	Description
1	N/C	-	Not connected
2	UART0_TXD_RS232	O	UART0 transmit
3	UART0_RXD_RS232	I	UART0 receive
4	N/C	-	Not connected
5	GND	-	GND
6	N/C	-	Not connected
7	N/C	-	Not connected
8	N/C	-	Not connected
9	N/C	-	Not connected

6 USB Connectivity

6.1 USB Host (X3)

The USB1 interface signals route to the bottom connector of X3 (USB Dual Standard A and Ethernet). Note that the top USB connector of X3 is a not used. Although the USB interface of the Cosmic processor complies with USB 2.0 HS specification and supports dual role device configuration, due to its USB-A style connector, USB1 is limited to Host operation only.

The USB1 interface on the Cosmic board is equipped with ESD protection. It has its own 5V supply that is current limited by U4 (TPS2051B). It supports connection of different USB devices such as mass storage device, keyboard, and mouse.

To use the USB Host interface the board must be configured to provide power from the wall adapter input at X2 (see Figure 1-1). Set jumper JP1 to 1+2 to configure the board for wall power.

6.2 USB OTG (X6)

The USB0 interface signals route to connector X6 (USB Micro-AB). The USB interface of the Cosmic processor complies with USB 2.0 HS specification. Firmware interaction configures the interface to act in host or Device mode, making it a dual role device but not a true OTG controller as described in more detail in the Cosmic processor Reference Manual.

The USB0 interface on the Cosmic board is equipped with ESD protection. USB0_VBUS is connected to VBUS of the cable meaning USB0 is powered by the host.

This interface can be used both to power the board, and to provide serial console access. Connect a USB Standard-A to Micro-B, or Micro-AB cable between a host PC and connector X6. To configure the board for USB power, set jumper JP1 to 2+3 (see Figure 1-1). Once booted, the Cosmic Board shows up as a virtual serial port over USB. Use appropriate serial communications software such as minicom for Linux, or putty for Windows. Configure the port for 115200,8,N,1 (8 data bits, no handshake, 1 stop bit).

7 SD Card (X18)

The Cosmic board provides a Micro SD card slot at X18 for connection to the Cosmic's MMC0 interface. The interface is powered by an instant-on 3.3 V power supply and has card detect support (CDET) via the Cosmic processor A13 signal.

In addition to mass storage usage, the processor can boot from this interface. As the default boot mode of the phyCORE-Cosmic SOM, SD boot is selected by closing 3+4 pins of JP5 (see Figure 1-1).

7.1 Inserting and Removing an SD Card

Insert a micro SD Card into slot X18, label down and pins facing up. After aligning the card with the connector, push to insert. The card will make a clicking sound and latch into the connector. To eject the card, push the card in to release. The connector will click and the card will be safe to remove. To avoid damaging the connector do not attempt to pull the card directly out without first pushing inward to release the lock mechanism.

8 HDMI (X16)

A High-Definition Multimedia Interface (HDMI) transmitter is connected to the parallel display interface of the processor. The interface is compliant with HDMI 1.4a specification and available through the micro HDMI connector at X16. Connection to an HDMI display is limited to 1920x1080 (1080p) @ 24 Hz due to Cosmic processor limitations and compatible display clock frequency limitations.

The 24-bit Cosmic LCD interface (3 x 8-bit RGB) along with the Multichannel audio serial port(McASP) signals are converted to HDMI signals by the HDMI transmitter at U1. The transmitter is configured by the processor via I2C and although operating at 1.8V, can handle the 3.3V processor signals. Along with delivering Consumer Electronic Control (CEC) the device also supports a low power or standby mode when HDMI is not being used. A port protection and interface device at U13 provides ESD protection, integrated level shifting of HDMI signals, and a 50 mA / 5V current-limited supply to the HDMI sink device (monitor, TV, projector, etc).

For access to the HDMI output, a micro HDMI cable is required. For connection to general HDMI compliant devices, an HDMI to Micro HDMI cable will typical be used.

The display signals that are connected to the HDMI interface (LCD_D0 to LCD_D15) are available at the expansion connector so that they can be used for other purposes such as connecting to an LCD expansion board. Refer to Chapter 13 for additional information.

Note: HDMI Connector not mounted on Revision 1.0 board.

9 User Buttons

The Cosmic board is populated with four user accessible push buttons located at S1, S2, S3, and S4 to enable user input (see [Figure 1-1](#)). Each button is connected to a GPIO on the Cosmic processor. A detailed list of the user buttons is presented below.

S1   User Button 1 (BTN1). Pressing this button generates a debounced, active high signal to the processor at X_GPIO1_9. Holding this button will keep the output to held X_GPIO1_9   high. Releasing this button will keep the output to X_GPIO1_9 held low.

S2   User Button 2 (BTN2). Pressing this button generates a debounced, active high signal to the processor at X_GPIO3_4. Holding this button will keep the output to X_GPIO3_4 held   high. Releasing this button will keep the output to X_GPIO3_4 held low.

S3   User Button 3 (BTN3). Pressing this button generates a debounced, active high signal to the processor at X_GPIO1_24. Holding this button will keep the output to X_GPIO1_24 held   high. Releasing this button will keep the output to X_GPIO1_24 held low.

S4   User Button 4 (BTN4). Pressing this button generates a debounced, active high signal to the processor at X_GPIO1_20. Holding this button will keep the output to X_GPIO1_20 held   high. Releasing this button will keep the output to X_GPIO1_20 held low.

10 System Reset Button (S5)

The Cosmic Board is equipped with a system reset button at S5. Pressing the button will toggle the X_PB_RESETn signal low and generate a manual system reset driving RESETn on the phyCORE-AM335x low.

The system reset signal, RESETn, is available on the Expansion connector (see Chapter 13 for more information) and can be used to reset various other peripheral devices. Refer to the PCM-051/phyCORE-AM335x Hardware Manual for details on the RESETn signal.

| **CAUTION:** |
| When running Linux a proper system shutdown should be performed, or reboot executed instead of pressing the reset button. Pressing the reset button (or cutting power) without properly shutting down can cause file system errors and is not advised. Issue a poweroff or reboot command at the Linux prompt to avoid file system damage. Only use the reset button when not running Linux, or if the system freezes up. |

11 User LEDs

The Cosmic board is populated with four user programmable LEDs located at D11, D10, D4, and D5 to provide visual feedback to the user (see Figure 1-1). Each LED is connected to a GPIO on the Cosmic processor. A detailed list of the user LEDs is presented below.

D11 LED1 (Green). Connected to processor signal X_GPIO3_7. Drive signal X_GPIO3_7 high to turn this LED on and low to turn this LED off.

D10 LED2 (Green). Connected to processor signal X_GPIO1_27. Drive signal X_GPIO1_27   high to turn this LED on and low to turn this LED off.

D4 LED3 (Red). Connected to processor signal X_GPIO1_26. Drive signal X_GPIO1_26 high   to turn this LED on and low to turn this LED off.

D5 LED4 (Red). Connected to processor signal X_GPIO1_21. Drive signal X_GPIO1_21 high   to turn this LED on and low to turn this LED off.

12 Boot Selection (JP5)

Jumper JP5 provides a way to override the default boot option configured on the Cosmic SOM.
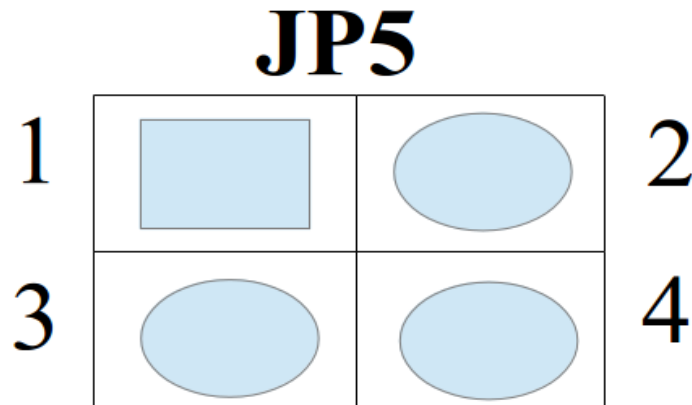
Figure 12- 1. Jumper Numbering Scheme

Figure 12-1 shows the jumper pin numbering scheme. Pin 1 on the board is marked with a number one on the PCB silk screen. It is also visibly marked with a clipped corner on the component outline.

Table 12-1 shows the required jumper positions for configuring the desired boot device. Use jumper wires to connect the pins of JP5 based on the settings described.

By default JP5 is open, configuring the Cosmic for NAND boot.

Table 12- 1. Jumper Settings and Descriptions

Jumper	Setting	Boot Device
JP5	**OPEN**	**NAND**
	1+2,3+4	NOR
	3+4	MMC0

13 Real-Time Clock Options (RTC)

There are two options for an RTC on the Cosmic-AM335x.

13.1 PMIC RTC

The Power Management IC at U4 includes an integrated RTC. This RTC includes alarm and time keeping functions. The RTC is supplied by the main system power when it is on, and by the backup battery voltage VBAT_IN_4RTC, if present, when the main system power is off and the jumper J10 has been moved from its default position of (1+2) to position (2+3).

13.2 AM335x RTC

The AM335x processor also includes an integrated RTC. However, the RTC integrated in the AM335x uses significantly more power than the RTC in the PMIC. Because of this power disadvantage, the SOM has not been designed to support the AM335x RTC with backup power.

To backup the RTC on the module, a secondary voltage source of 3 V can be attached to the Cosmic-AM335x at Jumper **JP4**. This voltage source supplies the backup voltage domain VBAT of the AM335x which supplies the RTC and some critical registers when the primary system power, VDD_3V3, is removed.

14 Controller Area Network (CAN) Interfaces

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real time control with a high level of security.

The CAN interface is accessible at the connector X25.

The PHYTEC cosmic board provides access to the CAN0 signals which are multiplexed onto the AM335x UART1_TX and UART1_RX pins. These signals route from the phyCORE connector to a CAN transceiver. The signals out of the transceiver route to X25.

Jumper JP3 can be installed to add a 120 Ohm termination resistor across the CAN data lines if needed.

Table 14- 1. Connector X25 Pin Descriptions

Pin	Signal	I/O	Description
1	N/C	-	Not connected
2	GND	-	GND
3	CAN _L	IO	Can Low
4	CAN_H	IO	Can High
5	GND	-	GND
6	N/C	-	Not connected
7	N/C	-	Not connected
8	N/C	-	Not connected
9	N/C	-	Not connected
10	N/C	-	Not connected

15 Expansion Connectors (X19, X20)

Two 2x30 2mm Expansion connectors (X19 and X20) provide easy access to many of the phyCORE-AM335x signals. All processor signals on the Expansion connector are 3.3 V. As an accessory, add-on expansion boards such as LCD and WiFi are made available through PHYTEC to connect to the Expansion connectors.

Most of the signals routed to the expansion connector have been configured for a given pin muxed function. Using these signals are alternate functions requires BSP modifications.

Tables detailing signal mapping of the Expansion Connectors are provided below. These tables list only the primary function intended on the Cosmic Board, but can be reconfigured for many other purposes. Refer to the AM335x Technical Reference manual on available operation modes.

Table 15- 2. Power Signal Map

Signal	Expansion Connector Pin	Description
VCC_5V0	X19-1, X19-3	5V power from currently selected source (wall or USB)
VCC_3V3	X19-2, X19-4	3.3V voltage domain
5V_IN	X19-5	5V power from wall adapter input
X_USB0_VBUS	X19-8	5V power from USB OTG connector
GND	X19-7, X19-10, X19-59, X19-60, X20-1, X20-2, X20-59, X20-60	Ground

Table 15- 3. System Signal Map

Signal	Expansion Board Pin	Type	Description
X_PB_RESETn	X20-58	O	System reset signal; can be used to reset external devices.
X_CLKOUT1	X19-12	O	CKLOUT1; free for external use

Table 15- 4. JTAG Signal Map

Signal	Expansion Board Pin	Type	Description
X_TDO	X19-18	O	JTAG test data output
X_TMS	X19-20	O	JTAG test mode select
X_TCK	X19-14	O	JTAG test clock input
X_nTRST	X19-22	I	JTAG test reset

X_TDI	X19-16	I	JTAG test data input

Table 15- 5. CAN Signal Map

Signal	Expansion Board Pin	Type	Description
X_GPIO1_9	X19-50	I	CAN1_RX; connected to PCL-051 CAN transceiver
X_GPIO1_8	X19-44	O	CAN1_TX; connected to PCL-051 CAN transceiver

Table 15- 6. I2C Signal Map

Signal	Expansion Board Pin	Type	Description
X_UART1_RXD/_P_UART0_RXD	X19-35	I/O	I2C1_SDA clock (open drain with pull-up resistor on the SOM)
X_UART1_TXD/_P_UART0_TXD	X19-37	I/O	I2C1_SCL data (open drain with pull-up resistor on the SOM)
X_UART1_RTS	X19-39	I/O	I2C2_SCL data (open drain with pull-up resistor on the SOM)
X_UART1_CTS	X19-41	I/O	I2C2_SDA data (open drain with pull-up resistor on the SOM)

Table 15- 7. UART Signal Map

Signal	Expansion Board Pin	Type	Description
X_UART1_TXD/_P_UART0_TXD	X19-37	O	UART 1 transmit data
X_UART1_RXD/_P_UART0_RXD	X19-35	I	UART 1 recieve data
X_UART1_RTS	X19-39	O	UART 1 request to send
X_UART1_CTS	X19-41	I	UART 1 clear to send
X_UART2_RX	X19-47	I	UART 2 recieve data
X_UART2_TX	X19-49	O	UART 2 transmit data
X_UART3_RX	X19-43	I	UART 3 recieve data
X_UART3_TX	X19-45	O	UART 3 transmit data
X_GPIO1_8	X19-44	I	UART 4 recieve data
X_GPIO1_9	X19-50	O	UART 4 transmit data

X_MII1_RCTL/_GPIO3_4	X19-51	O	UART 5 transmit data
X_MII1_COL/_MCASP1_AXR2	X19-57	I	UART 5 recieve data

Table 15- 8. SPI Signal Map

Signal	Expansion Board Pin	Type	Description
X_SPI0_SCLK	X19-46	O	SPI0 clock
X_SPI0_CS0	X19-48	O	SPI0 chip select 0
X_SPI0_D1	X19-56	I/O	SPI0 Data1 input / output
X_SPI0_D0	X19-58	I/O	SPI0 Data0 input / output
X_GPIO3_17	X19-40	O	SPI1 chip select 0
X_MII1_COL/_MCASP1_AXR2	X19-57	O	SPI1 clock
X_MCASP0_AXR0	X20-49	I/O	SPI1 Data1 input / output
X_MCASP0_FSX	X20-53	I/O	SPI1 Data0 input / output
X_ECAP0_IN_PWM0_OUT	X20-55	O	SPI1 chip select 1

Table 15- 9. ADC Signal Map

Signal	Expansion Board Pin	Type	Description
X_AIN0	X19-24	Analog	ADC input0; free for external use
X_AIN1	X19-26	Analog	ADC input1; free for external use
X_AIN2	X19-28	Analog	ADC input2; free for external use
X_AIN3	X19-30	Analog	ADC input3; free for external use
X_AIN4	X19-32	Analog	ADC input4; free for external use
X_AIN5	X19-34	Analog	ADC input5; free for external use
X_AIN6	X19-36	Analog	ADC input6; free for external use
X_AIN7	X19-38	Analog	ADC input7; free for external use

Table 15- 10. NAND (GPMC) Signal Map

Signal	Expansion Board Pin	Type	Description
X_GPMC_AD0	X20-33	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD1	X20-35	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD2	X20-37	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD3	X20-39	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD4	X20-41	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD5	X20-43	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD6	X20-32	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_AD7	X20-34	I/O	General Purpose Memory Controller interface Address/Data
X_GPMC_ADVn_ALE	X20-36	O	General Purpose Memory Controller interface address valid / address latch enable
X_GPMC_BE0n_CLE	X20-38	O	General Purpose Memory Controller interface byte enable 0 / command latch enable
X_GPMC_OEn_REn	X20-42	O	General Purpose Memory Controller output enable / read enable
X_GPMC_WAIT/_P_MII1_COL	X20-44	I/O	General Purpose Memory Controller WAIT / PRU Ethernet0 collision
X_GPMC_WEn	X20-46	O	General Purpose Memory Controller write enable

Table 15- 11. LCD Signal Map

Signal	Expansion Board Pin	Type	Description
X_LCD_D0	X20-19	O	LCD data bit 0
X_LCD_D1	X20-21	O	LCD data bit 1
X_LCD_D2	X20-23	O	LCD data bit 2
X_LCD_D3	X20-25	O	LCD data bit 3
X_LCD_D4	X20-27	O	LCD data bit 4

X_LCD_D5	X20-4	O	LCD data bit 5
X_LCD_D6	X20-6	O	LCD data bit 6
X_LCD_D7	X20-8	O	LCD data bit 7
X_LCD_D8	X20-10	O	LCD data bit 8
X_LCD_D9	X20-12	O	LCD data bit 9
X_LCD_D10	X20-14	O	LCD data bit 10
X_LCD_D11	X20-22	O	LCD data bit 11
X_LCD_D12	X20-24	O	LCD data bit 12
X_LCD_D13	X20-26	O	LCD data bit 13
X_LCD_D14	X20-28	O	LCD data bit 14
X_LCD_D15	X20-30	O	LCD data bit 15
X_LCD_D16	X20-17	O	LCD data bit 16
X_LCD_D17	X20-20	O	LCD data bit 17
X_LCD_D18	X20-15	O	LCD data bit 18
X_LCD_D19	X20-31	O	LCD data bit 19
X_LCD_D20	X20-18	O	LCD data bit 20
X_LCD_D21	X20-13	O	LCD data bit 21
X_LCD_D22	X20-29	O	LCD data bit 22
X_LCD_D23	X20-16	O	LCD data bit 23
X_LCD_PCLK	X20-7	O	LCD Pixel Clock
X_LCD_AC_BIAS_EN	X20-11	O	LCD Bias enable chip select
X_ECAP0_IN_PWM0_OUT	X20-55	O	PWM output, can be used for display brightness control
X_LCD_VSYNC	X20-5	O	LCD Vertical synchronization
X_LCD_HSYNC	X20-3	O	LCD Horizontal synchronization

Table 15- 12. Multichannel Audio Serial Ports (McASP) Signal Map

Signal	Expansion Board Pin	Type	Description
X_McASP0_AXR0	X20-49	I/O	serial data
X_McASP0_FSX	X20-53	I/O	frame synchronization transmit

X_McASP0_AHCLKX	X20-47	I/O	high frequency clock
X_McASP0_AXR1	X20-51	I/O	serial data
X_McASP0_ACLKX	X20-45	I/O	transmit bit clock

Table 15- 13. General Purpose I/O's (GPIO's) Signal Map

Signal	Expansion Board Pin	Type	Description
X_MMC2_CMD/_P_MDIO_DATA/GPIO2_0	X20-54	I/O	gpio2_0
X_MMC2_CLK/_P_MDIO_MDCLK	X20-50	I/O	gpio2_1
X_LCD_D15/_P_MII0_RXDV	X20-30	I/O	gpio0_11
X_LCD_D14/_P_MII0_MR_CLK	X20-28	I/O	gpio0_10
X_LCD_D13/_P_MII0_RXER	X20-26	I/O	gpio0_9
X_LCD_D12	X20-24	I/O	gpio0_8
X_LCD_D11	X20-22	I/O	gpio2_17
X_LCD_D5	X20-4	I/O	gpio2_11
X_LCD_D6	X20-6	I/O	gpio2_12
X_LCD_D7	X20-8	I/O	gpio2_13
X_LCD_D8	X20-10	I/O	gpio2_14
X_LCD_D9	X20-12	I/O	gpio2_15
X_LCD_D10	X20-14	I/O	gpio2_16
X_MCASP0_ACLKX	X20-45	I/O	gpio3_14
X_MCASP0_AHCLKX	X20-47	I/O	gpio3_21
X_MCASP0_AXR0	X20-49	I/O	gpio3_16
X_MCASP0_AXR1	X20-51	I/O	gpio3_20
X_MCASP0_FSX	X20-53	I/O	gpio3_15
X_ECAP0_IN_PWM0_OUT	X20-55	I/O	gpio0_7
X_LCD_D0/_P_MII0_MT_CLK	X20-19	I/O	gpio2_6
X_LCD_D1/_P_MII0_TXEN	X20-21	I/O	gpio2_7
X_LCD_D2/_P_MII0_TXD3	X20-23	I/O	gpio2_8
X_LCD_D3/_P_MII0_TXD2	X20-25	I/O	gpio2_9
X_LCD_D4/_P_MII0_TXD1	X20-27	I/O	gpio2_10
X_LCD_HSYNC	X20-3	I/O	gpio2_23
X_LCD_VSYNC	X20-5	I/O	gpio2_22

X_LCD_PCLK/_P_MII0_CRS	X20-7	I/O	gpio2_24
X_LCD_AC_BIAS_EN_/P_MII1_CRS	X20-11	I/O	gpio2_25
X_GPIO3_19	X19-42	I/O	gpio3_19
X_GPIO1_8	X19-44	I/O	gpio1_8
X_GPIO1_30	X19-52	I/O	gpio1_30
X_GPIO1_31	X19-54	I/O	gpio1_31
X_RGMII2_INT/_MMC2_DAT3/_P_MII1_RXLINK	X19-9	I/O	gpio1_28
X_RGMII2_RCLK/_MMC2_DAT5/_P_MII1_RXD1	X19-11	I/O	gpio1_23
X_RGMII2_RCTL/_MMC2_DAT0/_P_MII1_TXD3	X19-13	I/O	gpio1_17
X_RGMII2_RD2/_MMC2_DAT7/_P_MII1_MR_CLK	X19-19	I/O	gpio1_25
X_RGMII2_TCTL/_P_MII1_MT_CLK	X19-25	I/O	gpio1_16
X_RGMII2_TD2/_MMC2_DAT2/_P_MII1_TXD1	X19-31	I/O	gpio1_19
X_RGMII2_TD3/_MMC2_DAT1/_P_MII1_TXD2	X19-33	I/O	gpio1_18
X_UART1_RTS	X19-39	I/O	gpio0_13
X_UART1_CTS	X19-41	I/O	gpio0_12
X_INTR1/XDMA_EVENT_INTR1/TCLKIN/CLKOUT2	X20-57	I/O	gpio0_20
X_RGMII2_TCLK/_MMC2_DAT4/_P_MII1_RXD2	X19-23	I/O	gpio1_22
X_UART1_RXD/_P_UART0_RXD	X19-35	I/O	gpio0_14
X_UART1_TXD/_P_UART0_TXD	X19-37	I/O	gpio0_15
X_LCD_D16	X20-17	I/O	gpio1_15
X_LCD_D17	X20-20	I/O	gpio1_14
X_LCD_D18	X20-15	I/O	gpio1_13
X_LCD_D19	X20-31	I/O	gpio1_12
X_LCD_D20	X20-18	I/O	gpio0_27
X_LCD_D21	X20-13	I/O	gpio0_26
X_LCD_D22	X20-29	I/O	gpio0_23
X_LCD_D23	X20-16	I/O	gpio0_22
X_GPIO3_17	X19-40	I/O	gpio3_17

X_CLKOUT1	X19-12	I/O	gpio0_19
X_UART3_TX	X19-45	I/O	gpio2_19
X_UART3_RX	X19-43	I/O	gpio2_18
X_UART2_TX	X19-49	I/O	gpio3_10
X_UART2_RX	X19-47	I/O	gpio3_9
X_MII1_COL/_MCASP1_AXR2	X19-57	I/O	gpio3_0

Table 15- 14. Ethernet (RGMII) Signal Map

Signal	Expansion Board Pin	Type	Description
X_RGMII2_TCTL/_P_MII1_MT_CLK	X19-25	O	RGMII transmit control
X_RGMII2_TCLK/_MMC2_DAT4/_P_MII1_RXD2	X19-23	O	RGMII transmit clock
X_RGMII2_TD3/_MMC2_DAT1/_P_MII1_TXD2	X19-33	O	RGMII transmit data bit 3
X_RGMII2_TD2/_MMC2_DAT2/_P_MII1_TXD1	X19-31	O	RGMII transmit data bit 2
X_RGMII2_TD1/_P_MII1_TXD0	X19-29	O	RGMII transmit data bit 1
X_RGMII2_TD0/_P_MII1_RXD3	X19-27	O	RGMII transmit data bit 0
X_RGMII2_RCTL/_MMC2_DAT0/_P_MII1_TXD3	X19-13	I	RGMII receive control
X_RGMII2_RCLK/_MMC2_DAT5/_P_MII1_RXD1	X19-11	I	RGMII receive clock
X_RGMII2_RD3/_MMC2_DAT6/_P_MII1_RXD0	X19-21	I	RGMII receive data bit 3
X_RGMII2_RD2/_MMC2_DAT7/_P_MII1_MR_CLK	X19-19	I	RGMII receive data bit 2
X_RGMII2_RD1/_P_MII1_RXDV	X19-17	I	RGMII receive data bit 1
X_RGMII2_RD0/_P_MII1_RXER	X19-15	I	RGMII receive data bit 0

16 Technical Specifications

The physical dimensions of the Cosmic Board for phyCORE-AM335x are presented in Figure 15-1. A summary of technical specifications is provided in Table 15-1.
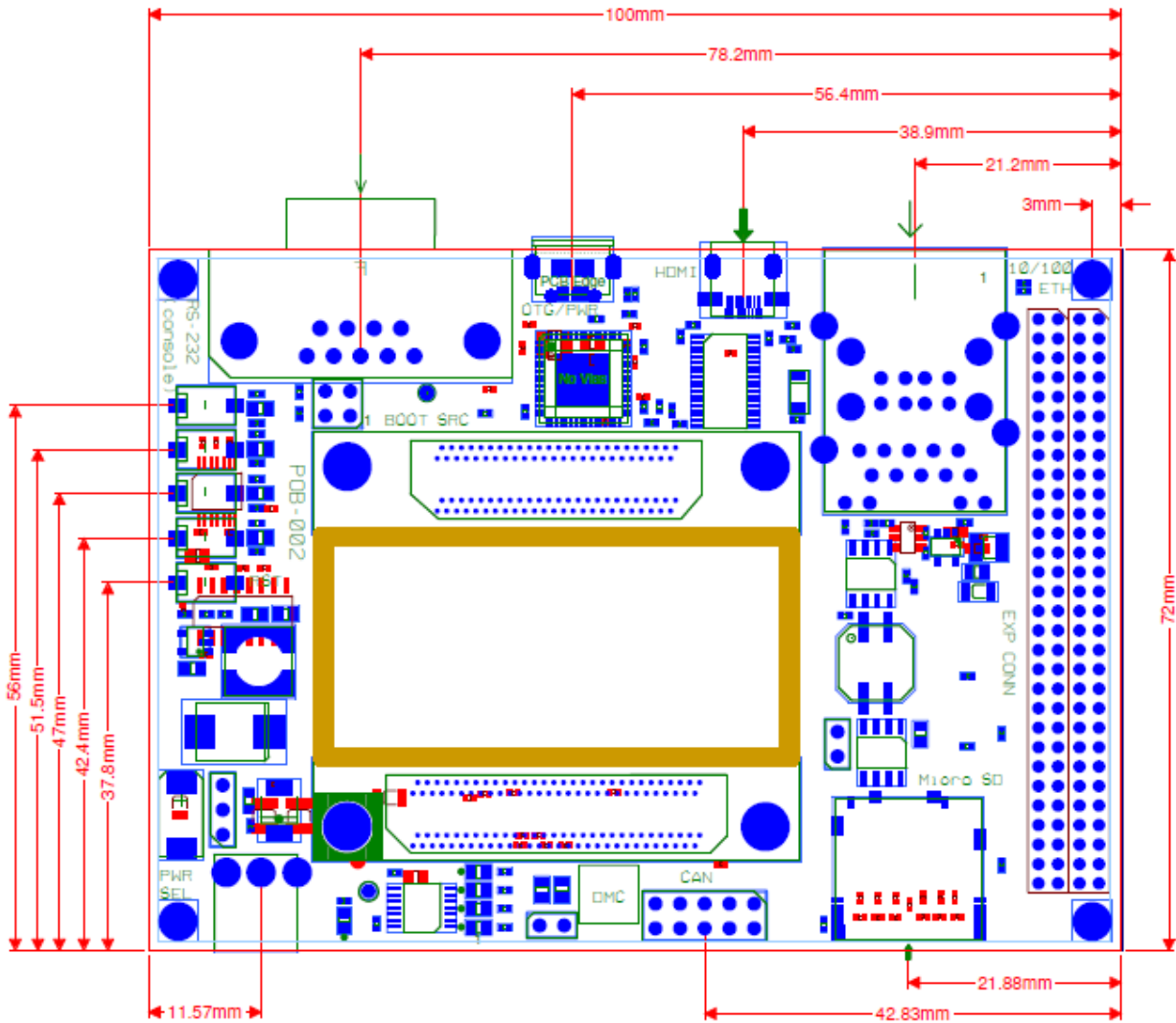

Fig. 16-1. Cosmic Board Physical Dimensions

Table 16- 1. Technical Specifications

Dimensions	100 x 72mm
Weight	64.2g / 2.26oz typ.
Storage Temperature	-40 °C to +125 °C
Operating Temperature	0 °C to +70 °C (commercial)
Humidity	95% r.F. not condensed
Operating Voltage	+5VDC +- 5%
Power Consumption	1.83W typ.; Linux booted from uSD card, running ping test

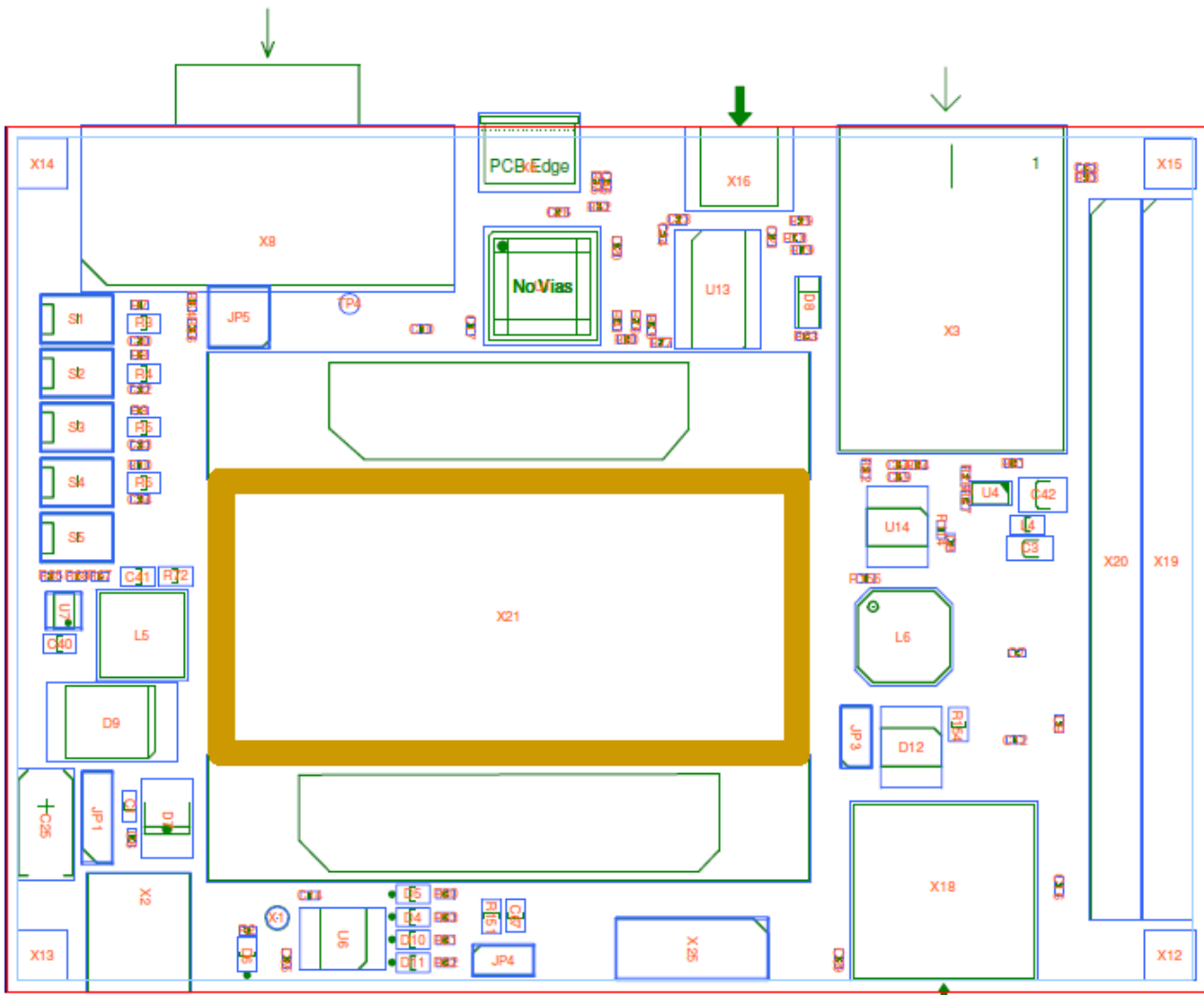## 17 Component Placement Diagrams
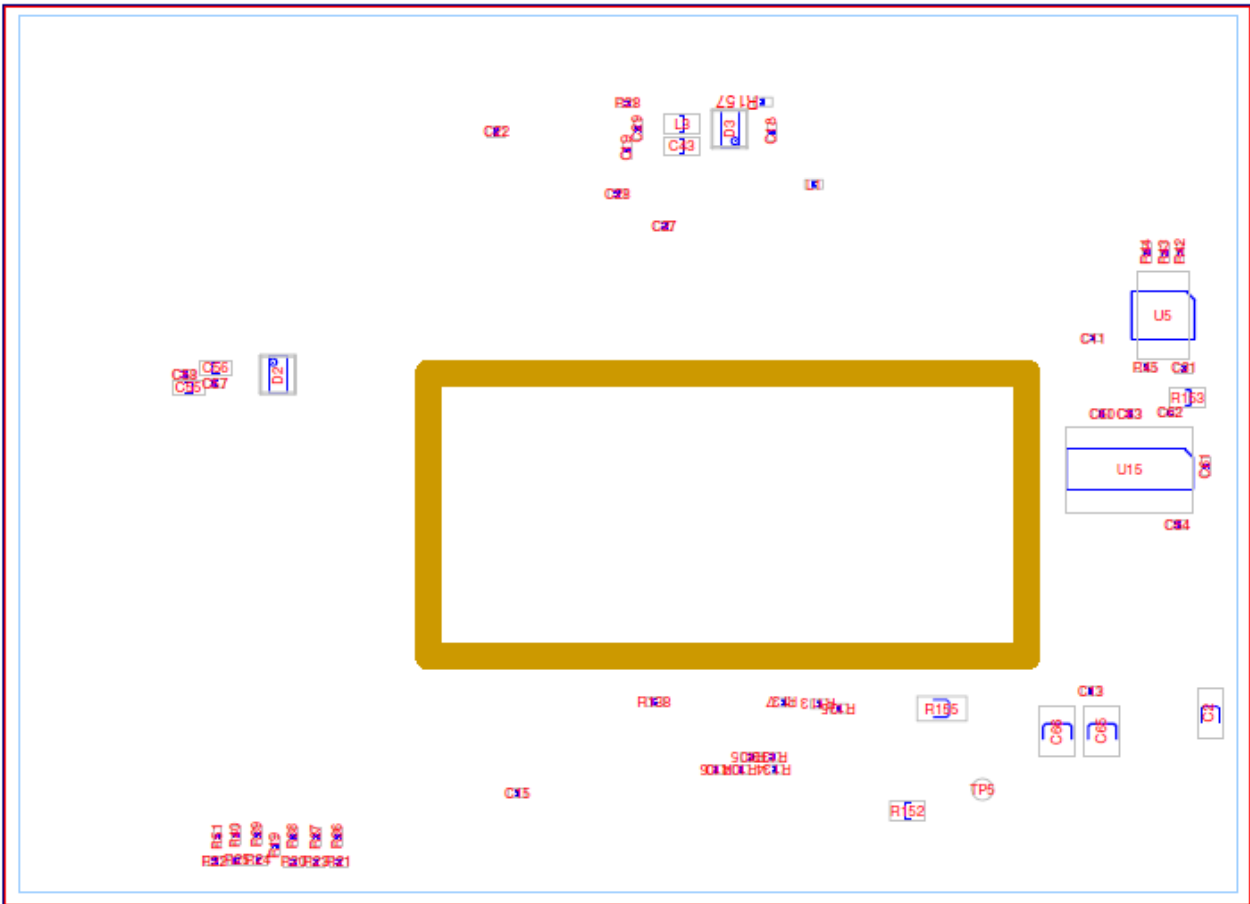

Figure 17- 1. Cosmic Board Top

Figure 17- 2. Cosmic Board Bottom

Revision History

Table 18- 1. Revision History

Date	Version Number	Changes in this Manual
31/10/2013		Release