PBA-CD-10
phyBOARD-Segin with phyCORE-i.MX 6UL/ULL, phyCORE-i.MX 93 or phyCORE-STM32MP1

PHYTEC	PHYTEC Messtechnik GmbH Barcelona-Allee 1 D-55129 Mainz	
Project: PBA-CD-10 (PB-02013, PB-02029, PB-02030)	Department : F&E Author: A.Beuscher, R.Stidronski, H.Atifi	
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Project Overview

Operating Voltage: 5V +/- 5%

Size: 100mm x 72mm x 40mm

I2C addresses used on SOM:	i.MX 6UL/ULL	i.MX 93
- EEPROM on SOM Memory Area	0x52	0x50
- EERPOM on SOM ID Page	0x5A	0x58

Onboard used I2C addresses:	I2C1	I2C2
- 0x18 Stereo Audio Codec		
- 0x49 Resistive Touch Controller		
- 0x54 EEPROM Memory Area		
- 0x5C EEPROM ID Page		
- 0x68 External RTC		

Please consider expansion boards for additional I2C devices:
- A/V Connector
- Expansion Connector
- Camera Interface (0x48, 0x5d, 0x45 should be reserved for phyCAM-P)

	EUROPE	NORTH AMERIKA
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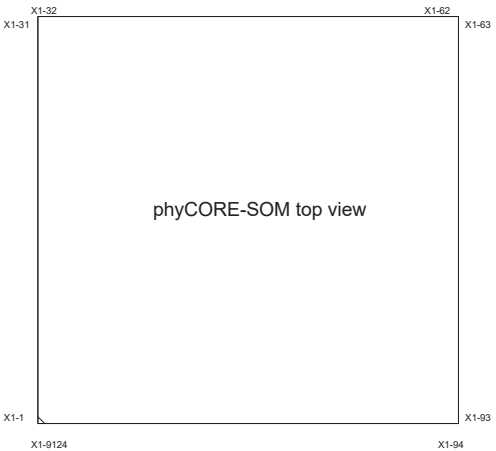
phyCORE-Connector Comparison

The phyBOARD-Segin carrier board (PB-CD-10) is designed to accommodate 3 different phyCORE modules. All three modules belong to a pin-compatible family of phyCORE modules with the same footprint. Unfortunately, only the signal names of our phyCORE-i.MX6 UL/ULL (PCL-063) match the signal names of the phyBOARD-Segin carrier board (PB-CD-10). The signal names of the phyCORE-i.MX 91/93 (PCL-077) and phyCORE-STM32MP13 (PCL-076) do not match those of the phyBOARD-Segin carrier board and must be translated when following signal paths from the phyCORE module to the phyBOARD carrier board. To make this task easier, we have created the translation table below. The first column lists the signal names of the phyCORE-i.MX 6UL/ULL (PCL-063) and the phyBOARD-Segin carrier board (PB-CD-10). The columns to the right contain the signal names of the phyCORE-i.MX 91/93 (PCL-077) and phyCORE-STM32MP13 (PCL-076). The signal names are then matched across the row. Since the signal names meet at connector X1, we have grouped the pin numbers of X1 into 4 groups for better orientation.

i.MX6UL/ULL Functions	i.MX93 Functions	STM32 Functions	i.MX6UL/ULL Functions	i.MX93 Functions	STM32 Functions
X1-[1:31]	X1-[1:31]	X1-[1:31]	X1-[32:62]	X1-[32:62]	X1-[32:62]
GND	GND	GND	GND	GND	GND
X_CSI_VSYNC	X_TAMPER1 *	X_DCMIPP_VSYNC	X_LCD_D7	X_LCD_D7 (X_pCAM_D5)	X_LTDC_G3
X_CSI_HSYNC	X_ADC_IN1 *	X_DCMIPP_HSYNC	X_LCD_D8	X_LCD_D8 (X_LVDS_CLK_P)	X_LTDC_G4
X_CSI_PIXCLK	X_ADC_IN2 *	X_DCMIPP_PIXCLK	X_LCD_D9	X_LCD_D9 (X_LVDS_CLK_N)	X_LTDC_G5
X_CSI_MCLK	X_SD2_nRESET **	X_DCMIPP_CLK	X_LCD_D10	X_LCD_D10 (X_pCAM_D6)	X_LTDC_G6
X_SD1_CLK	X_SD2_CLK **	X_SDMMC1_CLK	X_LCD_D11	X_LCD_D11 (X_pCAM_D7)	X_LTDC_G7
X_SD1_CMD	X_SD2_CMD **	X_SDMMC1_CMD	X_LCD_D12	X_LCD_D12 (X_LVDS_D2_P)	X_LTDC_R2
X_SD1_D0	X_SD2_D0 **	X_SDMMC1_D0	X_LCD_D13	X_LCD_D13 (X_pCAM_D8)	X_LTDC_R3
X_SD1_D1	X_SD2_D1 **	X_SDMMC1_D1	X_LCD_D14	X_LCD_D14 (X_pCAM_D9)	X_LTDC_R4
X_SD1_D2	X_SD2_D2 **	X_SDMMC1_D2	X_LCD_D15	X_LCD_D15 (X_LVDS_D2_N)	X_LTDC_R5
X_SD1_D3	X_SD2_D3 **	X_SDMMC1_D3	X_LCD_D16	X_LCD_D16 (X_LVDS_D3_P)	X_LTDC_R6
X_ENET1_TX+	X_ENET2_TX+	X_ENET1_TX+	X_LCD_D17	X_LCD_D17 (X_LVDS_D3_N)	X_LTDC_R7
X_ENET1_TX-	X_ENET2_TX-	X_ENET1_TX-	X_LCD_D18	X_LCD_D18 (X_SD3_CLK)	NC
X_ENET1_RX+	X_ENET2_RX+	X_ENET1_RX+	X_LCD_D19	X_LCD_D19 (X_SD3_CMD)	NC
X_ENET1_RX-	X_ENET2_RX-	X_ENET1_RX-	X_LCD_D20	X_LCD_D20 (X_SD3_D0)	NC
X_ENET1_LED1	X_ENET2_LED1	X_ENET1_LED1	X_LCD_D21	X_LCD_D21 (X_SD3_D1)	NC
X_ENET1_LED0	X_ENET2_LED0	X_ENET1_LED0	X_LCD_D22	X_LCD_D22 (X_SD3_D2)	NC
X_ENET_MDIO	X_ENET2_MDIO	X_ETH2_MDIO	X_LCD_D23	X_LCD_D23 (X_SD3_D3)	NC
X_ENET_MDC	X_ENET2_MDC	X_ETH2_MDC	X_CSI_FIELD	X_ENET1_TD3	X_GPIO_PE6
X_LCD_ENABLE	X_LCD_ENABLE (X_pCAM_D0)	X_LTDC_DE	X_GPIO5_9	X_ENET1_TD2	X_GPIO_PI2
X_LCD_CLK	X_LCD_CLK (X_pCAM_PCLK)	X_LTDC_CLK	X_ENET2_TX_D0	X_ENET1_TD0	X_ETH2_TXD0
X_LCD_VSYNC	X_LCD_VSYNC (X_pCAM_FVALID)	X_LTDC_VSYNC	X_ENET2_TX_D1	X_ENET1_TD1	X_ETH2_TXD1
X_LCD_RESET	X_LCD_RESET (X_LVDS_D0_P)	X_LTDC_RESET	X_ENET2_TX_EN	X_ENET1_TX_CTL	X_ETH2_TX_EN
X_LCD_HSYNC	X_LCD_HSYNC (X_pCAM_LVALID)	X_LTDC_HSYNC	X_ENET2_TX_CLK	X_ENET1_TXC	X_ETH2_CLK
X_LCD_D0	X_LCD_D0 (X_LVDS_D0_N)	X_LTDC_B2	X_ENET2_RX_D0	X_ENET1_RD0	X_ETH2_RXD0
X_LCD_D1	X_LCD_D1 (X_LVDS_D1_P)	X_LTDC_B3	X_ENET2_RX_D1	X_ENET1_RD1	X_ETH2_RXD1
X_LCD_D2	X_LCD_D2 (X_LVDS_D1_N)	X_LTDC_B4	X_ENET2_RX_ER	X_ENET1_RXC	X_ETH2_RX_ER
X_LCD_D3	X_LCD_D3 (X_pCAM_D1)	X_LTDC_B5	X_ENET2_RX_EN	X_ENET1_RX_CTL	X_ETH2_CRS_DV
X_LCD_D4	X_LCD_D4 (X_pCAM_D2)	X_LTDC_B6	X_I2C1_SCL	X_ENET1_RD2	X_I2C5_SCL
X_LCD_D5	X_LCD_D5 (X_pCAM_D3)	X_LTDC_B7	X_I2C1_SDA	X_ENET1_RD3	X_I2C5_SDA
X_LCD_D6	X_LCD_D6 (X_pCAM_D4)	X_LTDC_G2	GND	GND	GND

i.MX6UL/ULL Functions	i.MX93 Functions	STM32 Functions	i.MX6UL/ULL Functions	i.MX93 Functions	STM32 Functions
X1-[63:93]	X1-[63:93]	X1-[63:93]	X1-[94:124]	X1-[94:124]	X1-[94:124]
X_UART5_TX	X_UART_via_FLEXIO	X_USART2_TX	VDD_SNVS	N.C.	VBAT
X_UART5_RX	X_UART_via_FLEXIO	X_USART2_RX	X_GPIO5_5	X_I2C2_SCL_GPIO1_IO2	X_GPIO_PF5
X_USB_OTG1_D-	X_USB1_D_N	X_USB_OTG_HS_DM	X_GPIO1_1	X_I2C2_SDA_GPIO1_IO3	X_GPIO_PE8
X_USB_OTG1_D+	X_USB1_D_P	X_USB_OTG_HS_DP	X_USB_OTG1_ID	X_USB1_ID	X_USB_OTG_HS_ID
X_USB_OTG1_VBUS	X_USB1_VBUS	X_USB_OTG_HS_VBUS	X_nRESET_OUT	X_nRESET_OUT	X_nRESET_OUT
X_USB_OTG1_CHD	X_CLKIN1 *	NC	X_ONOFF	X_ONOFF *	TBD
X_USB_OTG2_D-	X_USB2_D_N	X_USBH_HS1_DM	X_nRESET_IN	X_nRESET_IN *	X_nRESET_IN
X_USB_OTG2_D+	X_USB2_D_P	X_USBH_HS1_DP	X_SVNS_PMIC_ON_REQ	X_PMIC_ON_REQ *	TBD
X_USB_OTG2_VBUS	X_USB2_VBUS	NC	X_PMIC_STBY_REQ	X_PMIC_STBY_REQ *	TBD
X_CCM_CLK1_P	X_CLKO1	X_GPIO_PC13	X_BOOT_MODE1	X_nPWR_READY - external Pull-Up required!	NC
X_CCM_CLK1_N	X_CLKO2	X_GPIO_PF8	X_BOOT_MODE0	X_TAMPER0 *	NC
X_UART5_RTS_B	X_SD3_DATA2	X_USART2_CTS	X_UART1_RX	X_UART1_RXD	X_UART4_RX
X_UART5_CTS_B	X_SD3_DATA3	X_USART2_RTS	X_GPIO1_18	X_GPIO4_29	X_GPIO_PB1
X_USB_OTG2_ID	X_USB2_ID	NC	X_UART1_TX	X_UART1_TXD_BOOT_MODE0	X_UART4_TX
X_PWM3_OUT	X_GPIO_via_FLEXIO	X_PWM_PE5	X_nSD1_CD	X_SD2_nCD **	X_GPIO_PI1
X_GPIO1_3	X_I2C1_SCL	X_GPIO_PF12	X_ECSPI3_CLK	X_SAI1_TXD0_BOOT_MODE3_UART2_RTS_B	X_SPI1_SCK
X_JTAG_TDI/SAI2_TX_BCLK	X_dap_TDI	X_JTAG_TDI_GPIO_PH4	X_ECSPI3_MOSI	X_SAI1_RXD0	X_SPI1_MOSI
X_JTAG_TCK/SAI2_RXD	X_dap_TCLK	X_JTAG_TCK_GPIO_PF14	X_ECSPI3_SS0	X_SAI1_TXFS_BOOT_MODE2	X_SPI1_nSS
X_JTAG_MOD	X_ADC_IN0 *	NC	X_ECSPI3_MISO	X_SAI1_TXC_UART2_CTS_B	X_SPI1_MISO
X_JTAG_TDO/SAI2_TX_SYNC	X_dap_TDO	X_JTAG_TDO_GPIO_PH5	X_FLEXCAN1_RX	X_PDM_BS0_CAN1_RX	X_FDCAN2_RX
X_JTAG_TMS/SAI2_MCLK	X_dap_TMS	X_JTAG_TMS_GPIO_PF15	X_FLEXCAN1_TX	X_PDM_CLK_CAN1_TX	X_FDCAN2_TX
X_JTAG_TRST_B/SAI2_TXD	X_I2C1_SDA	X_JTAG_TRST_GPIO_PA0	X_CSI_D0	X_UART2_RX_UART1_CTS_B_SAI1_MCLK	X_UART7_RX
X_GPIO5_3	X_SD3_CMD_GPIO3_IO21	X_GPIO_PA13	X_CSI_D1	X_UART2_TX_UART1_RTS_B_BOOT_MODE1	X_UART7_TX
X_GPIO5_2	X_GPIO4_16	X_GPIO_PA14	X_CSI_D2	X_WDOG_ANY	X_DCMIPP_D0
X_GPIO5_1	X_GPIO3_7	X_GPIO_PG12	X_CSI_D3	X_CLKIN2 *	X_DCMIPP_D1
X_GPIO5_0	X_PDM_BS1_GPIO1_IO10	X_GPIO_PA6	X_CSI_D4	X_MIPI_CSI_CLK_N	X_DCMIPP_D2
GND	GND	GND	X_CSI_D5	X_MIPI_CSI_CLK_P	X_DCMIPP_D3
VDD_3V3	VDD_3V3	VDD_3V3	X_CSI_D6	X_MIPI_CSI_D0_N	X_DCMIPP_D4
VDD_3V3	VDD_3V3	VDD_3V3	X_CSI_D7	X_MIPI_CSI_D0_P	X_DCMIPP_D5
VDD_3V3	VDD_3V3	VDD_3V3	X_CSI_D8	X_MIPI_CSI_D1_N	X_DCMIPP_D6
VDD_3V3	VDD_3V3	VDD_3V3	X_CSI_D9	X_MIPI_CSI_D1_P	X_DCMIPP_D7



* all signals have 1.8V voltage level

** 1.8V / 3.3V depending on interface mode

In addition to the table above, we also provide a more detailed Excel spreadsheet showing the complete default signal path of our reference design, from the processor to the carrier board. The standard Linux device tree muxing option is also included. This gives a developer all the information needed in one place to make muxing changes and design options more convenient when developing a special carrier board or customizing a PHYTEC phyCORE System on Module to an application. The spread sheet can be found in the download area of the desired phyCORE module, under Design Files -> Pinmuxing -> Pinout Table...

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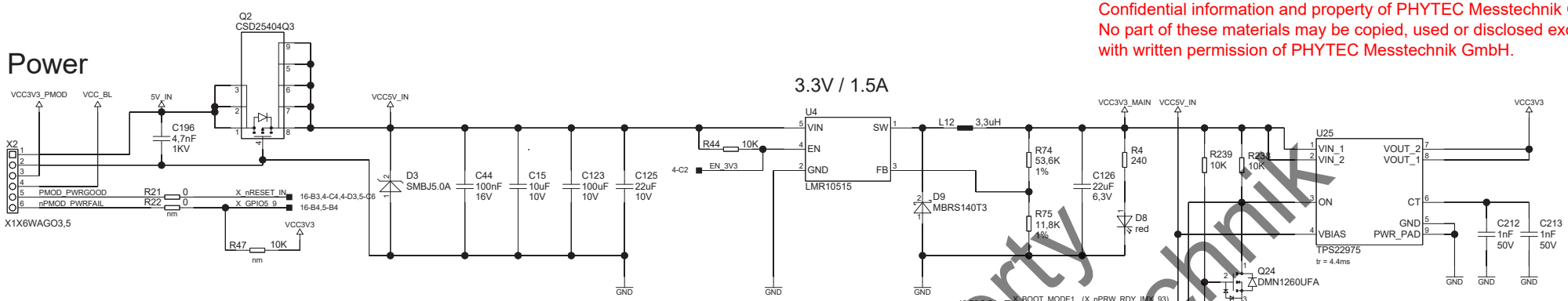
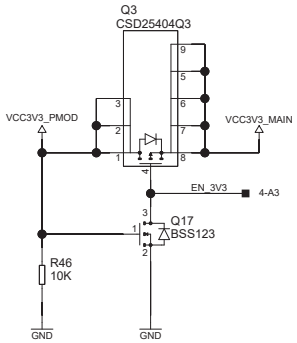
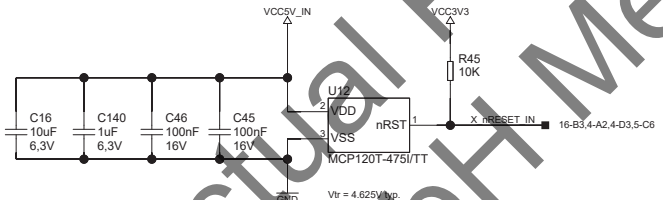
Power

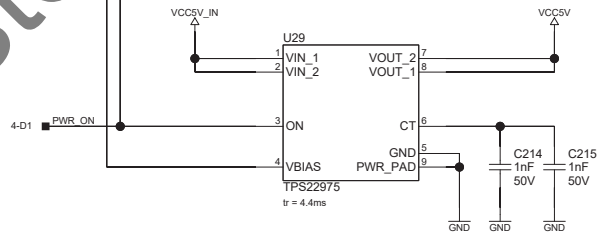


3V3 Supply Selector

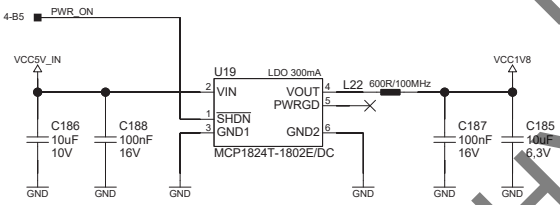


Voltage Supervisor

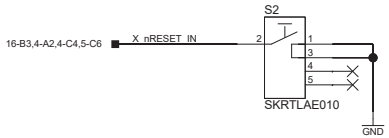




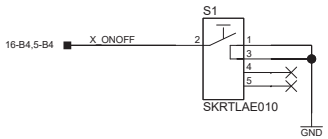
1.8V Power Supply



System Reset Button



CPU ON/OFF Button



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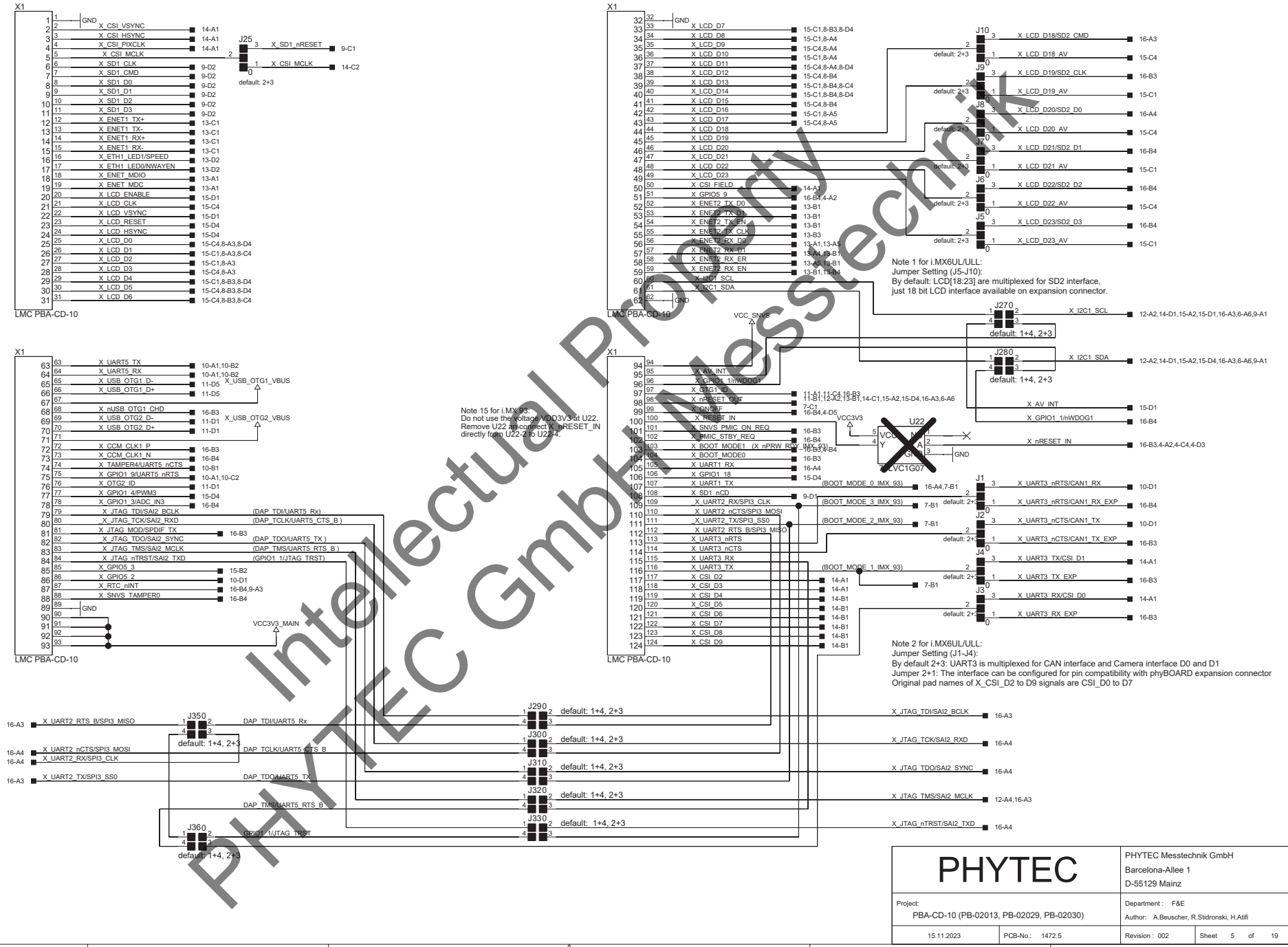
phyCORE-i.MX 6UL / i.MX 93 / STM32MP1 Connectors



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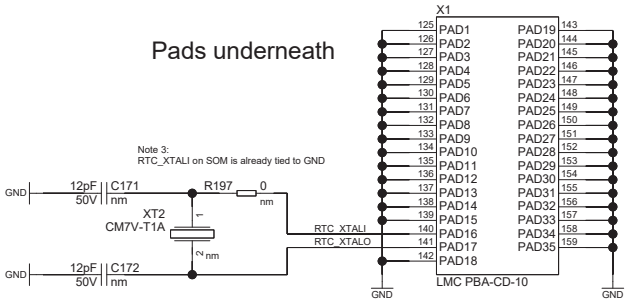
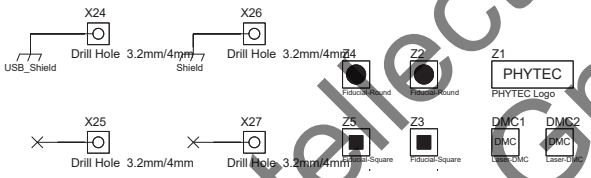
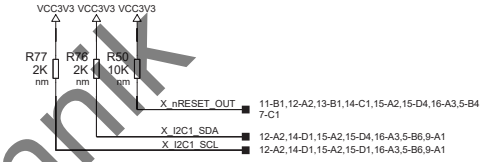
phyCORE-i.MX 6UL / i.MX 93 / STM32MP1 Connectors

Pads underneath

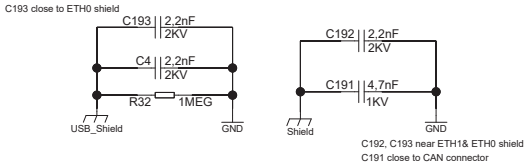




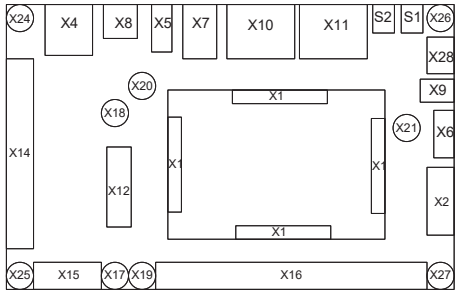
Pullups



Shield Coupler



Drill Hole Placement



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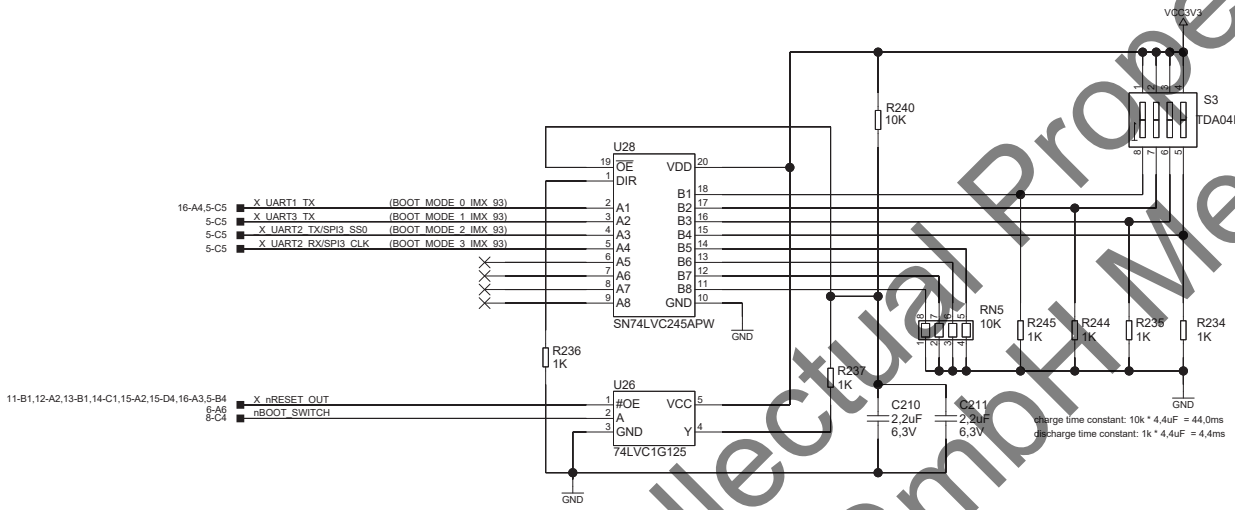
Boot Mode i.MX 93



Supported Boot Modes of SOM phyCORE-i.MX 93:	
BOOT_MODE[3:0]	Description
0000	Boot from internal fuses
0001	Serial Download (USB1)
0010	uSDHC1 8-bit eMMC 5.1 (default)
0011	uSDHC2 4-bit SD 3.0
1000	LPB: Boot from internal fuses
1001	LPB: Serial Download (USB1)
1010	LPB: uSDHC1 8-bit eMMC 5.1
1011	LPB: uSDHC2 4-bit SD 3.0

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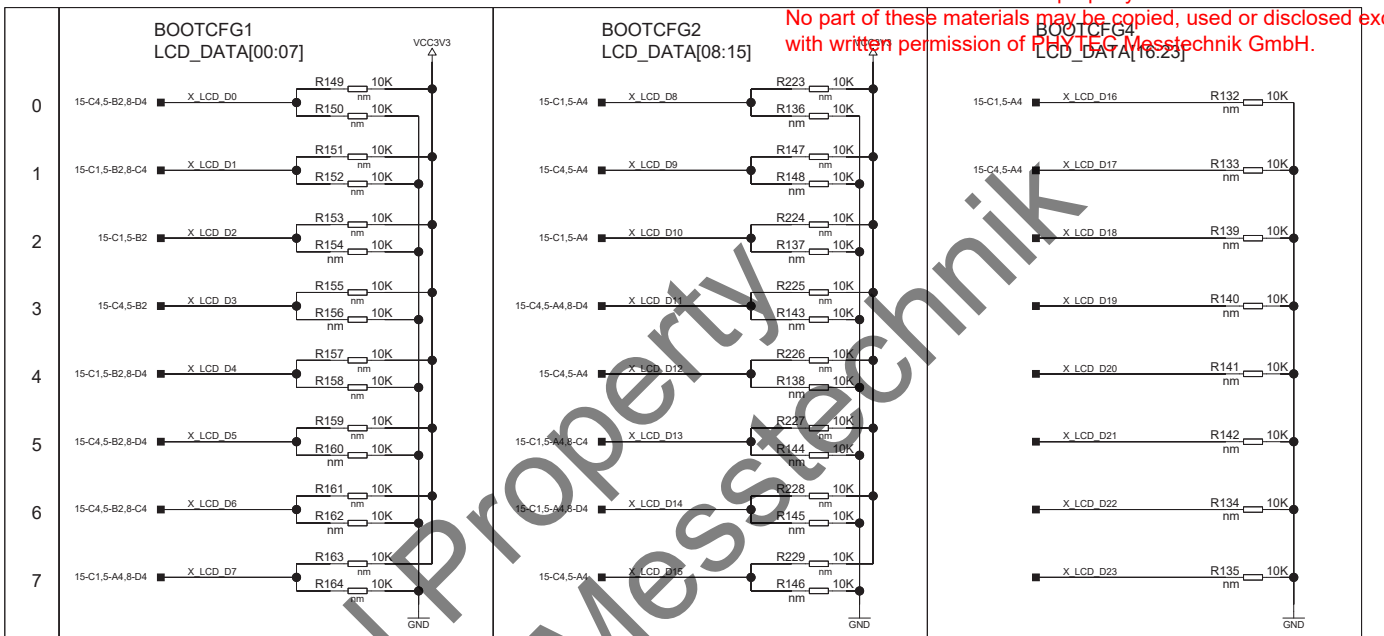
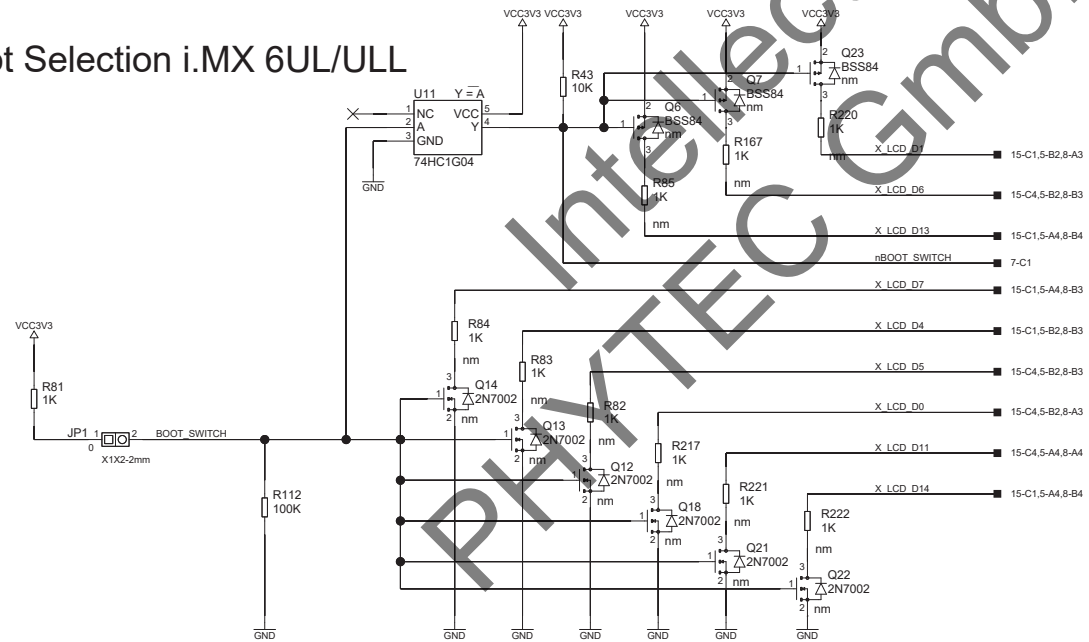
Boot Configuration i.MX 6UL/ULL



Description	BOOTCFG1[7:0] XXXXXXXX	BOOTCFG2[7:0] XXXXXXXX	BOOTCFG4[7:0] 00000000	mounted	not mounted
NAND 1Gbit (128MByte) (64 pages per block, 4 address bytes)	10010010	00000000	00000000	R150,151,154,156,157,160,162,163,136,148,137,143,138,144,145,146	R149,152,153,155,158,159,161,164,223,147,224,225,226,227,228,229
NAND 2/4Gbit (512MByte) (64 pages per block, 5 address bytes)	10010011	00000000	00000000	R149,151,154,156,157,160,162,163,148,136,137,143,138,144,145,146	R150,152,153,155,158,159,161,164,223,147,224,225,226,227,228,229
SD Card (usdhc1 interface)	01000010	00100000	00000000		
eMMC (usdhc2 interface)	01100000	01001000	00000000	R150,152,154,156,158,159,161,164,136,148,137,225,138,144,228,146	R149,151,153,155,157,160,162,163,223,147,224,143,226,227,145,229

Boot Selection i.MX 6UL/ULL



BOOT_CFG	NAND -> SD	eMMC -> SD
BOOT_CFG1 [1]		0 -> 1
BOOT_CFG1 [6]	0 -> 1	
BOOT_CFG2 [5]	0 -> 1	0 -> 1
BOOT_CFG1 [7]	1 -> 0	
BOOT_CFG1 [4]	1 -> 0	
BOOT_CFG1 [5]		1 -> 0
BOOT_CFG1 [0]	1 -> 0	
BOOT_CFG2 [3]		1 -> 0
BOOT_CFG2 [6]		1 -> 0

PHYTEC

PHYTEC Messtechnik GmbH
Barcelona-Allee 1
D-55129 Mainz

Project: PBA-CD-10 (PB-02013, PB-02029, PB-02030)
Department : F&E
Author: A.Beuscher, R.Stidronski, H.Atifi

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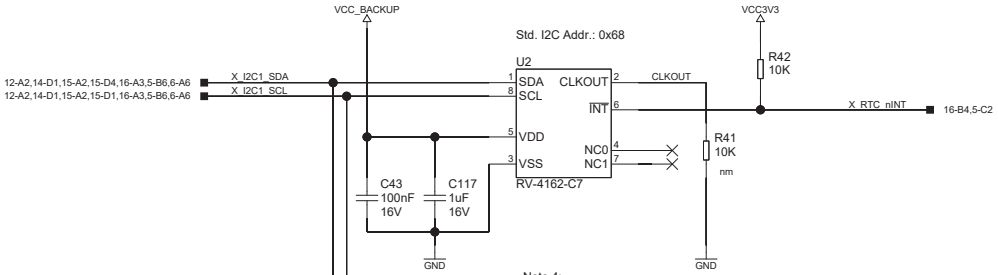
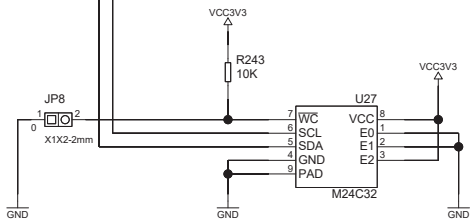
RTC



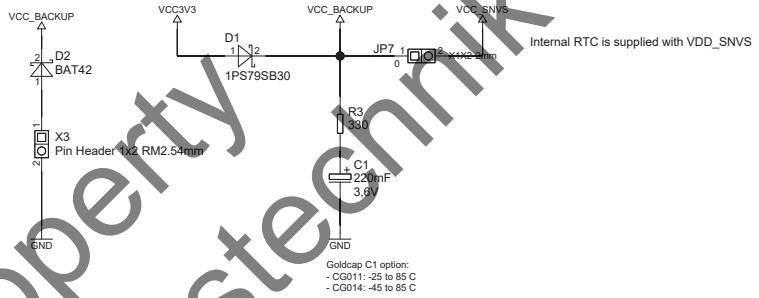
Note 4:
External RTC:
Current consumption during access: 35uA
Current consumption time keeping mode at 3V: 350nA
Timekeeping down to 1.0V

EEPROM



EEPROM I2C Addr.:
Address Memory Area: 0x54
Address ID Page: 0x5C

Goldcap

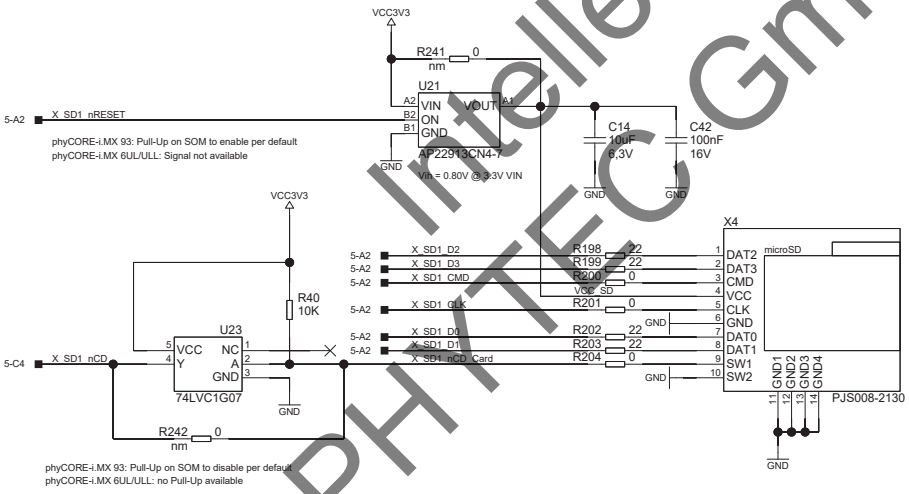


Note 5:
Internal RTC:
Current consumption time keeping mode at 3V: 500uA
Timekeeping down to 2.4V

BAT42: Forward current 2mA,
Forward Voltage 0.33V @ 25degree

1PS79SB30:
Forward Voltage 0.19V
at 0.1mA forward current

Micro SD Card



PCB Population SD-Card Interface phyCORE-SOMs		
Parts	phyCORE-i.MX 93	phyCORE-i.Mx 6UL/ULL
U21	populated	not mounted
R241	not mounted	populated
U23	populated	not mounted
R242	not mounted	populated

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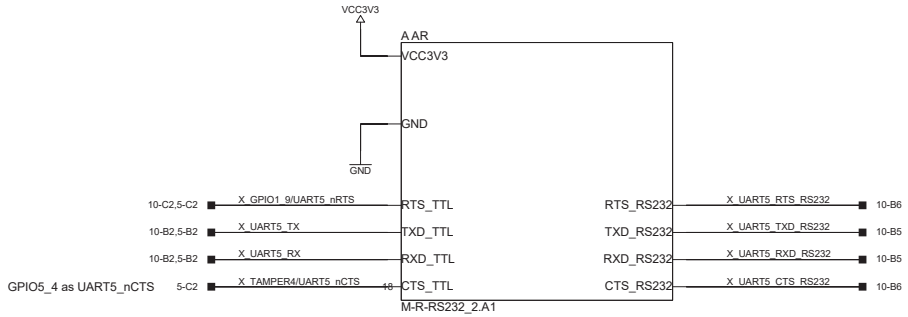
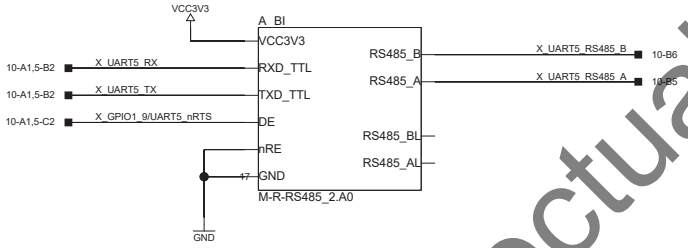
RS232

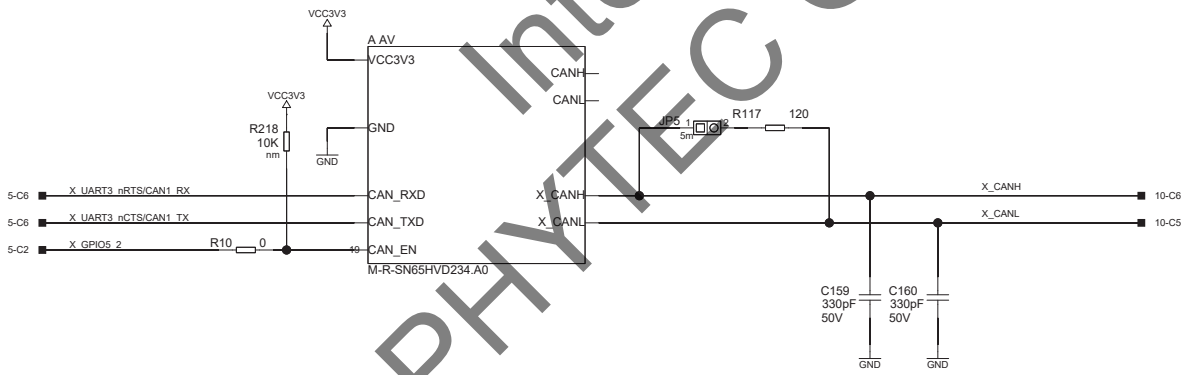


Note!: RS232 and RS485 are population options. You can only use one at a time!

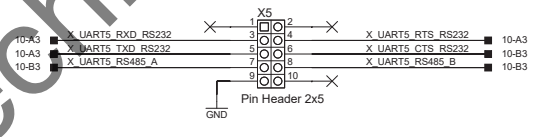
RS485



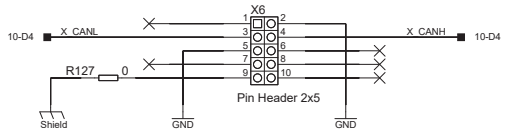
CAN



RS232/RS485 Pin Header



CAN Pin Header



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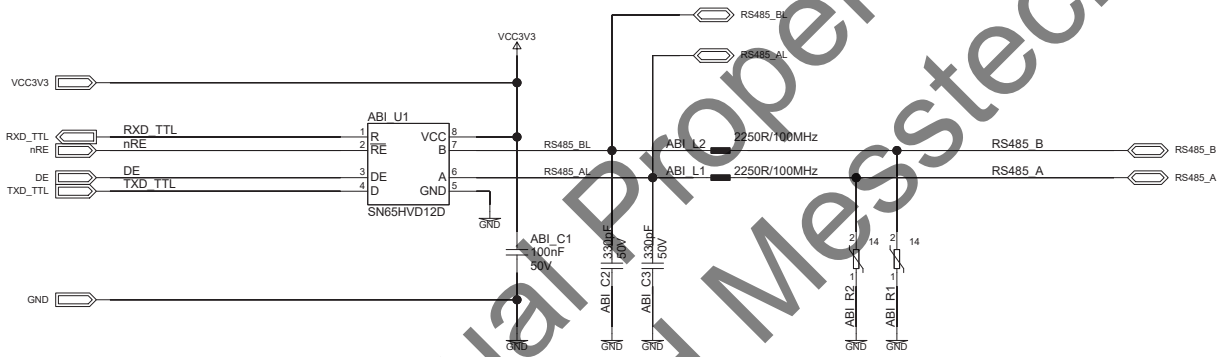
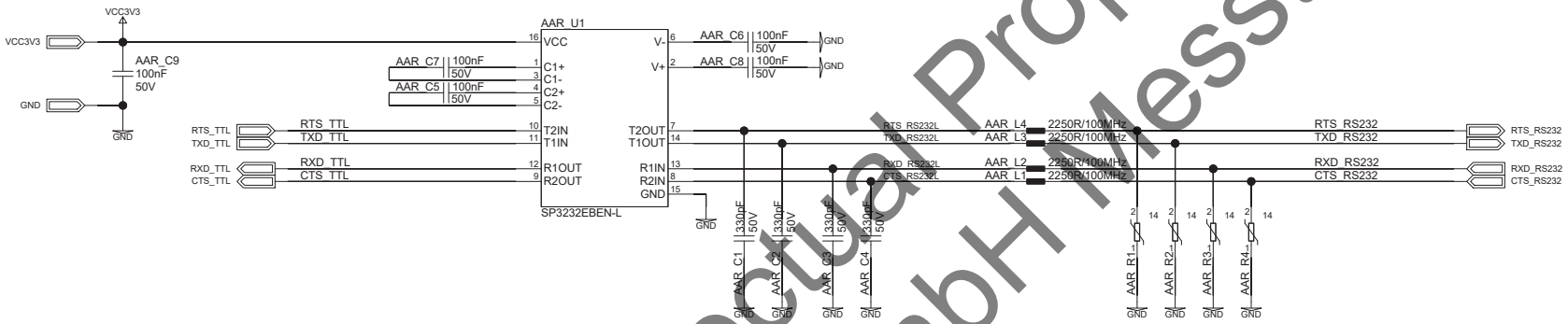
M-R-RS485_2



PHYTEC			PHYTEC Messtechnik GmbH Barcelona-Allee 1 D-55129 Mainz
Block Name: M-R-RS485_2		Block Prefix: BI	Department : F&E Author: T. Jacobus
23.06.2020	Makro: M-R-RS485_2.A0	Revision : 001	Sheet 11 of 19

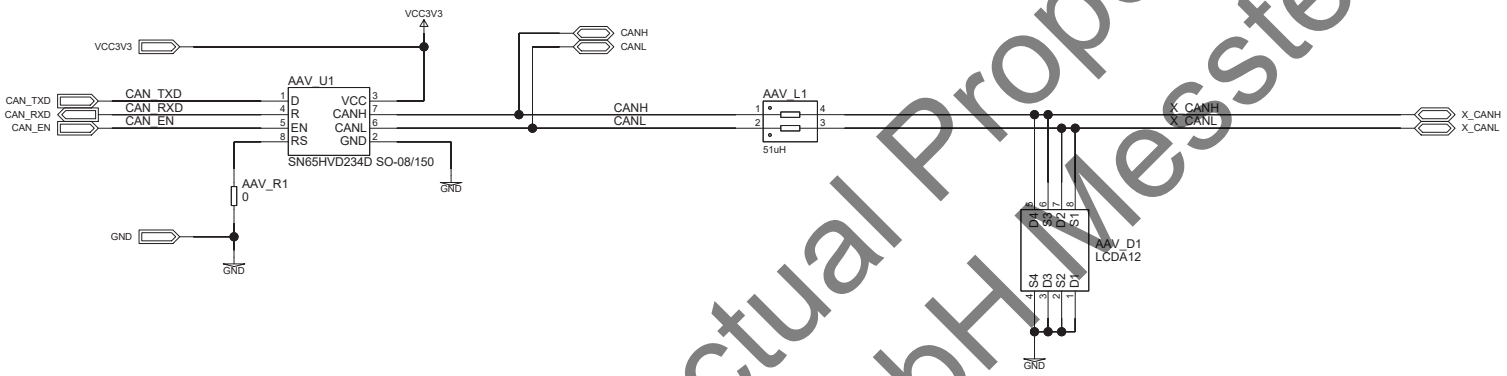
M-R-RS232_2

RS232 Transceiver



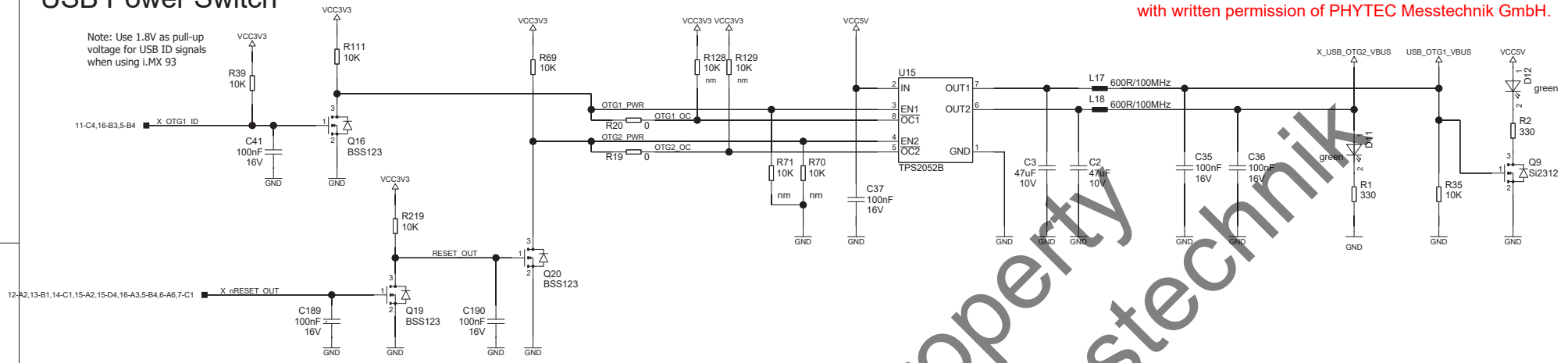
PHYTEC			PHYTEC Messtechnik GmbH Barcelona-Allee 1 D-55129 Mainz
Block Name: M-R-RS232_2	Block Prefix: AR		Department : F&E Author: T. Jacobus
06.03.2020	Makro: M-R-RS232_2.A2	Revision : 002	Sheet 12 of 19

M-R-SN65HVD234

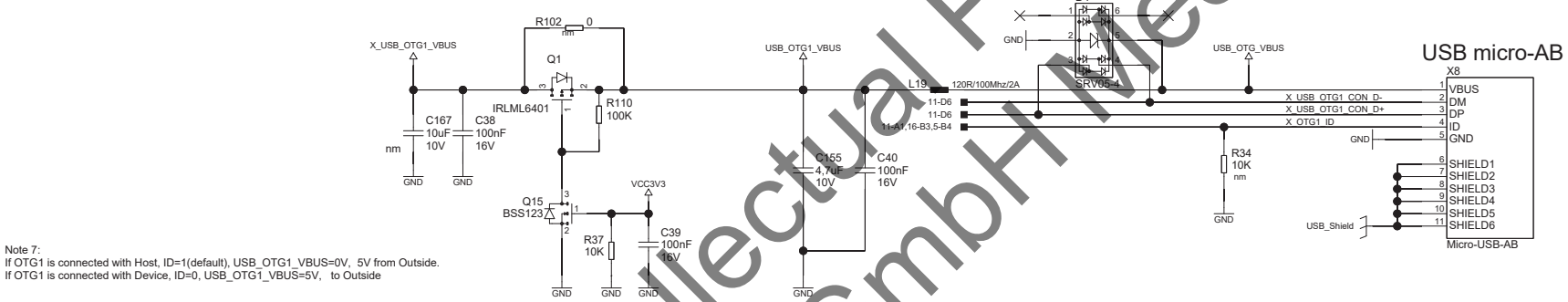


PHYTEC			PHYTEC Messtechnik GmbH Barcelona-Allee 1 D-55129 Mainz
Block Name: M-R-SN65HVD234		Block Prefix: AV	Department : F&E Author: T. Jacobus
16.04.2015	Makro: M-R-SN65HVD234.A0	Revision : 001	Sheet 13 of 19

USB Power Switch

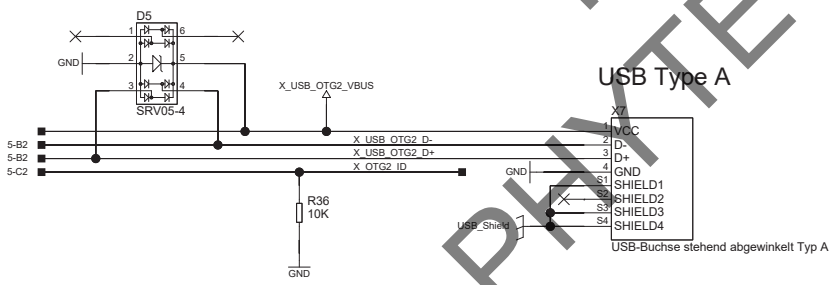


USB OTG1

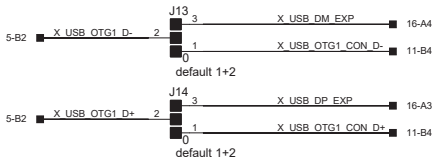


Note 7:
If OTG1 is connected with Host, ID=1(default), USB_OTG1_VBUS=0V, 5V from Outside.
If OTG1 is connected with Device, ID=0, USB_OTG1_VBUS=5V, to Outside

USB HOST



OTG1 Expansion Port Selection



Note 8:
USB_OTG1 on USB-OTG connector X8: J13+J14=1+2
USB_OTG1 on expansion connector X16: J13+J14=2+3

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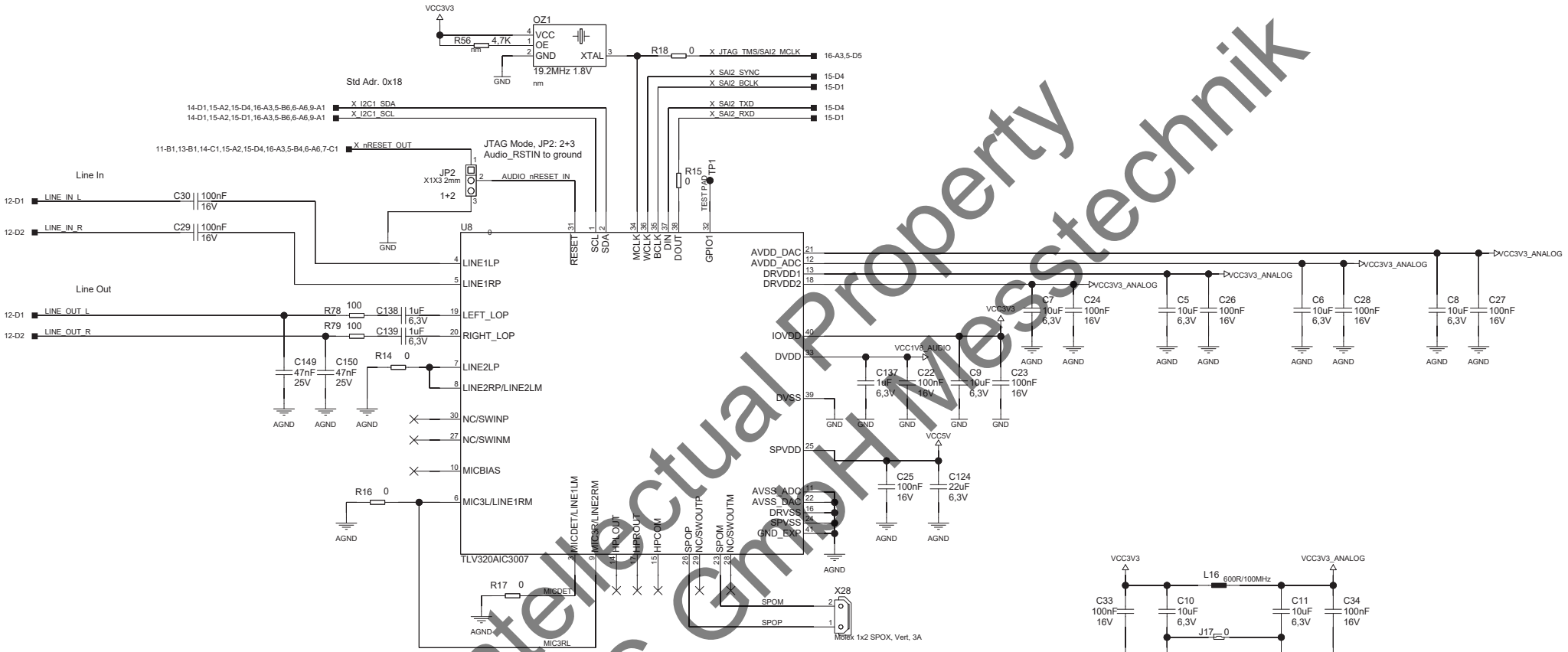
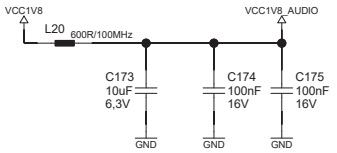
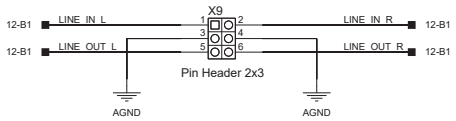
Audio Stereo Codec





Pin Header



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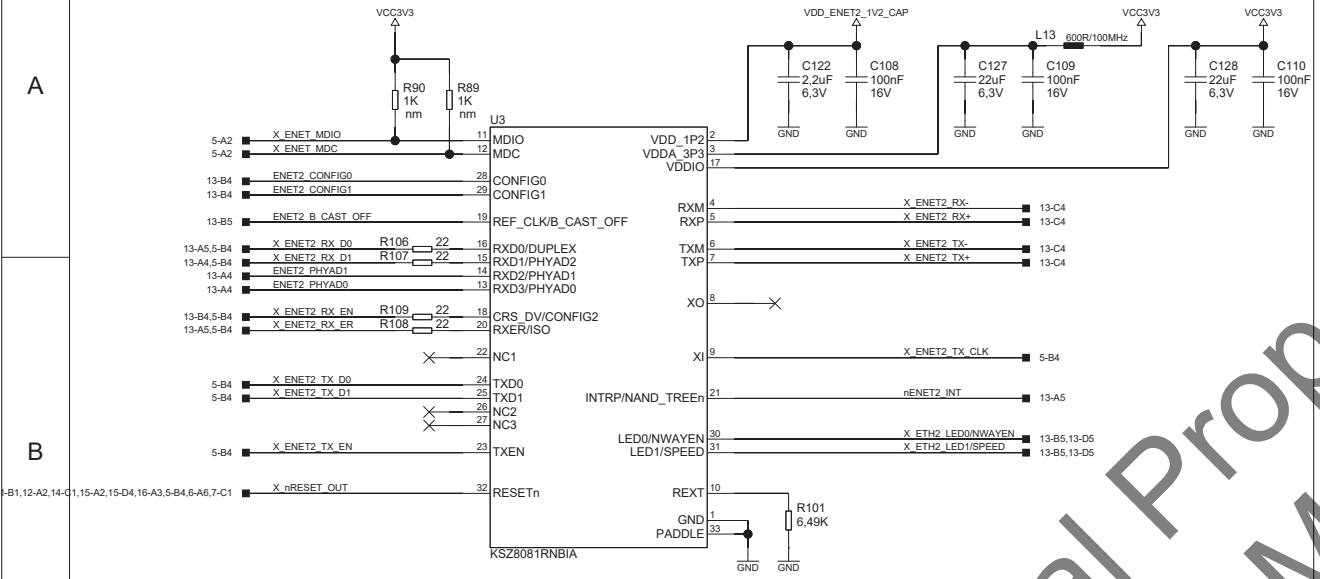
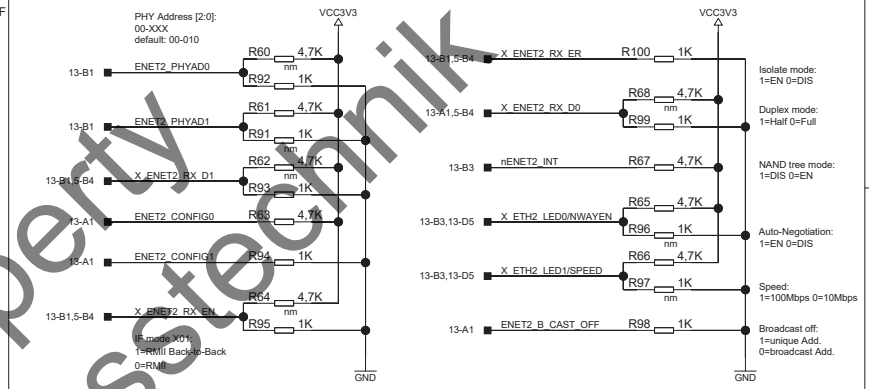
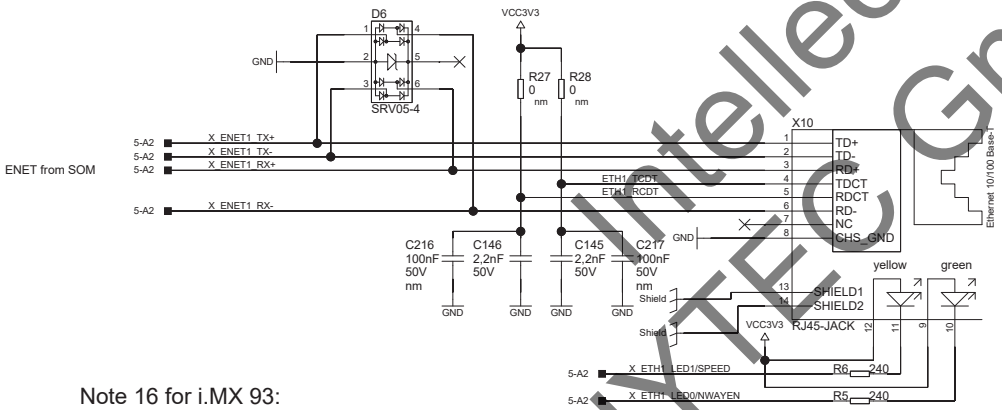
Ethernet 2 PHY (10/100Mbit)



ENET2 Configuration



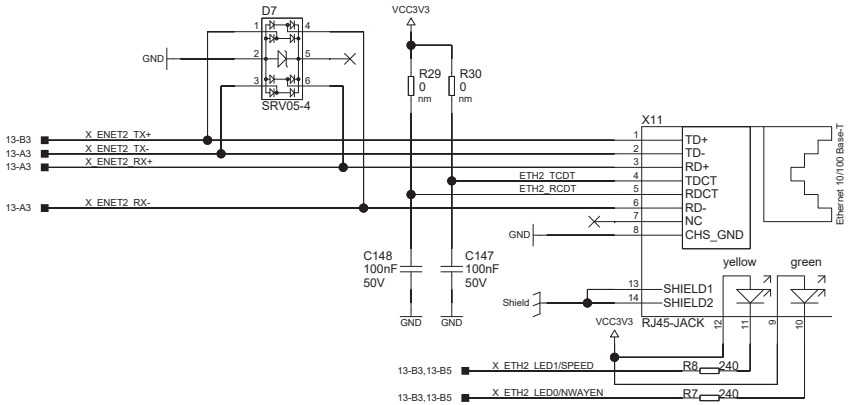
Ethernet 1 10/100Mbit RJ45



Note 16 for i.MX 93:
Please add MOSFET between ETH1&2 LED signal and and LEDs of RJ45 connector

Note 9:
RJ45 Connector:
Industrial (-40 to +85 C): VE309
Commercial (0 to 70 C): VE139

Ethernet 2 10/100Mbit RJ45



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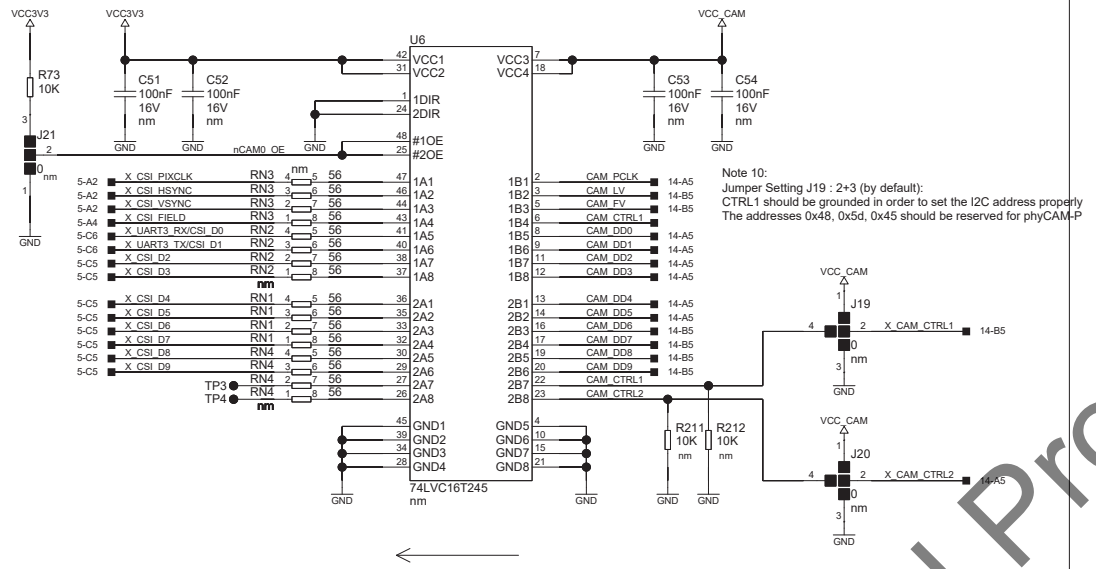
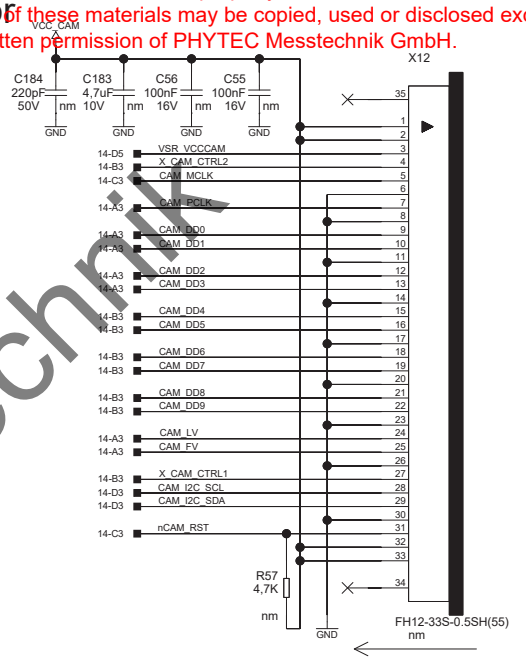
phyCAM-P(10 bit)

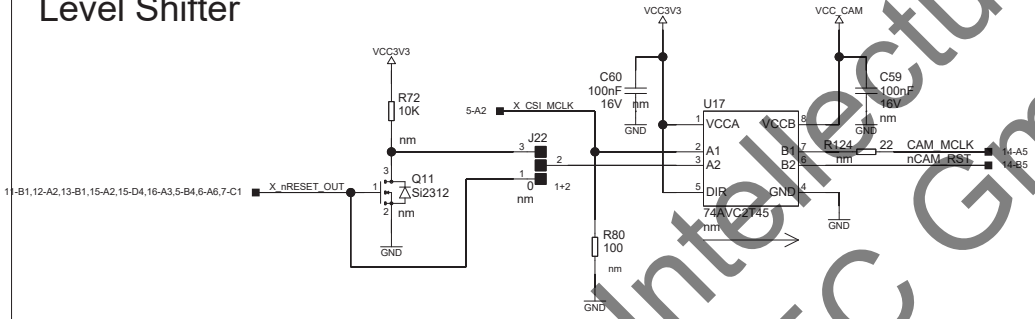


Note 10:
Jumper Setting J19 : 2+3 (by default):
CTRL1 should be grounded in order to set the I2C address properly
The addresses 0x48, 0x5d, 0x45 should be reserved for phyCAM-P

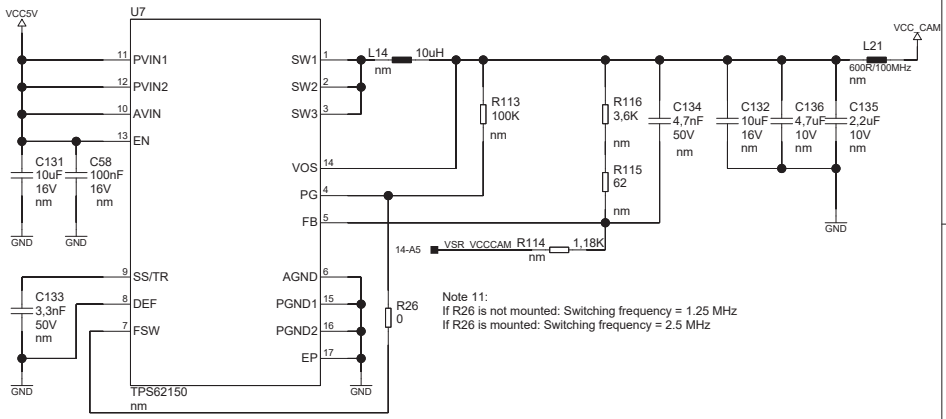
phyCAM-P Connector



Level Shifter

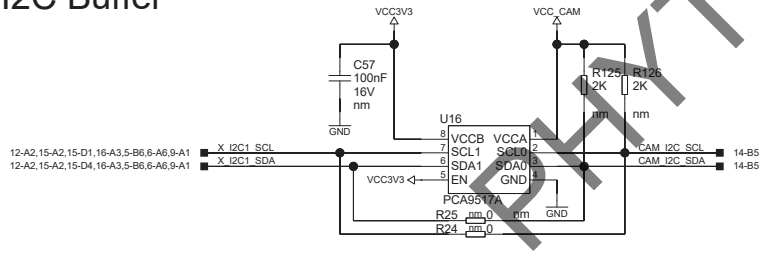


Camera Power Supply



Note 11:
If R26 is not mounted: Switching frequency = 1.25 MHz
If R26 is mounted: Switching frequency = 2.5 MHz

I2C Buffer



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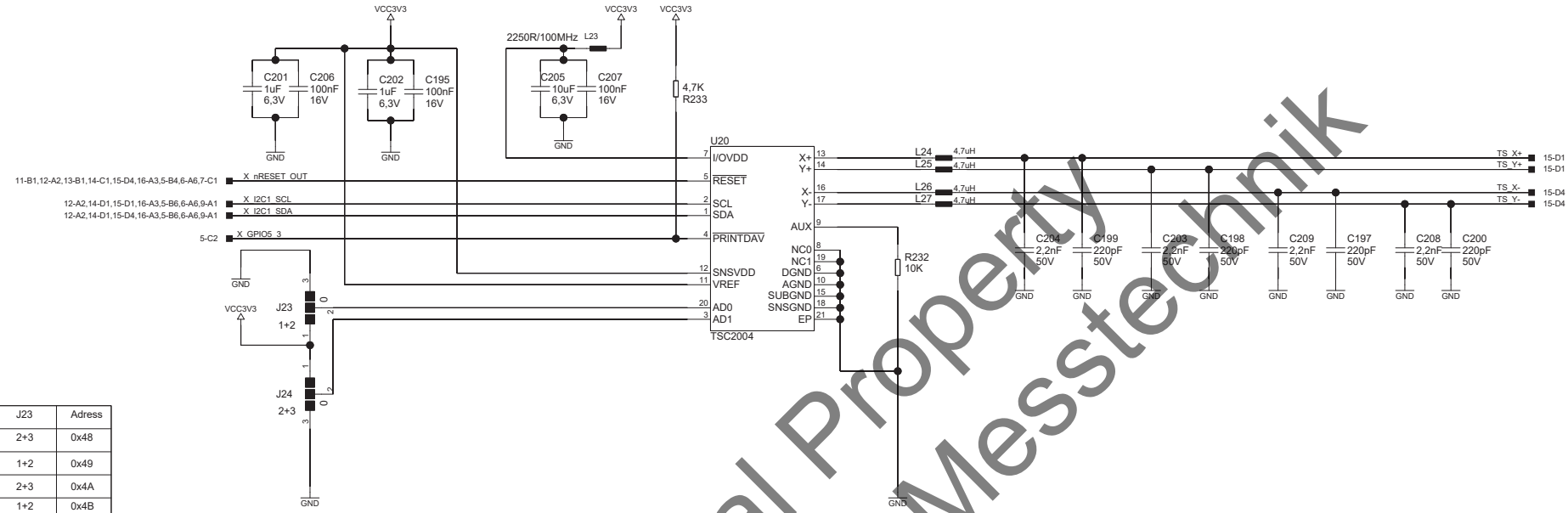
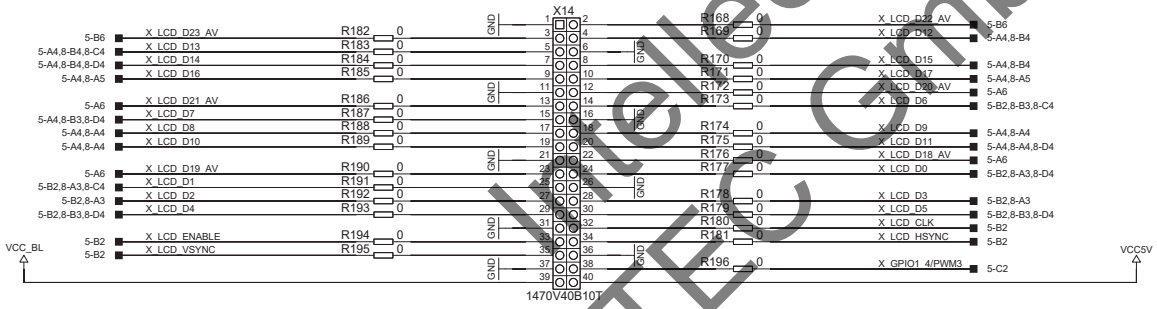
Resistive Touch Controller



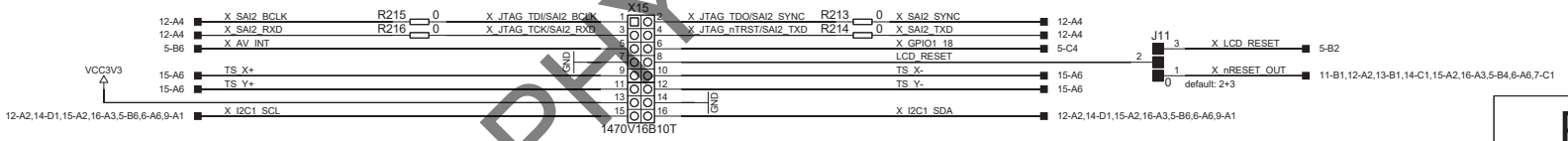
Default	J24	J23	Adress
	2+3	2+3	0x48
	2+3	1+2	0x49
	1+2	2+3	0x4A
	1+2	1+2	0x4B

Audio/Video Connector

Note 13:
Please place all the following resistors near the connector X1



Note 14:
If Audio Codec U8 is not populated,
the resistors from R213 to R216 should also not be mounted.



X17 Drill Hole 2.2mm/4.5mm GND
X18 Drill Hole 2.2mm/4.5mm GND

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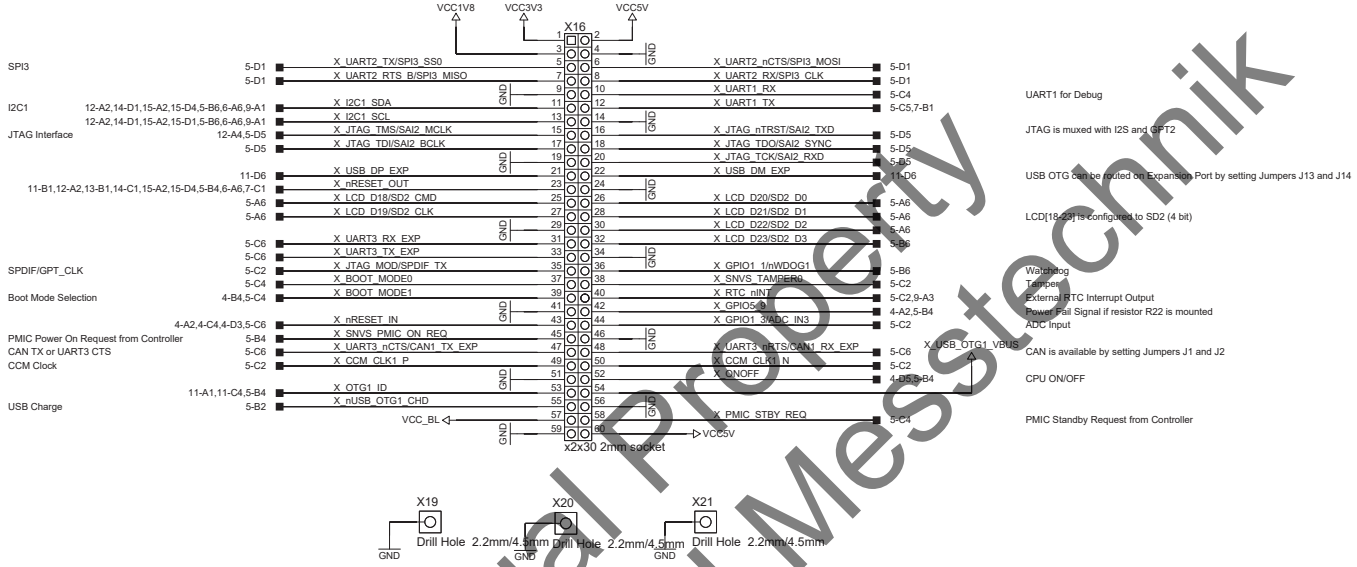
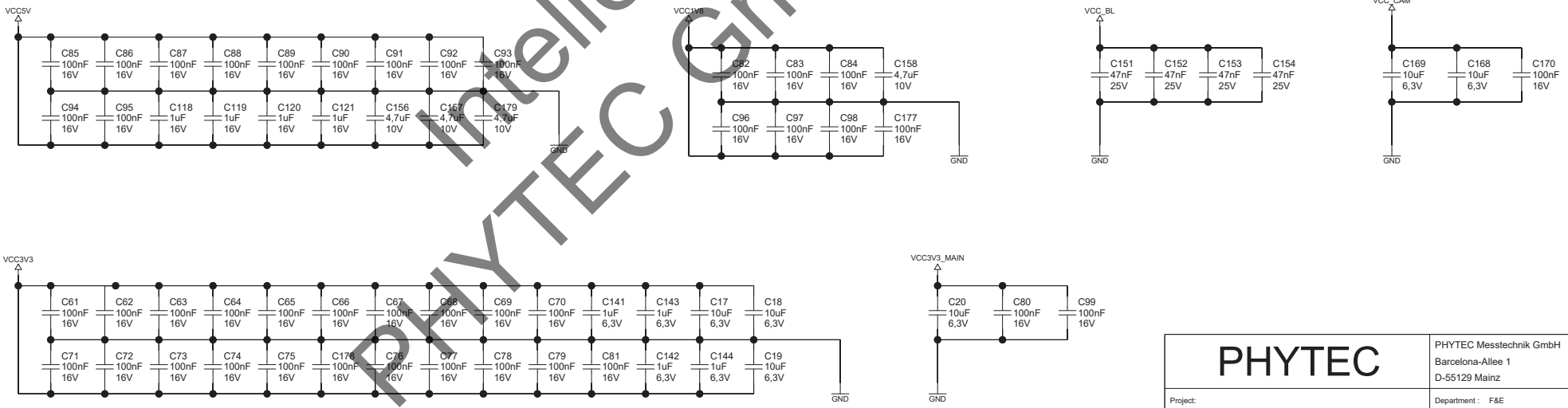
Expansion Connector



EMC Blocking



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