14 camera support

The phyFLEX-i.MX 6 - module offers many different ways to connect digital cameras.
The i.MX 6 controller has in the Dual- and Quad-core version two independent parallel camera ports and as an alternative one MIPI/CSI-2 receiver (Image 01).
Also have they two IPU 3H - Image Processing Units (version 3H) for separated processing of the two independent parallel cameras.

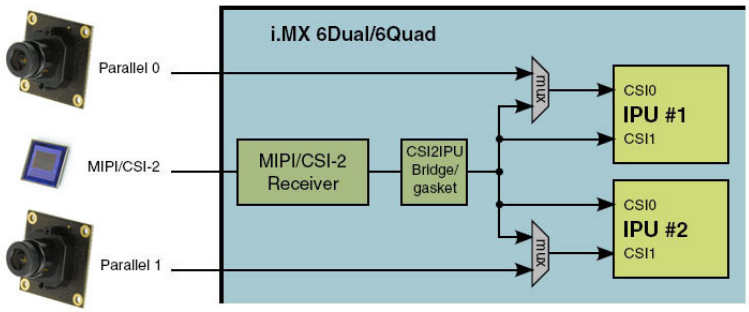

Image 01: Connection options of the cameras (i.MX6 Dual- and Quad-core)

The i.MX 6 controller has in the Solo- and DualLite-core version one parallel camera port and as an alternative one MIPI/CSI-2 receiver (Image 02).
They have one IPU 3H - Image Processing Unit (version 3H) for processing of one parallel camera.

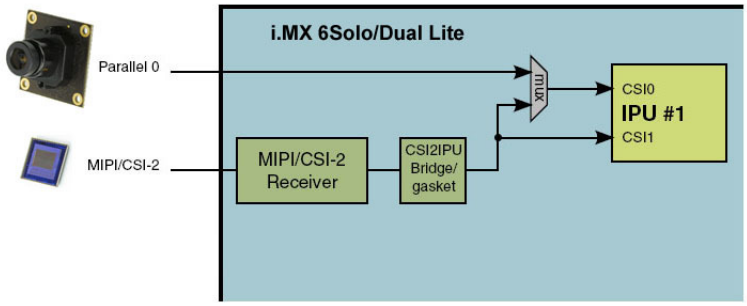

Image 02: Connection options of the cameras (i.MX6 Solo- and DualLite-core)

These 3(2) possible camera paths, are different routed on the PHYTEC phyFLEX-i.MX6 modul.
In combine with the reference circuits (on PHYTEC carrier-bord “PBA-B-01” and mapper-board “FLM-A-XL1”) can be connected all phyCAM-cameras or customers-cameras.

Parallel 0 (Camera_0 or also referred as CSI0)

The phyFLEX-i.MX 6 - module performs the "Parallel 0" (connect with CSI0 on IPU#1) path as "camera_0"- Ports out of module, than parallel interfaces (on connector 3) as well as serial LVDS interfaces (on connector 2).

On the application board can thus on "camera_0" either:

- camera moduls with phyCAM-S(+) interface (connection reference see PHYTEC carrier board PBA-B-01 "Camera_0, phyCAM-S+")

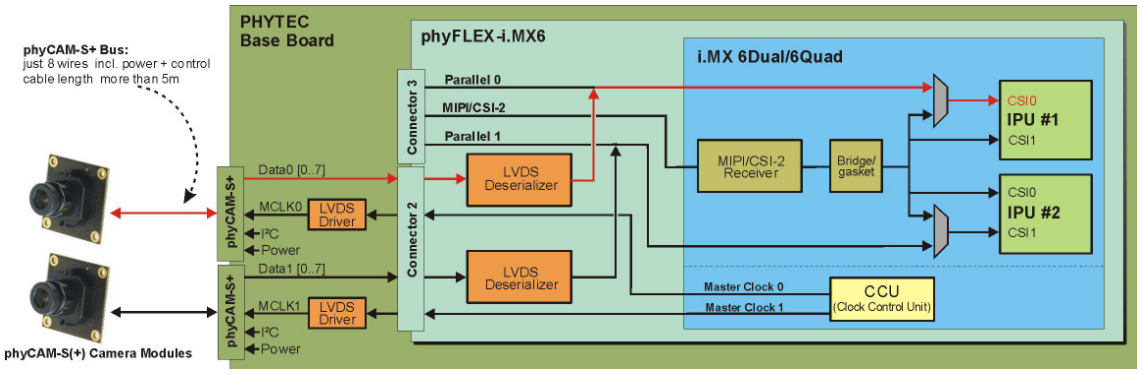

Image 03: Datapath Camera_0 to CSI0 (IPU#1) as phyCAM-S+

- camera modules with phyCAM-P interface (connection reference see PHYTEC mapper board FLM-A-XL1 "Camera_0, phyCAM-P")
- customer camera moduls with up to 18-Bit data parallel interface (connection reference see PHYTEC mapper board FLM-A-XL1 "Camera_0, Auxilary", Note: Please check position of jumper J8.)

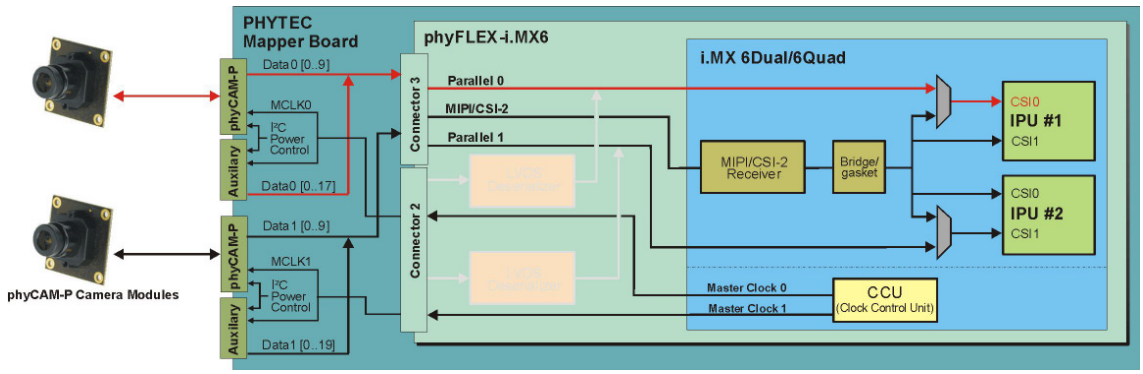

Image 04: Datapath Camera_0 to CSI0 (IPU#1) as phyCAM-P or customized

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Parallel 1 (Camera_1 or also referred as CSI1)

The phyFLEX-i.MX 6 - module performs the "Parallel 1" (connect with CSI1 on IPU#2) path as "camera_1"- Ports out of module, than parallel interfaces (on connector 3) as well as serial LVDS interfaces (on connector 2).
On the application board can thus on "camera_1" either:

- camera moduls with phyCAM-S(+) interface (connection reference see PHYTEC carrier board PBA-B-01 "Camera_1, phyCAM-S+")

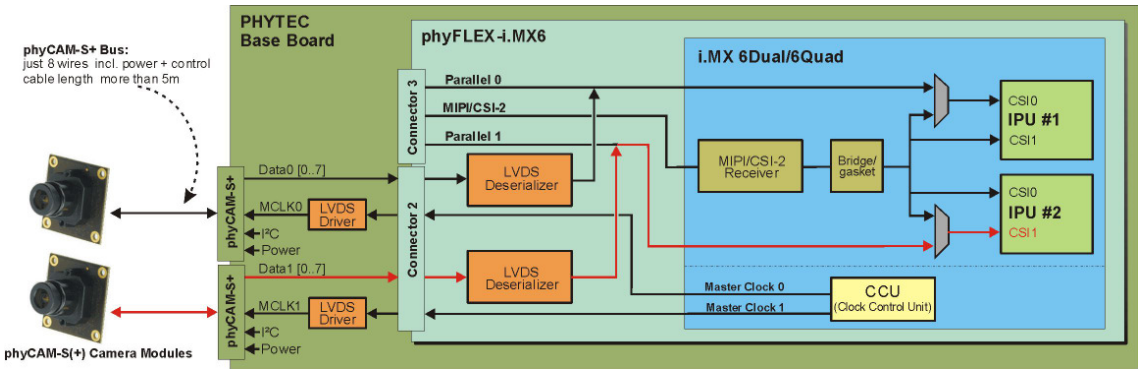

Image 05: Datapath Camera_1 to CSI1 (IPU#2) as phyCAM-S+

- camera modules with phyCAM-P interface (connection reference see PHYTEC mapper board FLM-A-XL1 "Camera_1, phyCAM-P")
- customer camera moduls with up to 20-Bit data parallel interface (connection reference see PHYTEC mapper board FLM-A-XL1 "Camera_1, Auxilary", Note: Please check position of jumper J11.)

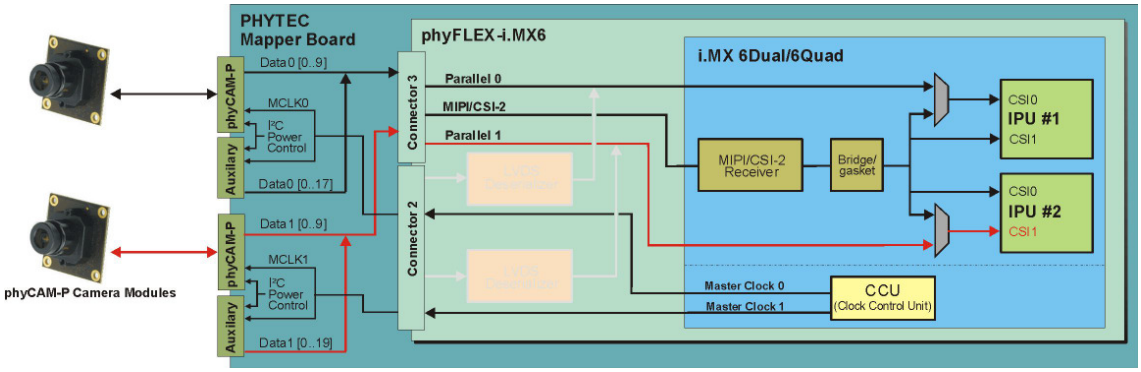

Image 06: Datapath Camera_1 to CSI1 (IPU#2) as phyCAM-P or customized

MIPI/CSI-2 (Camera_2)

The MIPI CSI-2 camera interface is also performs out of modul. This can alternative used for the connection of camera sensors with MIPI/CSI-2 Interface.

Please note:

- For each channel Camera_0/Camera_1 can either only phyCAM-P or only phyCAM-S+ interface can be used. The selection phyCAM-P / phyCAM-S+ are made in the config file.
- Some assembly options of the module does not allow, all input configurations for the camera interface.
- Reference PHYTEC camera moduls with phyCAM-P and S(+) - interface to be used (see phyCAM-P/-S manual L-748).
- PHYTEC mapper board FLM-A-XL1 is not in all kit available.
- The signals of the CSI-2 (MIPI) interface connectors are placed on the Camera_2 connector of the mapper. By using the CSI-2 - interfaces depending on the configuration, the respective parallel CSI0/1 channels are occupied.

14.1 Camera_0 interface (CSI0 on IPU#1)

14.1.1 Camera_0 as parallel interface

When all module connector are present, is the parallel Camera_0 interface connect to CSI0 (IPU#1) with 18-data-bits on the X3 module connector available.
Note: The "CSI0_DATA_EN" - pad (U27) controls the Camera_0 LVDS deserializer. For use of a parallel camera source on CSI0 (IPU#1), this signal must be turned off.

The following table shows the location of CSI0 (IPU#1) camera signals at phyFLEX-connector:

Pin #	Signal	ST	Voltage Domain	Description
X3A23	X_CSI0_DAT19	I	VDD_3V3_LOGIC	Camera0 D19
X3A22	X_CSI0_DAT18	I	VDD_3V3_LOGIC	Camera0 D18

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X3A21	X_CSI0_DAT17	I	VDD_3V3_LOGIC	Camera0 D17
X3A20	X_CSI0_DAT16	I	VDD_3V3_LOGIC	Camera0 D16
X3A19	X_CSI0_DAT15	I	VDD_3V3_LOGIC	Camera0 D15
X3A17	X_CSI0_DAT14	I	VDD_3V3_LOGIC	Camera0 D14
X3A16	X_CSI0_DAT13	I	VDD_3V3_LOGIC	Camera0 D13
X3A15	X_CSI0_DAT12	I	VDD_3V3_LOGIC	Camera0 D12
X3A9	X_CSI0_DAT11	I	VDD_3V3_LOGIC	Camera0 D11
X3A3	X_CSI0_DAT10	I	VDD_3V3_LOGIC	Camera0 D10
X3B24	X_CSI0_DAT9	I	VDD_3V3_LOGIC	Camera0 D9
X3B28	X_CSI0_DAT8	I	VDD_3V3_LOGIC	Camera0 D8
X3B40	X_CSI0_DAT7	I	VDD_3V3_LOGIC	Camera0 D7
X3B41	X_CSI0_DAT6	I	VDD_3V3_LOGIC	Camera0 D6
X3B18	X_CSI0_DAT5	I	VDD_3V3_LOGIC	Camera0 D5
X3B12	X_CSI0_DAT4	I	VDD_3V3_LOGIC	Camera0 D4
X1A14	X_UART1_RTS	I	VDD_3V3_LOGIC	Camera0 D3
X1A15	X_UART1_CTS	I	VDD_3V3_LOGIC	Camera0 D2
X3A25	X_CSI0_MCLK	I	VDD_3V3_LOGIC	Camera0 HSYNC
X3A27	X_CSI0_VSYNC	I	VDD_3V3_LOGIC	Camera0 VSYNC
X3A26	X_CSI0_PIXCLK	I	VDD_3V3_LOGIC	Camera0 PCLK
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera0 MCLK

Table xx: CSI0 (IPU#1) as parallel interface signal location at phyFLEX connector

Together with an I²C bus, can a camera module which a CMOS camera-interface has, be connected in a simple manner.
On the mapper-board (Note: Not in all kit available) "FLM-A-XL1" is the parallel port Camera_0 as phyCAM-P (up to 12 data-bits) camera-interfaces to lead out. Furthermore is the parallel ports with 18-data-bits lead out. Note: Please check position of jumper J8.

14.1.2 Camera_0 as LVDS (phyCAM-S+)

On the X2 module connector is the Camera_0 interface as LVDS-Signal available.
The phyFLEX-i.MX 6 uses one 1-channel 10-Bit LVDS random lock deserializer (U27), to receive LVDS-signals from a LVDS camera interface. The LVDS deserializer converts the LVDS Signals to a 10-bit wide parallel data bus and separate clock which can be used as inputs for

the i.MX 6 camera sensor interfaces connected to CSI0 (IPU#1). The 10-bit wide data bus consists of 8 data bits and 2 sync bits (HSYNC/VSYNC). Note: The deserializer needs the same clock frequency, as the source-serializer on the camera.

The following table shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X2A40	X_CAMERA0_L0+	LVDS_I	VDD_3V3_LOGIC	Camera0 data+
X2A41	X_CAMERA0_L0-	LVDS_I	VDD_3V3_LOGIC	Camera0 data-
X2A43	X_CAMERA0_CLK	O	VDD_3V3_LOGIC	Camera0 master clock
X2A44	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera0 reference voltage

Table xx: CSI0 (IPU#1) as LVDS interface signal location at phyFLEX connector

In combination with an I²C-bus and the master-clock-seralizer on the main board, this represents the phyCAM-S+ interface.

The “CSI0_DATA_EN” pad (U27) enabled the CSI0 (IPU#1) LVDS-deserializer. For use a serial source at Camera_0 this signal must be on. For use a parallel source at Camera_0 from the modul connector this signal must be off.
To assists the implementation of a power management the Camera_0 deserializer “CAM_LVDS_PRWDN/GPIO1” pad (U27) can used.

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14.2 Camera_1 interface (CSI1 on IPU#2)

14.2.1 Camera_1 as parallel interface

When all module connector are present, is the parallel Camera_1 interface connect to CSI1 (IPU#2) with 20-data-bits on the X3 module connector available.
Note: The " X_EIM_DA10" - pad (U12) controls the Camera_1 LVDS deserializer. For use of a parallel camera source on CSI1 (IPU#2), this signal must be turned off.

The following table shows the location of CSI1 (IPU#2) camera signals at phyFLEX-connector:

Pin #	Signal	ST	Voltage Domain	Description
X3A32	X_EIM_A24	I	VDD_3V3_LOGIC	Camera1 D19
X3A33	X_EIM_A23	I	VDD_3V3_LOGIC	Camera1 D18
X3A34	X_EIM_A22	I	VDD_3V3_LOGIC	Camera1 D17
X3A35	X_EIM_A21	I	VDD_3V3_LOGIC	Camera1 D16
X3A37	X_EIM_A20	I	VDD_3V3_LOGIC	Camera1 D15
X3A38	X_EIM_A19	I	VDD_3V3_LOGIC	Camera1 D14
X3A39	X_EIM_A18	I	VDD_3V3_LOGIC	Camera1 D13
X3A40	X_EIM_A17	I	VDD_3V3_LOGIC	Camera1 D12
X3A41	X_EIM_EB0	I	VDD_3V3_LOGIC	Camera1 D11
X3A43	X_EIM_EB1	I	VDD_3V3_LOGIC	Camera1 D10
X3A44	X_EIM_DA0	I	VDD_3V3_LOGIC	Camera1 D9
X3A45	X_EIM_DA1	I	VDD_3V3_LOGIC	Camera1 D8
X3A46	X_EIM_DA2	I	VDD_3V3_LOGIC	Camera1 D7
X3A47	X_EIM_DA3	I	VDD_3V3_LOGIC	Camera1 D6
X3A49	X_EIM_DA4	I	VDD_3V3_LOGIC	Camera1 D5
X3A50	X_EIM_DA5	I	VDD_3V3_LOGIC	Camera1 D4
X3A51	X_EIM_DA6	I	VDD_3V3_LOGIC	Camera1 D3
X3A52	X_EIM_DA7	I	VDD_3V3_LOGIC	Camera1 D2
X3A53	X_EIM_DA8	I	VDD_3V3_LOGIC	Camera1 D1
X3A55	X_EIM_DA9	I	VDD_3V3_LOGIC	Camera1 D0
X3A57	X_EIM_DA11	I	VDD_3V3_LOGIC	Camera1 HSYNC
X3A58	X_EIM_DA12	I	VDD_3V3_LOGIC	Camera1 VSYNC
X3A59	X_EIM_A16	I	VDD_3V3_LOGIC	Camera1 PCLK
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera1 MCLK

Table xx: CSI1 (IPU#2) as parallel interface signal location at phyFLEX connector

Together with an I²C bus, can a camera module which a CMOS camera-interface has, be connected in a simple manner.
On the mapper-board (Note: Not in all kit available) "FLM-A-XL1" is the parallel port Camera_1 as phyCAM-P (up to 12 data-bits) camera-interfaces to lead out. Furthermore is the parallel ports with 20-data-bits lead out. Note: Please check position of jumper J11.

14.2.2 Camera_1 as LVDS (phyCAM-S+)

On the X2 module connector is the Camera_0 interface as LVDS-Signal available.
The phyFLEX-i.MX 6 uses one 1-channel 10-Bit LVDS random lock deserializer (U12), to receive LVDS-signals from a LVDS camera interface. The LVDS deserializer converts the LVDS Signals to a 10-bit wide parallel data bus and separate clock which can be used as inputs for the i.MX 6 camera sensor interfaces connected to CSI1 (IPU#2). The 10-bit wide data bus consists of 8 data bits and 2 sync bits (HSYNC/VSYNC). Note: The deserializer needs the same clock frequency, as the source-serializer on the camera.

The following table shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X2A46	X_CAMERA1_L0+	LVDS_I	VDD_3V3_LOGIC	Camera1 data+
X2A47	X_CAMERA1_L0-	LVDS_I	VDD_3V3_LOGIC	Camera1 data-
X2A49	X_CAMERA1_CLK	O	VDD_3V3_LOGIC	Camera1 master clock
X2A50	reference-voltage	REF_O	VDD_3V3_LOGIC	Camera1 reference voltage

Table xx: CSI1 (IPU#2) as LVDS interface signal location at phyFLEX connector

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In combination with an I²C-bus and the master-clock-seralizer on the main board, this represents a phyCAM-S+ interface.

The “X_EIM_DA10” pad (U12) enabled the Camera_1 LVDS-deserializer. For use a serial source at Camera_1 this signal must be on. For use a parallel source at CSI1 (IPU#2) from the modul connector this signal must be off.
To assists the implementation of a power management the Camera_1 deserializer “X_EIM_EB0” pad (U12) can used.

14.3 Camera_2 interface MIPI/CSI-2

On the X3 module connector is the MIPI/CSI-2 camera interface with up to 4 data-lanes and one clock-lane available.

The following table shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X3A1	X_CSI_CLK0P	LVDS_I	i.MX6 internal	MIPI/CSI-2 clk+
X3A2	X_CSI_CLK0M	LVDS_I	i.MX6 internal	MIPI/CSI-2 clk-
X3A4	X_CSI_D0P	LVDS_I	i.MX6 internal	MIPI/CSI-2 data0+
X3A5	X_CSI_D0M	LVDS_I	i.MX6 internal	MIPI/CSI-2 data0-
X3A7	X_CSI_D1P	LVDS_I	i.MX6 internal	MIPI/CSI-2 data1+
X3A8	X_CSI_D1M	LVDS_I	i.MX6 internal	MIPI/CSI-2 data1-
X3A10	X_CSI_D2P	LVDS_I	i.MX6 internal	MIPI/CSI-2 data2+
X3A11	X_CSI_D2M	LVDS_I	i.MX6 internal	MIPI/CSI-2 data2-
X3A13	X_CSI_D3P	LVDS_I	i.MX6 internal	MIPI/CSI-2 data3+
X3A14	X_CSI_D3M	LVDS_I	i.MX6 internal	MIPI/CSI-2 data3-

Table xx: MIPI/CSI-2 signal location at phyFLEX connector

Together with an I²C bus, and a camera-clock can a MIPI/CSI-2 camera module be connected.
On the mapper-board (Note: Not in all kit available) "FLM-A-XL1" is the MIPI/CSI-2 interface (Camera_2) to lead out on a connector.

Note: When using the optional MIPI/CSI-2 interface have these effects of using parallel interface.