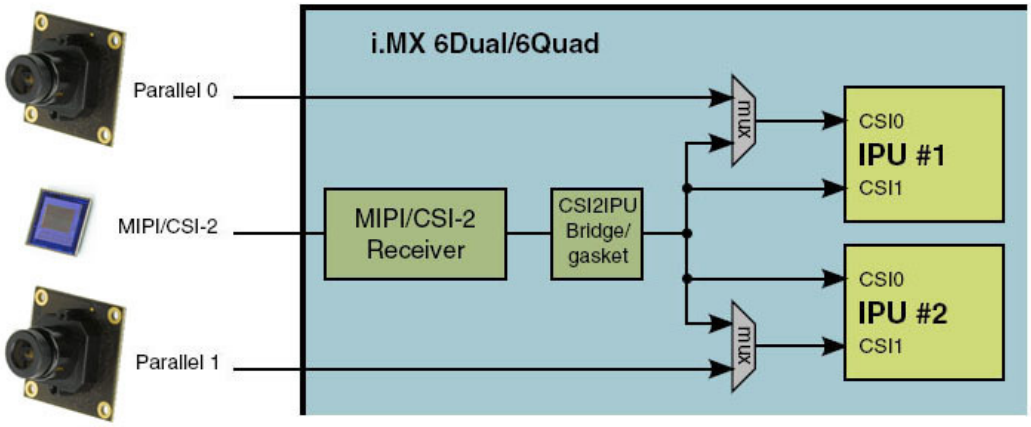
14 Camera Support

The phyCORE-i.MX 6 SOM offers various interfaces to connect digital cameras. Up to two parallel camera interfaces (CSI0 and CSI1[1]) as well as the interface to the MIPI/CSI-2 Host Controller are supported and brought out in different ways.

The i.MX 6 microcontroller is equipped with one or two image processing units (version 3H) (IPU #1 and IPU #2[1]) to process the signals from the parallel, or the MIPI camera interface.

Specifically, the i.MX 6 (Solo), and i.MX 6 (DualLite) have one parallel camera port (CSI0), and alternatively, one MIPI/CSI-2 interface, while the i.MX 6D (dual core), and i.MX 6Q (quad core) have an additional parallel camera port (CSI1) and a second image processing unit (IPU #2)(see *Figure 1* and Figure 2). The two IPUs allow operating two cameras independently.



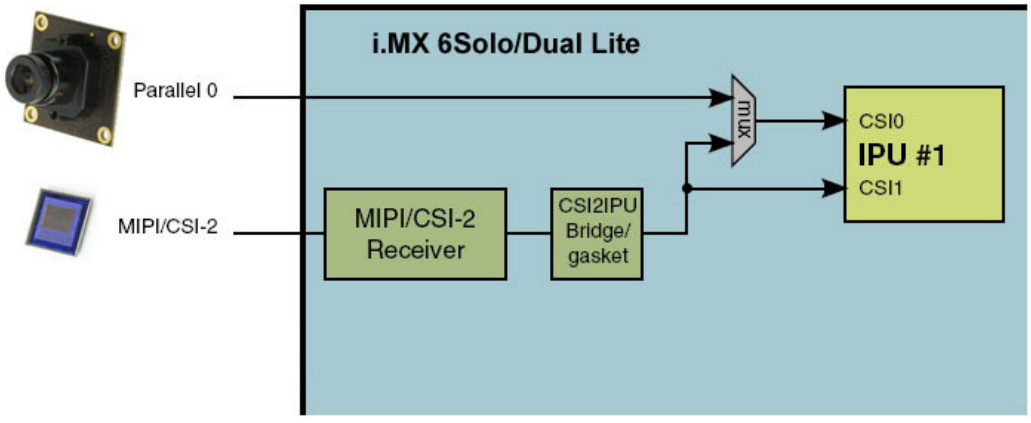


Figure 1: Camera Connectivity of the i.MX 6 (Solo/DualLite)

[1]: only i.MX 6 with Dual-. or Quad core. i.MX 6 with Solo-, or DualLite core provide only one parallel camera interface and one IPU.

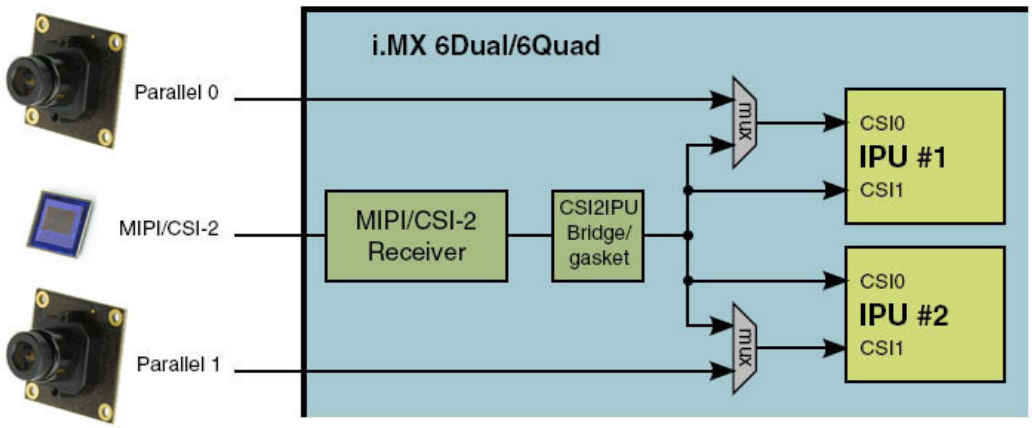


Figure 2: Camera Connectivity of the i.MX 6 (dual core/quad core)

The phyCORE-i.MX 6 SOM provides the camera interfaces as parallel interfaces. So on the connector X1 the two parallel interfaces and the MIPI Interface are available. (see Fig3) Parallel_0 is with 16-data-bits, HSYNC, VSYNC and PIXCLK available. Parallel_1 is with 20-data-bits, HSYNC, VSYNC and PIXCLK available. And the MIPI Interface is with 5-lanes available.

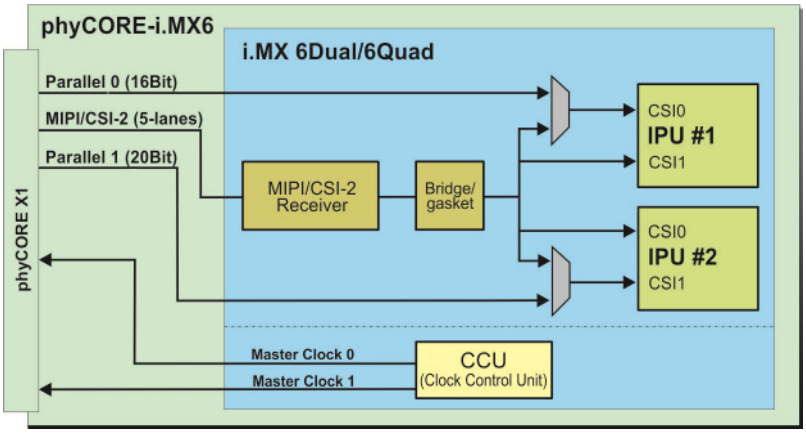
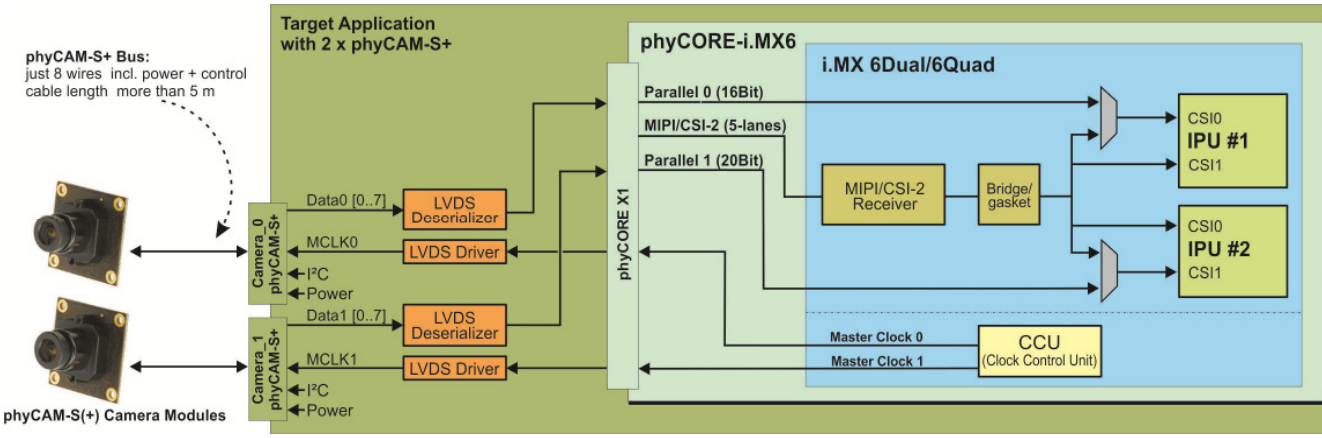


Figure 3:



On the PHYTEC or customer carrier boards can the interfaces are led out as phyCAM-P (or raw-parallel) see Fig4 and/or phyCAM-S+ see Fig5, or MIPI/CSI 2 interface.

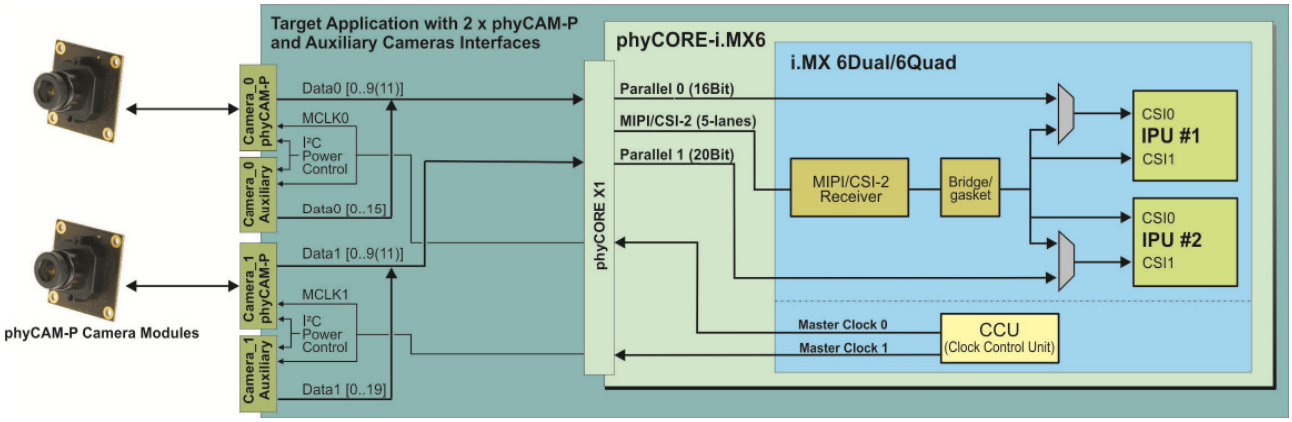


Figure 4: Use of Camera_0 (CSI0 of IPU#1) and Camera_1 (CSI1 of IPU#2) as phyCAM-P interface

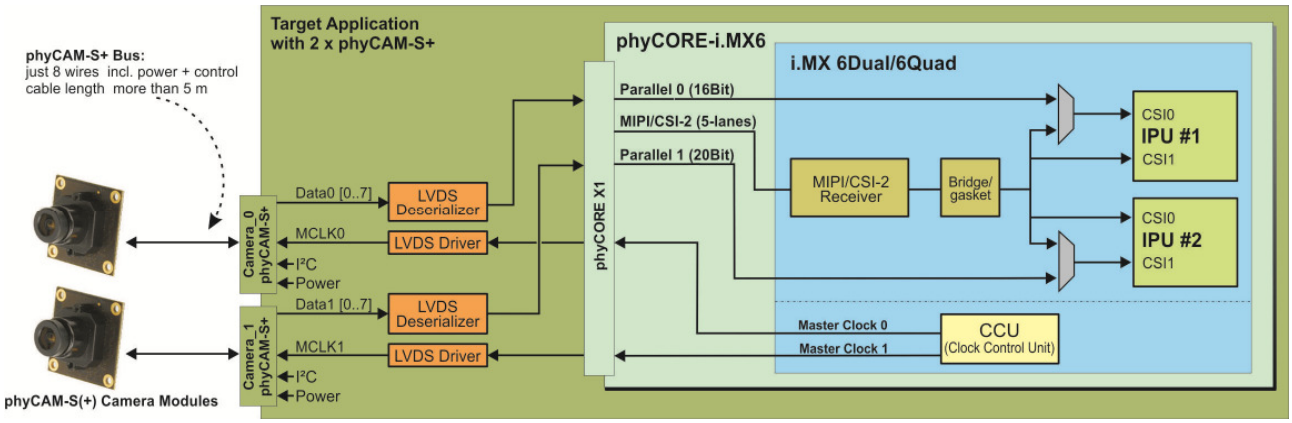


Figure 5: Use of Camera_0 (CSI0 of IPU#1) and Camera_1 (CSI1 of IPU#2) as phyCAM-S+ interface

Please refer to section *14.3.1* for more information on how to connect a camera to the PHYTEC carrier board "MIRA" using the different interface options.

14.1 Parallel Camera_0 Interface (CSI0 of IPU#1)

When the software multiplexing is correct initializing, is the parallel camera interface CSI0 with 16-data-bits available.

The following table shows the location of CSI0 camera signals at phyCORE-connector:

Pin #	Signal	ST	Voltage Domain	Description
X1D40	X_CSI0_DAT19	I	VDD_3V3_LOGIC	Camera0 D19
X1C45	X_CSI0_DAT18	I	VDD_3V3_LOGIC	Camera0 D18
X1D41	X_CSI0_DAT17	I	VDD_3V3_LOGIC	Camera0 D17
X1C46	X_CSI0_DAT16	I	VDD_3V3_LOGIC	Camera0 D16
X1D43	X_CSI0_DAT15	I	VDD_3V3_LOGIC	Camera0 D15
X1C47	X_CSI0_DAT14	I	VDD_3V3_LOGIC	Camera0 D14
X1D44	X_CSI0_DAT13	I	VDD_3V3_LOGIC	Camera0 D13
X1C49	X_CSI0_DAT12	I	VDD_3V3_LOGIC	Camera0 D12
X1D45	X_CSI0_DAT11	I	VDD_3V3_LOGIC	Camera0 D11
X1C50	X_CSI0_DAT10	I	VDD_3V3_LOGIC	Camera0 D10
X1D46	X_CSI0_DAT9	I	VDD_3V3_LOGIC	Camera0 D9
X1C51	X_CSI0_DAT8	I	VDD_3V3_LOGIC	Camera0 D8
X1D47	X_CSI0_DAT7	I	VDD_3V3_LOGIC	Camera0 D7
X1C52	X_CSI0_DAT6	I	VDD_3V3_LOGIC	Camera0 D6
X1C53	X_CSI0_DAT5	I	VDD_3V3_LOGIC	Camera0 D5
X1C55	X_CSI0_DAT4	I	VDD_3V3_LOGIC	Camera0 D4
X1D51	X_CSI0_HSYNC	I	VDD_3V3_LOGIC	Camera0 HSYNC
X1D48	X_CSI0_VSYNC	I	VDD_3V3_LOGIC	Camera0 VSYNC
X1C56	X_CSI0_PIXCLK	I	VDD_3V3_LOGIC	Camera0 PCLK
X1D16	X_CCM_CLKO1	O	VDD_3V3_LOGIC	Camera0 MCLK
Optional signals can use with camera ports.				
X1B23	X_I2C1_SCL	O	VDD_3V3_LOGIC	I²C1_SCL for camera control
X1B24	X_I2C1_SDA	I/O	VDD_3V3_LOGIC	I²C1_SDA for camera control
X1D50	X_CSI0_DATA_EN	O	VDD_3V3_LOGIC	e.g. switcher for phyCAM-P or phyCAM-S+ components
X1A38	X_CSI1_DATA00	O	VDD_3V3_LOGIC	e.g. switcher for phyCAM-P or phyCAM-S+ components

Table 1: CSI0 as parallel interface signal location at phyCORE connector

Together with an I²C bus, can a camera module which a CMOS camera-interface has, be connected in a simple manner. For example as phyCAM-P or phyCAM-S+ interface.
On the PHYTEC “MIRA” base-board "PBA-C-06" is the parallel Camera_0 interface converting in phyCAM-S+ (LVDS) standard to lead out on a connector.

14.2 Parallel Camera_1 Interface (CSI1 of IPU#2)

When the software multiplexing is correct initializing, is the parallel camera interface CSI1 with 20-data-bits available.

The following table shows the location of CSI1 camera signals at phyCORE-connector:

Pin #	Signal	ST	Voltage Domain	Description
X1B29	X_CSI1_DATA19	I	VDD_3V3_LOGIC	Camera1 D19
X1B30	X_CSI1_DATA18	I	VDD_3V3_LOGIC	Camera1 D18
X1B31	X_CSI1_DATA17	I	VDD_3V3_LOGIC	Camera1 D17
X1B32	X_CSI1_DATA16	I	VDD_3V3_LOGIC	Camera1 D16
X1B34	X_CSI1_DATA15	I	VDD_3V3_LOGIC	Camera1 D15
X1B35	X_CSI1_DATA14	I	VDD_3V3_LOGIC	Camera1 D14
X1B37	X_CSI1_DATA13	I	VDD_3V3_LOGIC	Camera1 D13
X1A27	X_CSI1_DATA12	I	VDD_3V3_LOGIC	Camera1 D12
X1A28	X_CSI1_DATA11	I	VDD_3V3_LOGIC	Camera1 D11
X1A29	X_CSI1_DATA10	I	VDD_3V3_LOGIC	Camera1 D10
X1A30	X_CSI1_DATA09	I	VDD_3V3_LOGIC	Camera1 D9
X1A32	X_CSI1_DATA08	I	VDD_3V3_LOGIC	Camera1 D8
X1B39	X_CSI1_DATA07	I	VDD_3V3_LOGIC	Camera1 D7
X1B40	X_CSI1_DATA06	I	VDD_3V3_LOGIC	Camera1 D6
X1B41	X_CSI1_DATA05	I	VDD_3V3_LOGIC	Camera1 D5
X1B42	X_CSI1_DATA04	I	VDD_3V3_LOGIC	Camera1 D4
X1A33	X_CSI1_DATA03	I	VDD_3V3_LOGIC	Camera1 D3
X1A34	X_CSI1_DATA02	I	VDD_3V3_LOGIC	Camera1 D2
X1A37	X_CSI1_DATA01	I	VDD_3V3_LOGIC	Camera1 D1
X1A38	X_CSI1_DATA00	I	VDD_3V3_LOGIC	Camera1 D0
X1A40	X_CSI1_HSYNC	I	VDD_3V3_LOGIC	Camera1 HSYNC
X1A39	X_CSI1_VSYNC	I	VDD_3V3_LOGIC	Camera1 VSYNC
X1B36	X_CSI1_PIXCLK	I	VDD_3V3_LOGIC	Camera1 PCLK
X1C22	X_CCM_CLKO2	O	VDD_3V3_LOGIC	Camera1 MCLK
Optional signals can use with camera ports.				
X1B23	X_I2C1_SCL	O	VDD_3V3_LOGIC	I²C1_SCL for camera control
X1B24	X_I2C1_SDA	I/O	VDD_3V3_LOGIC	I²C1_SDA for camera control
X1A35	X_CSI1_DATA_EN	O	VDD_3V3_LOGIC	e.g. switcher for phyCAM
X1A37	X_CSI1_DATA01	O	VDD_3V3_LOGIC	e.g. switcher for phyCAM

Table 2: CSI1 as parallel interface signal location at phyCORE connector

Together with an I²C bus, can a camera module which a CMOS camera-interface has, be connected in a simple manner. For example as phyCAM-P or phyCAM-S+ interface.

14.3MIPI/CSI-2 (Camera_2) Camera Interface

On the X1 module connector is the MIPI/CSI-2 camera interface with up to 4 data-lanes and one clock-lane available.

The following table shows the location of the signals:

Pin #	Signal	ST	Voltage Domain	Description
X1C35	X_CSI_CLK0P	LVDS_I	i.MX 6 internal	MIPI/CSI-2 clk+
X1C36	X_CSI_CLK0M	LVDS_I	i.MX 6 internal	MIPI/CSI-2 clk-
X1C30	X_CSI_D0P	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data0+
X1C31	X_CSI_D0M	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data0-
X1D27	X_CSI_D1P	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data1+
X1D28	X_CSI_D1M	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data1-
X1C33	X_CSI_D2P	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data2+
X1C34	X_CSI_D2M	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data2-
X1D29	X_CSI_D3P	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data3+
X1D30	X_CSI_D3M	LVDS_I	i.MX 6 internal	MIPI/CSI-2 data3-
Optional signals can use with camera ports.				
X1B23	X_I2C1_SCL	O	VDD_3V3_LOGIC	I²C1_SCL for camera control
X1B24	X_I2C1_SDA	I/O	VDD_3V3_LOGIC	I²C1_SDA for camera control
X1D16	X_CCM_CLKO1	O	VDD_3V3_LOGIC	Camera0 MCLK

Table 3: MIPI/CSI-2 signal location at phyCORE connector

Together with an I²C bus, and a camera-clock can a MIPI/CSI-2 camera module be connected.

Note:
When using the optional MIPI/CSI-2 interface eliminates the CSI0 or CSI1 interface.

14.3.1 Camera Interface on "MIRA" (PBA-C-06) base board (X10)

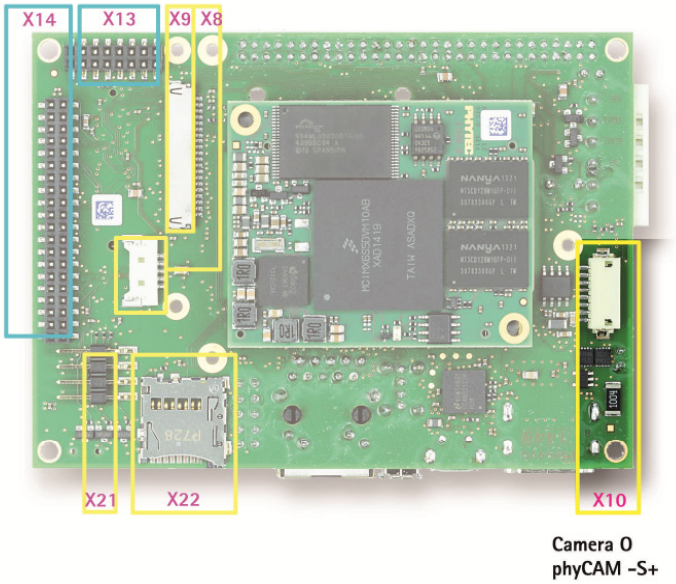


Figure 6: Camera Interface at Connector X10

The phyCORE i.MX 6 provides two types of camera interfaces (parallel and MIPI CSI-2). The parallel port on the carrier board can be expanded in many ways:
1) as phyCAM-P camera interface standard
2) as phyCAM-S+ camera interface standard
3) as phyCAM-G camera interface standard
4) as interface for customer parallel cameras

On the base board "MIRA" we convert the parallel Camera_0 interface in the phyCAM-S+ camera interface standard (see Fig 7). The phyCAM-S+ interface is support on connector X10. Information's to phyCAM-S+ are in the phyCAM-manual (L-748).

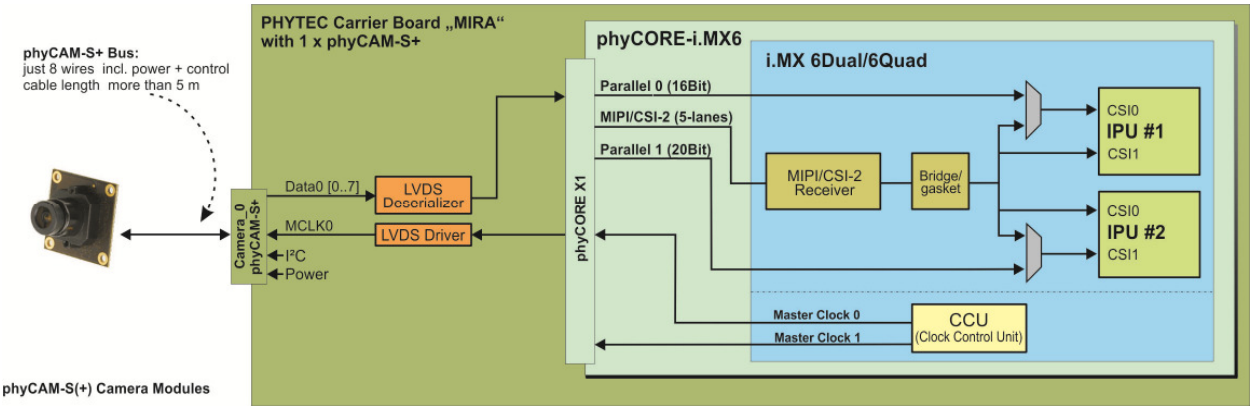


Figure 7: phyCAM-S+ Camera Interface on base board "MIRA"

Information's to the other ways, are described in the phyFLEX-i.MX6 Baseboard manual (L-773) and in the phyCAM-manual (L-748).

The table below shows the pinout of connector X10:

Pin #	Signal Name	Description
1	Camera0_L0+	LVDS Input+
2	Camera0_L0-	LVDS Input-
3	Camera0_RXCLK-	LVDS Clock-
4	I2C_SDA_CAMERA	I^2C Data
5	I2C_SCL_CAMERA	I^2C Clock
6	Camera0_RXCLK +	LVDS Clock+
7	VCC_CAMERA0	Power supply camera (3.3 V)
8	GND	Ground

Table 4: PHYTEC Camera Connector X11

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